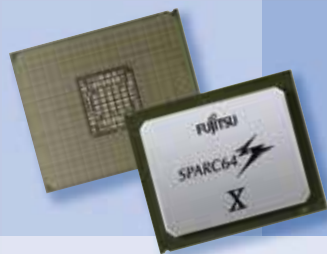
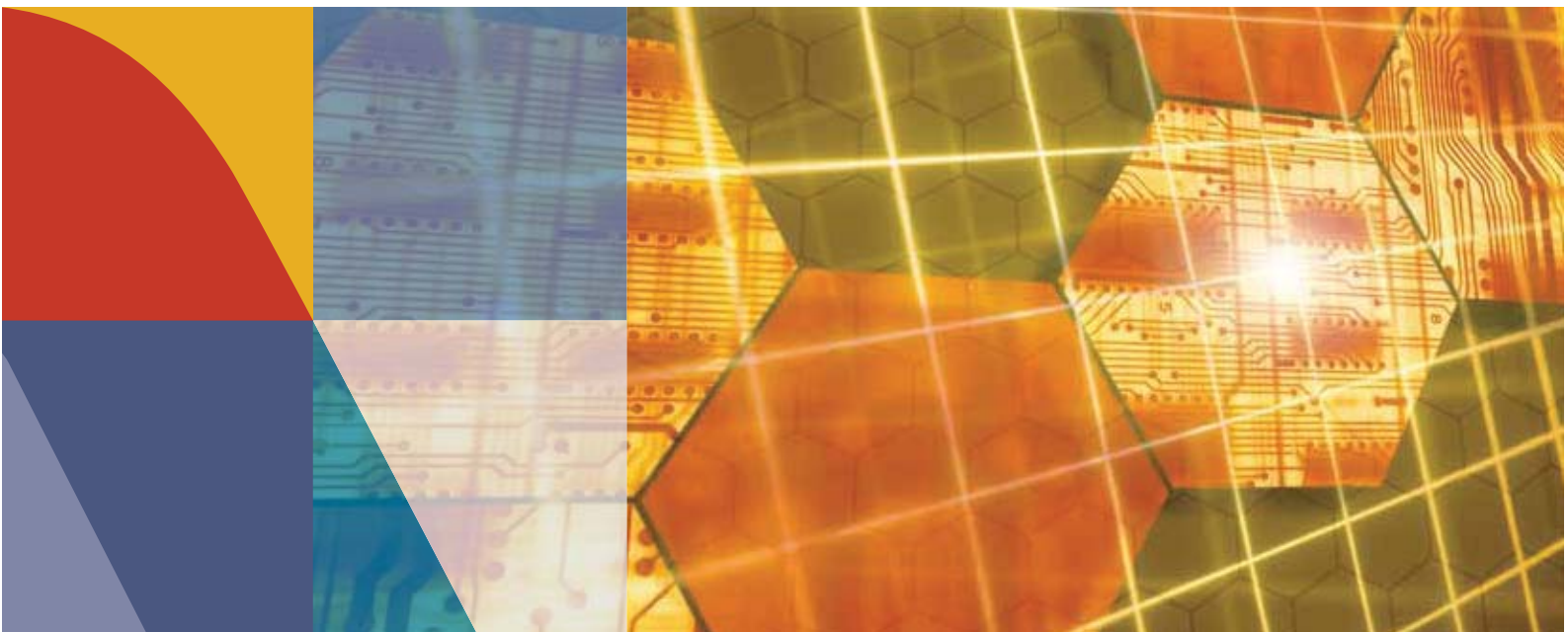


Using high-speed parallel computing to create new business value with the SPARC64 X processor



SPARC64 



SPARC64™ X Processor with Fujitsu M10 Server for Faster Optimization Processing



Amazing advances in ICT (Information and Communication Technology) are bringing significant changes to the business environment of companies today.

Large volumes of data are being produced daily from various types of smart devices and sensors installed in companies, homes, cars, and other locations, and this data is starting to be used for a wide array of applications in our society and environment.

One major change has been the growing importance of how companies can find ways to perform advanced and high-speed analysis on and use big data to differentiate themselves from other competitors in the business and to create new services that go beyond their company and industry boundaries.

Evaluation of Parallel Arithmetic Processing Performance

Overview

This evaluation is based on a sports scheduling problem that uses the MSI Numerical Optimizer™ *1, which is a general-purpose mathematical planning package.

The sports scheduling problem involves the creation of head-to-head schedules for league games. Because it is difficult to find an exact solution to this problem, the MSI Numerical Optimizer finds an approximate solution. The accuracy of this approximate solution increases based on the number of times (attempts) that a “search for a solution” is executed. This evaluation is used to measure how many of these searches for a solution can be executed within a certain period of time, demonstrating the linear scalability of the Fujitsu M10.

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Environment

The Fujitsu M10 environment used for this evaluation is shown below.

Model	Fujitsu M10-4S
CPU	SPARC64 X 3.0GHz/24MB cache 8 CPUs/128 cores /256 threads
Memory	512 GB
OS	Oracle Solaris 11.1

* The number of cores is 128, however SPARC64 X uses SMT (Simultaneous multithreading) to simultaneously execute two threads per core. As a result, at the OS level, Fujitsu M10 appears to have 256 CPUs.

Schedule Creation Conditions

The schedule creation conditions are shown below.

- Creation of head-to-head schedule for league games using 20 teams
- The time limit is 70 seconds (measuring how many attempts are possible within 70 seconds)

Evaluation Results

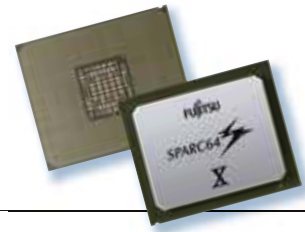
The evaluation results are shown in Table 1.

No. of processes	Total number of attempts	Average number of attempts per process
1	2,331	2,331
32	68,267	2,133
64	134,885	2,108
128	246,656	1,927
256	327,052	1,278

* The orange number (=128) shown in the “No. of processes” column in Table 1 is the measurement for “No. of processes = No. of cores”. The blue number (=256) is the measurement for “No. of processes = Maximum number of simultaneously executed threads”. (The same applies to the figure below.)

* This evaluation was conducted three times for each number of processes, and the median value was taken as the total number of attempts for each result. The average number of attempts per process was calculated using “Number of attempts / No. of processes”.

Table 1. Evaluation Results



Linear Scalability

The results of plotting the number of processes and total number of attempts are shown in Fig. 1.

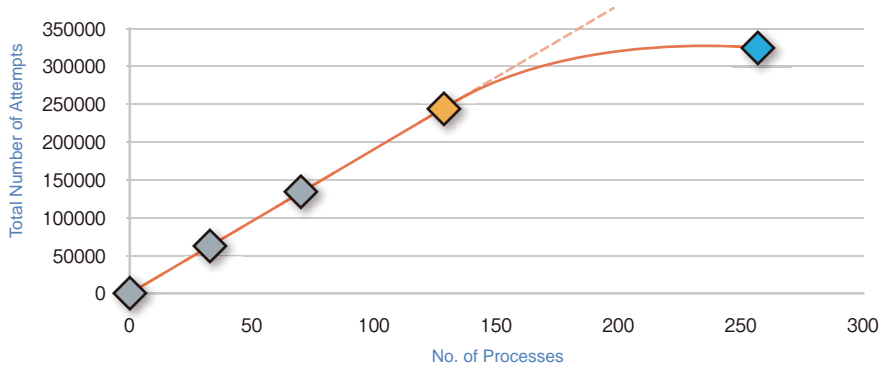


Fig. 1. Relationship Between Number of Processes and Total Number of Attempts

As shown in the graph, the total number of attempts increased linearly until the number of processes reached 128. The Fujitsu M10 used in this evaluation had 128 cores, and this result shows that these were used effectively.

Also, even when the number of processes was increased to 256, the total number of attempts increased by 1.3 times compared to the total number of processes at 128. (Specifically, the number of attempts per process dropped to about 1/1.5, but because the number of processes was doubled, the total number of attempts increased by 1.3 times.)

This is thought to be due to the effective utilization of simultaneous multi-threading by the SPARC64 X, which enabled efficient use of the CPUs.

Thread Efficiency

The examination results for the CPI^{*2} in this evaluation are shown in Fig. 2.

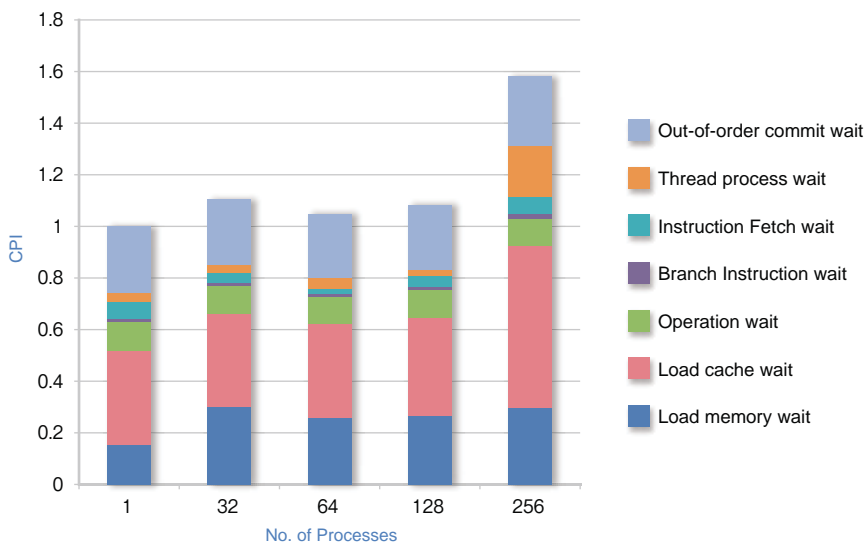


Fig. 2. Relationship Between Number of Processes and CPI

The CPI is virtually unchanged up to 128 processes. This supports the fact that the performance improved linearly up to 128 processes in the evaluation results. At 256 processes, the CPI increased by about 1.6 times per process. This means that performance was about 1/1.5, but this is also consistent with an average of attempts per process of 1/1.5.

Looking at the breakdown, we can see that the "Thread process wait" and "Load cache wait" increased. At 256 processes, the simultaneous multi-threading function enables the assigning of two processes to a single core, but as a result, each process can only use one-half of the L1 cache of the CPU. This causes the L1 cache to fill with data (so that loading from L2 cache becomes necessary), which leads to an increase in the load cache wait.

This increase in the thread processing wait is due to the occurrence of resource conflicts between different threads.

^{*2} Cycles Per Instruction=Average number of clock cycles required to execute a single CPU instruction

The problem area in this evaluation program was the size that could fit within the L2 cache, and that each process was completely independent. This evaluation showed extremely positive results for scalability up to 128 processes.

Moreover, even when the number of processes was increased to twice the number of cores (=256), we found that SMT enabled further improvements in performance.

This evaluation indicates that there are an unlimited number of potential areas for optimization, such as large-scale shift scheduling. As system integrators that support our social infrastructure, both Fujitsu and the NTT DATA Group are building advanced analytical logic systems for solving a wide array of problems. To achieve this, CPUs capable of high-speed arithmetic processing of large volumes of data are essential, and we are forging ahead with businesses through our ongoing partnerships.

Results of This Evaluation

- Confirmation of the compatibility and superiority of optimization processing by the MSI Numerical Optimizer and the SPARC64 X multi-core environment
- Linear scalability is achieved even when the number of simultaneously-executed processes is increased up to the number of cores
- Even when the simultaneously-executed processes exceed the number of cores, SMT continues to function effectively and to provide improved performance

Fujitsu M10

Fujitsu M10 is a revolutionary new server that combines exclusive Fujitsu technologies adopted from super-computers and mainframes. Fujitsu M10 combines high reliability with high-speed computational processing to achieve realtime processing and the world's top scalability to provide the optimum platform leading to the success of your businesses.

SPARC64 X for Realtime Processing

SPARC64X processors with the Fujitsu M10 server incorporate technology for high-speed parallel arithmetic processing and in-memory processing to enable realtime processing.

High-speed parallel arithmetic processing	SMT is used to enable efficient processing in the SPARC64 X thread structure. Moreover, each thread includes four computing units for performing a large number of computations simultaneously and efficiently.
In-memory processing	The SPARC64 X processor has eight memory buses, which are connected directly. This achieves low latency to allow memory access at high bandwidths for high-speed processing of large amounts of data.

World's Top Scalability

Fujitsu M10 adopts the Building Block method of expansion, which enables the addition of up to 16 chassis to provide high scalability that supports up to 64 CPUs and 1,024 cores. A cutting-edge, fast interconnection technology is used to connect chassis and to provide an expansive bandwidth based on technology developed for super-computers, achieving linear scalability in performance.

* For details on Fujitsu M10 and SPARC64 X, see <http://www.fujitsu.com/sparc/>.

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