Description

The high-performance MB86R24 “Triton-C” combines the latest ARM® Cortex™-A9 dual CPU core with state-of-the-art, embedded 2.5D and 3D graphics cores. This third-generation application processor is the first device in Fujitsu’s new “Blueline” family of high-performance GDCs.

The 3D core incorporates Imagination Technologies’ POWERVR™ SGX543-MP1, which supports open standard API formats such as OpenGL® ES 2.0. The POWERVR core uses Tile-Based Deferred Rendering (TBDR) for render processing, which reduces performance loads on the CPU and GPU, and increases system capacity.

The high-end SoC also combines six video-capture inputs and three independent parallel display outputs.

The chip’s architecture has been optimized for the simultaneous use of all functional blocks, virtually eliminating performance gaps. The device’s harmonized structure permits the simultaneous rendering of independent 2.5D and 3D graphics, the capturing of multiple video streams, and the display of content to multiple sources.

With its outstanding rendering performance and multiple standard and automotive-specific peripheral interfaces, this device is appropriate for a wide range of demanding automotive and industrial applications.

Features

- ARM Cortex-A9, dual-core 533 MHz (600 MHz in restricted operating conditions) per core
- 2.5D graphics engine
- 3D graphics engine: POWERVR, SGX543-MP1
  - Tile-Based Deferred Rendering (TBDR)
  - Support for OpenGL ES 2.0, OpenVG™ 1.1 and OpenCL™ 1.0
- Video capture from five independent channels
- Broad support for standard and automotive-specific peripherals
- Three independent parallel display controllers for display up to 1920x768
- Up to 1GB of graphics memory

Applications

- Dashboards
- HUD (head-up display) systems
- CID (central information display) systems
- RSE (rear seat entertainment) systems
Specifications

**Power-supply voltage**
- IO: 3.3±0.3 V and core: 1.2±0.1 V and DDR3: 1.5±0.1 V (DDR2: 1.8±0.1 V)

**Package: FCBGA-672**
- 27mm x 27mm, 1.0 pitch

**External RAM interface**
- Unified 16/32/64-bit DDR2/3 memory interface
- DDR2: 400/533/800Mbit/s and DDR3: 800/1066Mbit/s

**External Flash interface for NOR and NAND (serial, parallel), managed NAND (eMMC)**

**Internal SRAM**
- 3x 32k built-in SRAM

**Central processor cores**
- ARM Cortex-A9, dual-core 533 MHz (600 MHz in restricted operating conditions) per core
- 2.5 DMIPS/MHz
- 32 kB instruction cache / 32 kB data cache, 512 kB L2 cache
- ARM NEON™ SIMD Engine
- JTAG ICE interface
- Java acceleration (Jazelle technology)
- VFP instruction set (VFPv3)

The "Triton-C" is well-suited for a variety of graphics applications.
Multi-layer AXI/AHB bus architecture

External bus (16 bit)

Graphics cores
• 2.5D graphics engine
• 3D graphics engine: PowerVR SGX543-MP1
  – Tile-Based Deferred Rendering (TBDR)
  – OpenGL ES 2.0, OpenVG 1.1 and OpenCL 1.0

Display controller
• Three independent parallel display controllers up to 1920x768
• Display layers per controller: 8 + 4 alpha + cursor (Display0, Display1), up to 3 display layers (Display2)
• Gamma correction unit (color LUT)
• Dithering unit display resolution up to WUXGA

Output formats/channels
• Up to 3x single-channel DRGB888 or 1x dual-channel DRGB888
• 1x single or dual-channel RSDS (replaces one or two DRGB888 output if selected)

Embedded TCON
• Support for dual-view display
• Support for dual-channel output (for HD resolutions)
• Warping on the fly (Display2)

Video capture
• 6 independent channels
• MIPI-CSI2, ITU-R BT.656, SMPTE 293M-2003, SMPTE 296M-2001
• YCbCr 4:2:2 interlaced, YCbCr 4:2:2 progressive
• SMPTE 296M-2001, SMPTE 274M-2005
• RGB888 – 1 channel
• Color conversion
• Histogram unit, histogram equalization

Peripherals and more
• SPI slave host interface – 1 channel
• SPI master – 2 channels
• Ethernet MAC
  – 10/100/1000 Mbit
  – IEEE 1588 support
• USB 2.0 host or function – 1 channel
• SDIO/MMC – 1 channel
• UART – 6 channels
• USART – 5 channels
• PS – 2 ports
• I²C – 4 channels
• PWM – 8 channels
• Timer 16/32 bit - 2 channels
• Signature Unit (signature and checksum calculation for display content, intended use: ASIL)

Automotive interfaces
• CAN (I/O voltage: 3.3 V) – 2 channels
• MediaLB (MOST150) – 1 channel, support for 3 pin and 6 pin

Software support
• Linux Board Support Package (BSP) including:
  – Kernel 3.x (including dual-core support)
  – U-Boot (boot loader)
  – Peripherals drivers
  – Tool chain
• Graphics software stack providing APIs for multiple capture and display units
  – 3D graphics: OpenGL ES 2.0, EGL 1.4; OpenGL ES shading language 1.0
  – 2.5D pixel graphics functionality (including warping-on-the-fly)
  – 2.5D vector graphics: OpenVG 1.1 (special request necessary)
• Video and image processing
  – VXD392 driver support for media decoding middleware suppliers/integrators
  – Driver support for OpenCL 1.0 (special request necessary)
• Tooling
  – Fujitsu Developer Suite for setup, debugging and application support
  – CGI Studio (2.5D and 3D)
"Triton-C" is a "right-sized" SoC featuring a unique blend of special-purpose functional blocks combined with a high-powered, standards-based GPU.

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