AN app note

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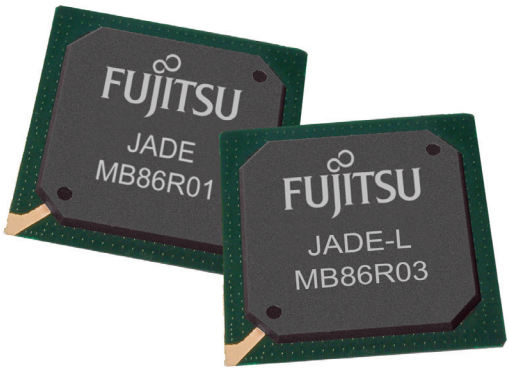
Using NOR Flash Bigger than 32MB with the MB86R0x "Jade" Family



Introduction to Jade and External Bus Interface

The MB86R0x "Jade" devices are part of a family of graphics Systems-on-a-Chip (SoCs) that feature an ARM926 processor, a built-in 3D graphics engine, and a variety of peripheral sets. The SoC is ideal for use in graphics applications in automotive, industrial, and medical applications.

The MB86R0x "Jade" family is equipped with an external bus interface that can be used with NOR Flash memory and to control other slave devices. This interface is connected directly to the AHB bus inside the SoC and operates in an asynchronous fashion.

How the External Bus Interface Works

The interface on the MB86R0x "Jade" devices consists of standard memory bus signals for address, data, and control. The different aspects of interface operation are controlled using register settings. For example, the external bus interface can be configured to a 32-16-, or 8-bit wide data bus. The address range of the external device can be set up to accommodate a range of memory sizes. Read and write timing is also configurable.

The three registers used to set up the external bus interface operation are:

- MCFMODE: Configures the ready mode, page access mode, and data bus width.
- MCFAREA: Defines the address range of the external device.
- MCFTIMING: Defines the read and write timing for communication with the external device.

Setting Up the Address Range for the External Device (Memory Size)

The address range or addressable memory size for the external device is managed using the MCFAREA register, which provides two key controls:

- Mask: This determines the addressable memory size.
- ADDR (Address): This determines the starting address of the external device within the memory of the MB86R0x "Jade" device.

These controls are in the form of bits that can be set in the MCFAREA register. Together they determine the start address and address range for the external device.

For example, for a 16MB NOR Flash, Mask bits should be set to 0001111. ADDR bits can be set to "0" so that the range starts from 0x1000_0000. For further details, please refer to the "External Bus Interface" chapter of the MB86R0x "Jade" device specification.

The MCFAREA register setting allows an address range up to 32MB only per chip select. A 32MB range may be sufficient for most applications; however, an address range in excess of that can sometimes be needed for the external boot ROM device. The following section describes how this can be achieved.

How to Support More Than 32MB

Although MB86R0x "Jade" devices have three chip-select pins for the external bus interface, only one of them (CS4) can be used for an external boot ROM device, such as NOR Flash. Therefore, with the register-setting options discussed above, the address range is limited to 32MB for CS4. There are two possible ways to surpass that limit.

- Using GPIOs to emulate the extra address lines needed for a bigger address range.
- Using external glue logic to derive the extra address lines from the additional chip-select pins.

1. Using GPIOs

MB86R0x "Jade" devices have plenty of GPIO pins. Two of them can be used to emulate the extra address pins (A25 and A26) needed to connect memory higher than 32MB. As the table below shows, a memory size of up to 128MB can be connected using this technique. To the external bus interface, the four 32MB areas will appear the same. (All have the same address range.) Only the software controlling the GPIOs will know which area is being accessed.

Table 1 – Memory Area and GPIO Relationship

	Address Range	A26	A25
First 32MB	0x1000_0000 to 0x11ff_ffff	L	L
Second 32MB	0x1000_0000 to 0x11ff_ffff	L	H
Third 32MB	0x1000_0000 to 0x11ff_ffff	H	L
Forth 32MB	0x1000_0000 to 0x11ff_ffff	H	H

There are a few points to note when using this technique:

- The GPIO pins used to emulate A26 and A25 should be stable at power-on.
- Both GPIOs should be set to low.
- The boot code should reside in the top 16MB (0x1000_0000 to 0x10ff_ffff).
- Since GPIO pins are software controlled and possibly slower than hardware-driven pins, it is important to make sure that they have the right state when needed. When the memory address changes such that the GPIOs need to change the state, the GPIO state must change before the memory is accessed.
- The address issued by the CPU should be same as the area to be accessed.
- Software must manage GPIO pins and must control which memory area is being accessed.
- It may be possible to access the memory size even up to 256MB. IBIS simulation should be used in advance to make sure that Jade's external bus interface has sufficient signal drive capability for the 256MB Flash device.

2. Using External Glue Logic

If external glue logic is permitted, the extra chip select pins (CS2 and CS4) of the external bus interface can be used to drive chip-select pins and additional address lines for the external device. The difference from the first approach is that the external bus interface will be aware of the entire address range as its chip-select pins are accessing the memory area higher than 32MB. The maximum addressable memory using this approach is only 96MB as there are only three chip-select pins in the external bus interface.

The following table illustrates this glue logic design.

Table 2 – Memory Area and Glue Logic Relationship

Address Range	MB86R0x "Jade" Side	External Device Side
0-32MB	XCS4	CE#
32-64MB	XCS4 AND XCS2	CE#
	NOT XCS2	MEM_ADDR25 *
64-96MB	XCS4 AND XC2 AND XCS0	CE#
	NOT XCS2	MEM_ADDR25 **
	NOT XCS0	MEM_ADDR26 ***

* When XCS4 is active, MEM_ADDR25 is "L." When XCS2 is active, MEM_ADDR25 is "H."

** When XCS4 is active, MEM_ADDR25 and MEM_ADDR26 are "L."
When XCS2 is active, MEM_ADDR25 is "H" and MEM_ADDR26 is "L."
When XCS0 is active, MEM_ADDR25 is "L" and MEM_ADDR26 is "H."

*** Maximum capacity is 96MB because the MB86R0x "Jade" external bus interface has only three chip selects available.

In conclusion, the MB86R0x "Jade" family of SoCs can support NOR Flash capacity up to 128MB. This can be very useful in systems that have high memory requirements due to the graphics involved.

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