

TB-FMCH-DP3

Hardware User's Manual

Rev.1.00

Revision history

Revision	Date	Description	Publisher
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Introduction

Thank you for purchasing the **TB-FMCH-DP3** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- Before using the product, read these safety precautions carefully to assure correct use.
- These precautions contain serious safety instructions that must be observed.
- After reading through this manual, be sure to always keep it handy.

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

 Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
 Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
 Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.



Warning

	In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	If an unpleasant smell or smoking occurs, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	Do not disassemble, repair or modify the product. Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	Do not touch a cooling fan. As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	Do not place the product on unstable locations. Otherwise, it may drop or fall, resulting in injury to persons or failure.
	If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.
	Do not touch the product with a metallic object. Otherwise, a fire or electric shock may occur.
	Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.
	Do not get the product wet or touch it with a wet hand. Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	Do not touch a connector on the product (gold-plated portion). Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

**Caution****Do not use or place the product in the following locations.**

- Humid and dusty locations
- Airless locations such as closet or bookshelf
- Locations which receive oily smoke or steam
- Locations exposed to direct sunlight
- Locations close to heating equipment
- Closed inside of a car where the temperature becomes high
- Sticky locations
- Locations close to water or chemicals

Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.

**Do not place heavy things on the product.**

Otherwise, the product may be damaged.

■ Disclaimer

This product is an evaluation board for Displayport interface. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

- (1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
- (2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
- (3) Use of this product against the instructions given in this manual.
- (4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

- (1) Erasure or corruption of data arising from use of this product.
- (2) Any consequences or other abnormalities arising from use of this product, or
- (3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Board Accessories

Related documents:

All documents relating to this Board can be downloaded from our website. Please refer to attached paper of the products.

Board Accessories:

- Spacer set : x1

2. Overview

The TB-FMCH-DP3 provides test environment for DisplayPort Standard Version1, Revision 2a.

It supports below features

4 Lane of 1.62Gbps, 2.7Gbps and 5.4Gbps

It uses TI SN75SP130 for Source(TX) and SN65DP159 for Sink(RX)

AUX Communication.(FAUX is not supported)

Also, it could stack up two TB-FMCH-DP3 for expand more channels.

Notice: This board is used with Xilinx's Displayport IP core.

Some points are not tested because IP does not use.

Question for IP core and reference design, please contact to Xilinx.

3. Feature

DisplayPort Driver IC: Texas Instruments, SN75DP130SS

DisplayPort Redriver IC: Texas Instruments, SN65DP159RGZ

PLLIC: Texas Instruments, LMK04906

DisplayPort connector: JAE, DP1RD20JQ1R400

FMC connector: Samtec, ASP-134488-01 / ASP-134486-01

	K	J	H	G	F	E	D	C	B	A
1	VREF_B M2C	GND	VREF_A M2C	GND	PG M2C	GND	PG C2M	GND	RES1	GND
2	GND	CLK3 M2C P	PRSN1 M2C L	CLK1 M2C P	GND	HA01 P CC	GND	DP0 C2M P	GND	DP1 M2C P
3	GND	CLK3 M2C N	GND	CLK1 M2C N	GND	HA01 N CC	GND	DP0 C2M N	GND	DP1 M2C N
4	CLK2 M2C P	GND	CLK0 M2C P	GND	HA00 P CC	GND	GBTCLK0 M2C P	GND	DP9 M2C P	GND
5	CLK2 M2C N	GND	CLK0 M2C N	GND	HA00 N CC	GND	GBTCLK0 M2C N	GND	DP9 M2C N	GND
6	GND	HA03 P	GND	LA00 P CC	GND	HA05 P	GND	DP0 M2C P	GND	DP2 M2C P
7	HA02 P	HA03 N	LA02 P	LA00 N CC	HA04 P	HA05 N	GND	DP0 M2C N	GND	DP2 M2C N
8	HA02 N	GND	LA02 N	GND	HA04 N	GND	LA01 P CC	GND	DP8 M2C P	GND
9	GND	HA07 P	GND	LA03 P	GND	HA09 P	LA01 N CC	GND	DP8 M2C N	GND
10	HA06 P	HA07 N	LA04 P	LA03 N	HA08 P	HA09 N	GND	LA06 P	GND	DP3 M2C P
11	HA06 N	GND	LA04 N	GND	HA08 N	GND	LA05 P	LA06 N	GND	DP3 M2C N
12	GND	HA11 P	GND	LA08 P	GND	HA13 P	LA05 N	GND	DP7 M2C P	GND
13	HA10 P	HA11 N	LA07 P	LA08 N	HA12 P	HA13 N	GND	GND	DP7 M2C N	GND
14	HA10 N	GND	LA07 N	GND	HA12 N	GND	LA09 P	LA10 P	GND	DP4 M2C P
15	GND	HA14 P	GND	LA12 P	GND	HA16 P	LA09 N	LA10 N	GND	DP4 M2C N
16	HA17 P CC	HA14 N	LA11 P	LA12 N	HA15 P	HA16 N	GND	GND	DP6 M2C P	GND
17	HA17 N CC	GND	LA11 N	GND	HA15 N	GND	LA13 P	GND	DP6 M2C N	GND
18	GND	HA18 P	GND	LA16 P	GND	HA20 P	LA13 N	LA14 P	GND	DP5 M2C P
19	HA21 P	HA18 N	LA15 P	LA16 N	HA19 P	HA20 N	GND	LA14 N	GND	DP5 M2C N
20	HA21 N	GND	LA15 N	GND	HA19 N	GND	LA17 P CC	GND	GBTCLK1 M2C P	GND
21	GND	HA22 P	GND	LA20 P	GND	HB03 P	LA17 N CC	GND	GBTCLK1 M2C N	GND
22	HA23 P	HA22 N	LA19 P	LA20 N	HB02 P	HB03 N	GND	LA18 P CC	GND	DP1 C2M P
23	HA23 N	GND	LA19 N	GND	HB02 N	GND	LA23 P	LA18 N CC	GND	DP1 C2M N
24	GND	HB01 P	GND	LA22 P	GND	HB05 P	LA23 N	GND	DP9 C2M P	GND
25	HB00 P CC	HB01 N	LA21 P	LA22 N	HB04 P	HB05 N	GND	GND	DP9 C2M N	GND
26	HB00 N CC	GND	LA21 N	GND	HB04 N	GND	LA26 P	LA27 P	GND	DP2 C2M P
27	GND	HB07 P	GND	LA25 P	GND	HB09 P	LA26 N	LA27 N	GND	DP2 C2M N
28	HB06 P CC	HB07 N	LA24 P	LA25 N	HB08 P	HB09 N	GND	GND	DP8 C2M P	GND
29	HB06 N CC	GND	LA24 N	GND	HB08 N	GND	TCK	GND	DP8 C2M N	GND
30	GND	HB11 P	GND	LA29 P	GND	HB13 P	TDI	SCL	GND	DP3 C2M P
31	HB10 P	HB11 N	LA28 P	LA29 N	HB12 P	HB13 N	TDO	SDA	GND	DP3 C2M N
32	HB10 N	GND	LA28 N	GND	HB12 N	GND	3P3VALUX	GND	DP7 C2M P	GND
33	GND	HB15 P	GND	LA31 P	GND	HB19 P	TMS	GND	DP7 C2M N	GND
34	HB14 P	HB15 N	LA30 P	LA31 N	HB16 P	HB19 N	TRST_L	GA0	GND	DP4 C2M P
35	HB14 N	GND	LA30 N	GND	HB16 N	GND	GA1	120VW	GND	DP4 C2M N
36	GND	HB18 P	GND	LA33 P	GND	HB21 P	3P3V	GND	DP6 C2M P	GND
37	HB17 P CC	HB18 N	LA32 P	LA33 N	HB20 P	HB21 N	GND	120VW	DP6 C2M N	GND
38	HB17 N CC	GND	LA32 N	GND	HB20 N	GND	3P3V	GND	GND	DP5 C2M P
39	GND	VIO_B M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5 C2M N
40	VIO_B M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			1 PC Connector	1 PC Connector			1 PC Connector	1 PC Connector		

Figure 3-1 High-pin Count Pin assignment

4. TB-FMCH-DP3 Function

4.1. Block Diagram

The following figure shows the block diagram of this Board.

CN4 is mounted to bottom side and it will connect to FPGA Evaluation boards.

Please see more detail of each circuit.

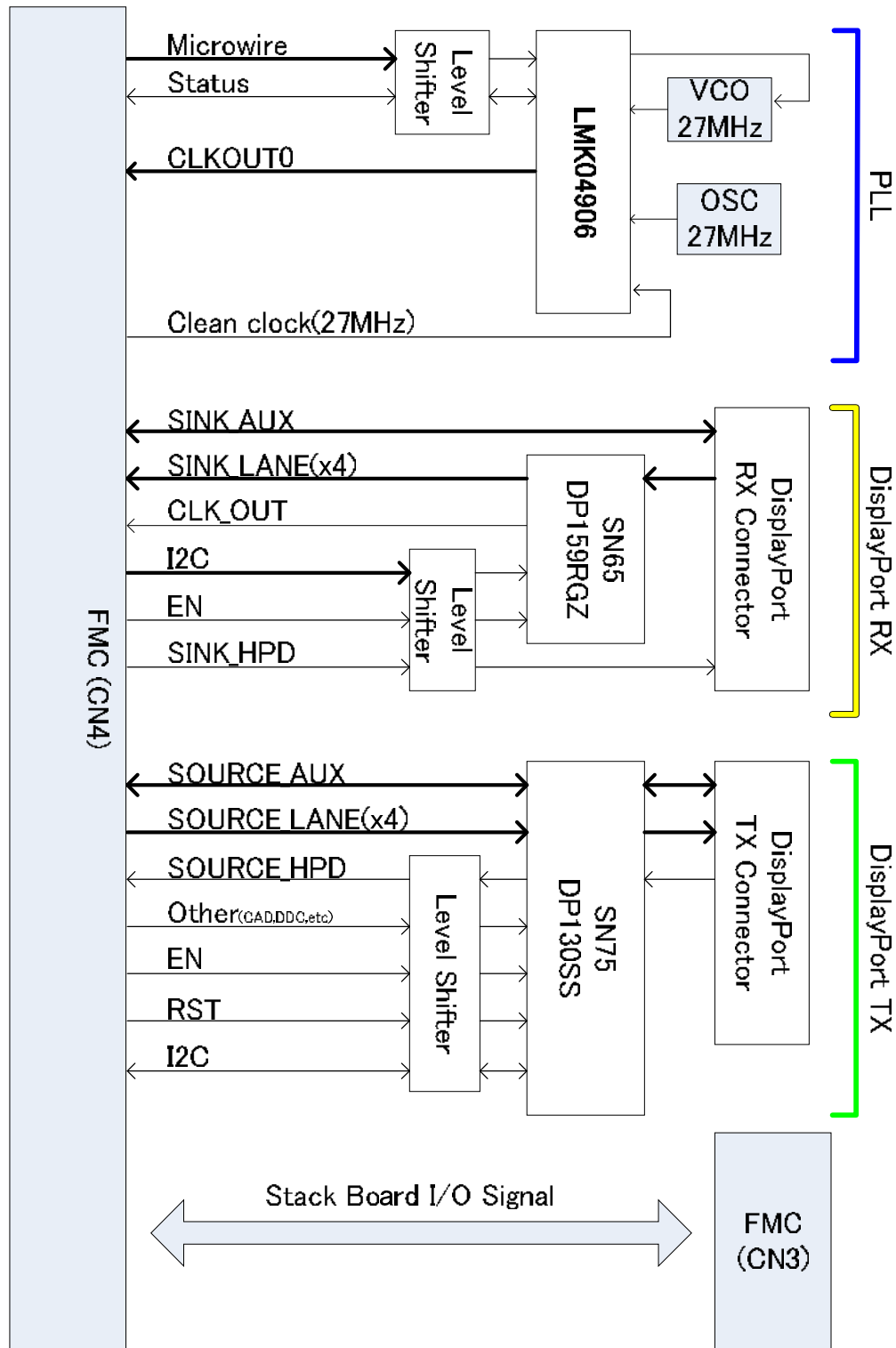


Figure 4-1 TB-FMCH-DP3 Block Diagram

4.2. External View of the Board

The following figures show the external views of the Board.

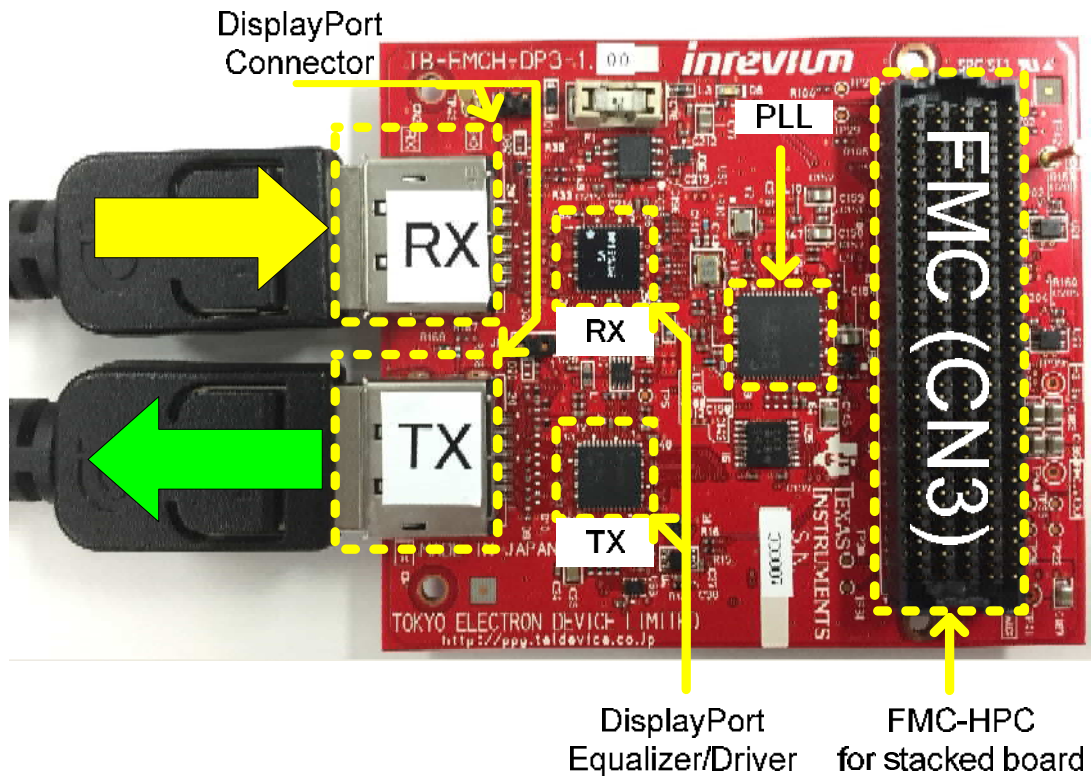


Figure 4-2 Top view

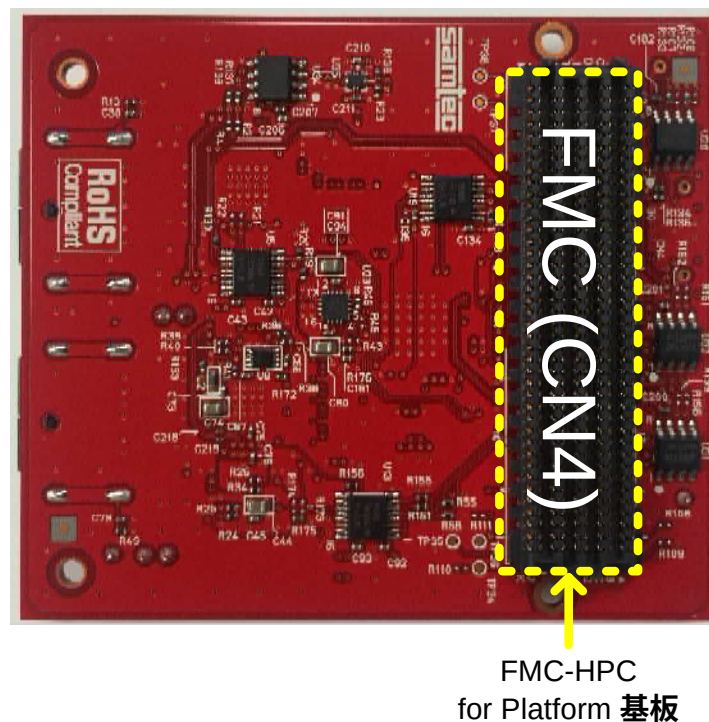


Figure 4-3 bottom view

4.3. Board Specification

External Dimensions: W:78.8mm x H:69.0mm
 Number of Layers: 8 Layers
 Board Thickness: 1.6mm
 Material: MEG-6(R-5775) or same specification.

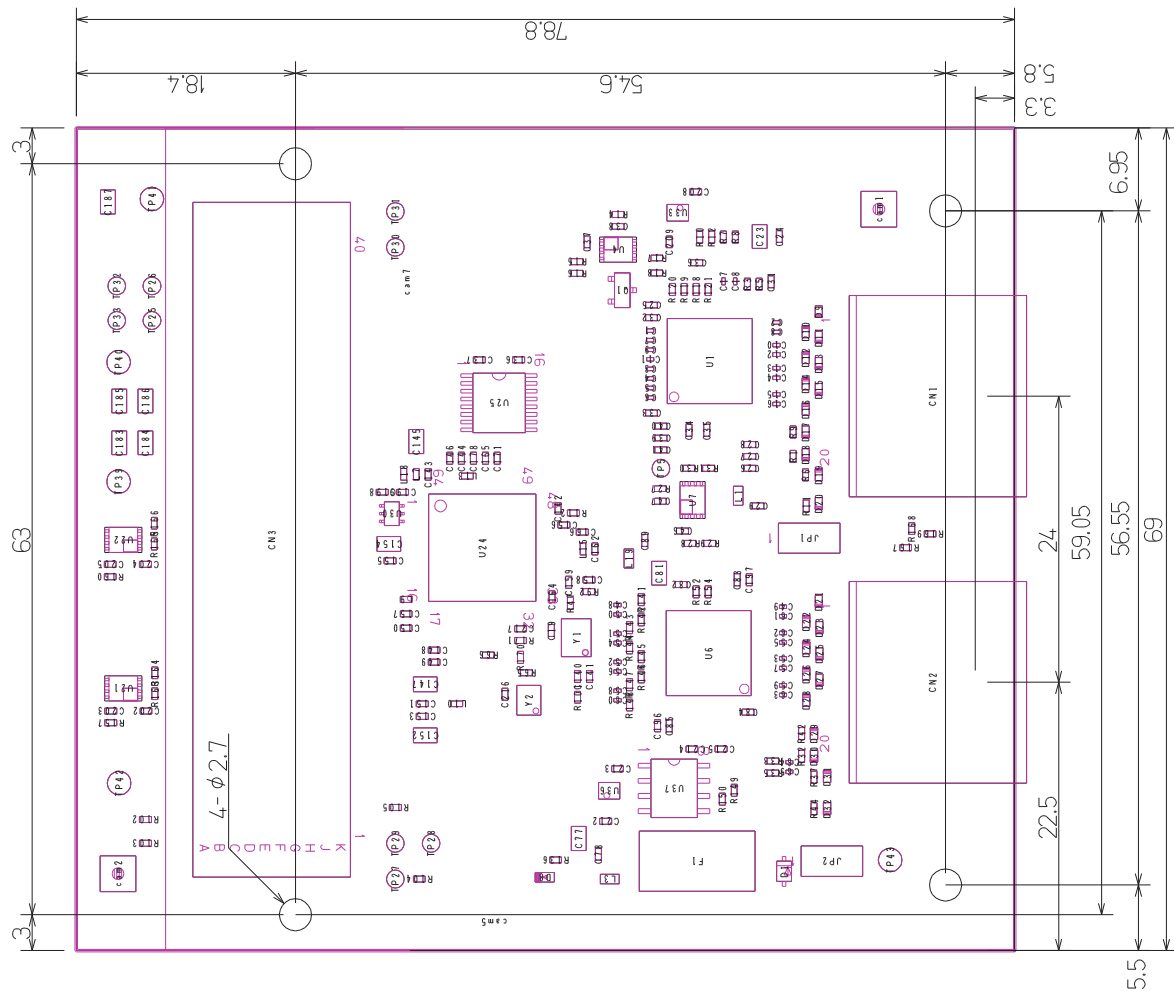


Figure 4-4 TB-FMCH-DP3 Dimension Diagram

4.4. Power Supply

This board generates required voltage(1.1V) of DP139 from +3.3V is coming from FMC Connector. Following is block diagram of power circuit.

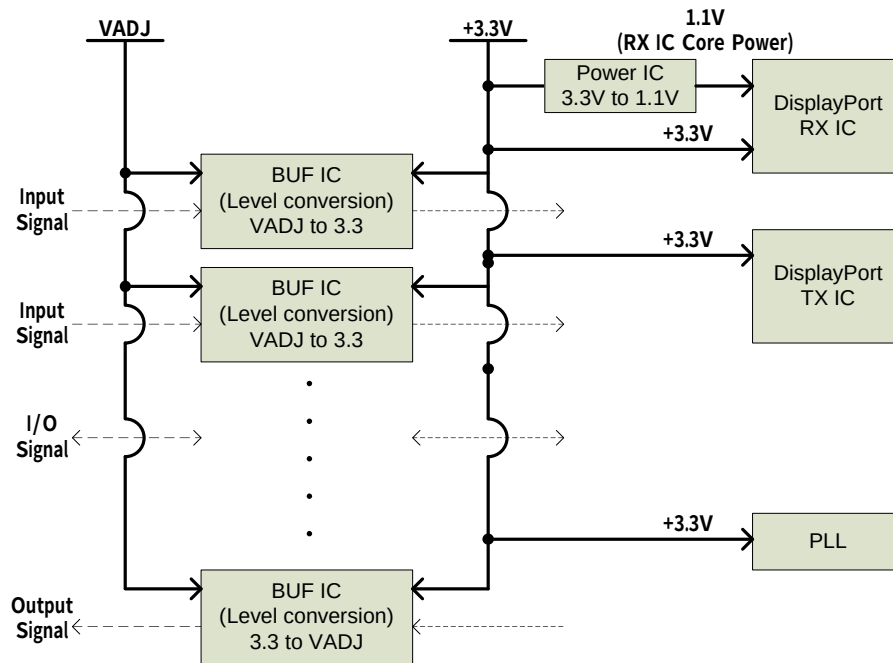


Figure 4-5 Block diagram of Power Circuit

4.4.1. IO Voltage

This board has a voltage level shifter for required signals.

FPGA IO voltage should be connected via FMC_VADJ on Carrier board.

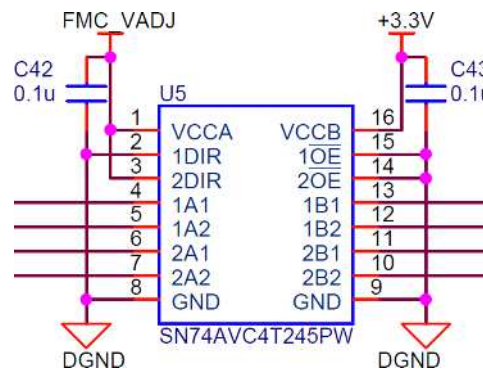


Figure 4-6 Voltage level shifter

4.5. Source(TX) Block

Following figure shows block diagram of Source circuit. DP130 keep signal integrity before transfer signal via cable and it can change swing level and pre-emphasis by AUX communication.

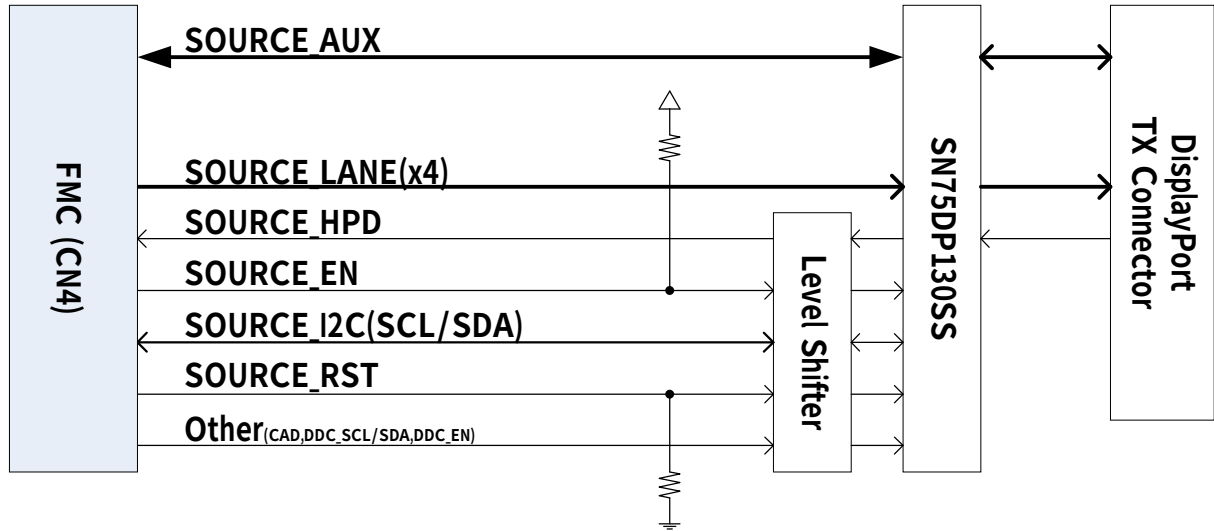


Figure 4-7 Block Diagram of Source circuit.

Table 4-1 Signals of Source Circuit

Signal Name	I/O	Description
SOURCE_AUX	IO	AUX signal. Bi-direction, Differential signals. Normally use this signals.
SOURCE_LANE	O	Main link of displayport
SOURCE_HPD	I	Hot Plug Detect Signal
SOURCE_EN	O	This is enabling DP130. It has pull-up register on the board. Enable: High(1)
SOURCE_I2C	IO	I2C signals for DP130. It is control interface without AUX communication. Normally, it is not required to controlling.
SOURCE_RST	O	Reset Signal of DP130. It has pull-down register on the board. Reset: High(1)
Other	-	CAD_DDC, SCL/SDA, DDC_EN (not tested)

Accessing to DP130 via I2C interface.

It is possible to accessing DP130 via I2C interface. About I2C address please refer to below table.

Note: Basically, it is controlled by AUX communication. I2C access is not required.

Table 4-2 DP130 I2C Address

I2C Address(7bit)	010 1110 (0x2E)
-------------------	-----------------

4.6. Sink(RX) Block

Following figure shows block diagram of Sink circuit. DP159 keep signal integrity as swing level and jitter.

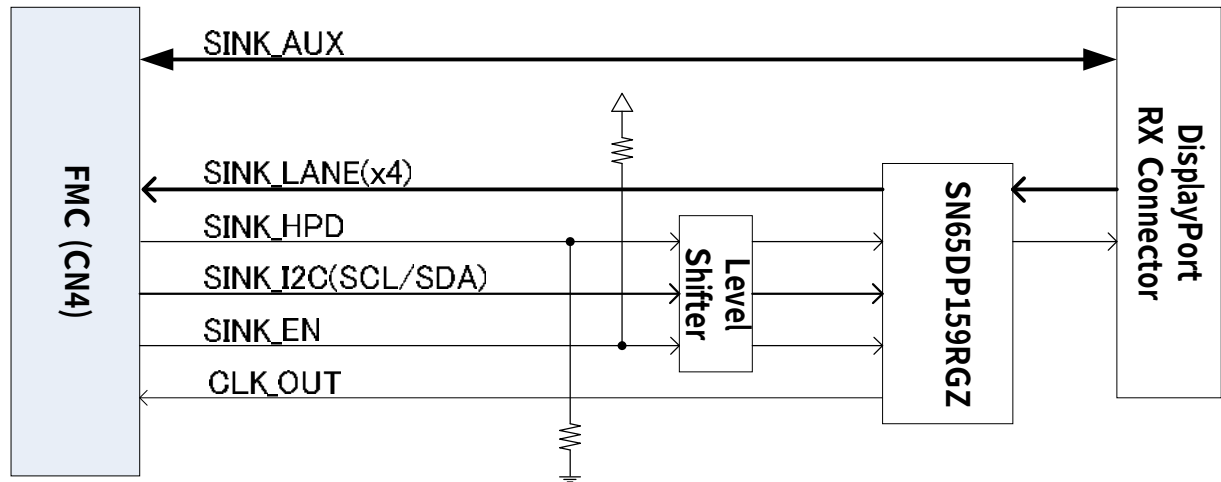


Figure 4-8 Block Diagram of Sink circuit

Table 4-3 Signals of Sink Circuit

Signal Name	I/O	Description
SINK_AUX	IO	AUX signal. Bi-direction, Differential signals. Normally use this signals.
SINK_LANE	I	Main link of displayport
SINK_HPD	O	Hot Plug Detect Signal
SINK_I2C	IO	I2C signals for DP159. It is control interface from Xilinx IP. DP159 required control from I2C because DP159 does not have AUX interface.
SINK_EN	O	This is output enable for DP159 It has pull-up register on the board. Enable: High(1)
CLKOUT	O	This is CDR clock output. Frequency is depended on DP159 internal PLL setting. It is related Xilinx Displayport IP control. HBR2(5.4Gbps): 270MHz HBR (2.7Gbps): 135MHz RBR (1.62Gbps): 81MHz

Accessing to DP159 via I2C interface.

It is possible to accessing DP159 via I2C interface. About I2C address please refer to below table.

Note: It is required to access DP159 via I2C. setting is depended on AUX communication.

Xilinx Displayport IP supports DP159 and I2C control.

Table 4-4 DP159 I2C Address

I2C Address(7bit)	101 1110 (0x5E)
-------------------	-----------------

4.7. Clock circuit

Following block diagram shows PLL circuit.

PLL device is TI “LMK04906” to generating reference clock of FPGA

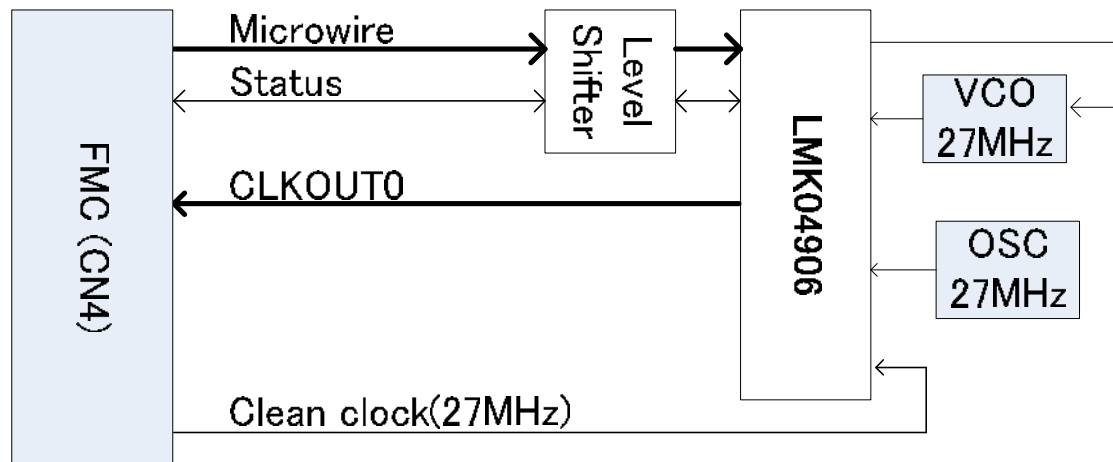


Figure 4-9 Block Diagram of PLL Circuit

Table 4-5 signals of PLL circuit

Signal Name	I/O	Description
Microwire	IO	Interface of LMK04906 internal resister. Please refer to data sheet of LMK04906.
Status	IO	Status signals. Status meaning is depended on resister settings.
CLKOUT0	O	Output clock. It is possible to use reference clock of FPGA.
Clean clock	O	Not Tested

4.7.1. Operation example of PLL

This section described how to set register of PLL for generating 135MHz, 81MHz, 162MHz and 270MHz.

- 1) Enable resister change: Write 0x00000031 to R31
- 2) Reset to PLL: write 0x00200000 to R00
- 3) Set following settings to each resister.

Table 4-6 PLL Resister settings (Step3)

Resister	Address[5:0]	Data[31:6]	Note
R 00*	0x00	0x0000009	Disable reset of PLL. CLKOut0 : 270MHz
		0x000000F	Disable reset of PLL. CLKOut0 : 162MHz
		0x0000012	Disable reset of PLL. CLKOut0 : 135MHz
		0x000001E	Disable reset of PLL. CLKOut0 : 81MHz
R 01*	0x01	0x0000009	CLKOut1 : 270MHz
		0x000000F	CLKOut1 : 162MHz
		0x0000012	CLKOut1 : 135MHz
		0x000001E	CLKOut1 : 81MHz
R 02*	0x02	0x0000009	CLKOut2 : 270MHz
		0x000000F	CLKOut2 : 162MHz
		0x0000012	CLKOut2 : 135MHz
		0x000001E	CLKOut2 : 81MHz
R 03	0x03	0x400_0001	Same setting, even different frequency.
R 04	0x04	0x400_0000	Same setting, even different frequency.
R 05	0x05	0x400_0000	Same setting, even different frequency.
R 06	0x06	0x088_8000	Same setting, even different frequency.
R 07	0x07	0x088_8000	Same setting, even different frequency.
R 08	0x08	0x088_8000	Same setting, even different frequency.
R 09	0x09	0x2AA_AAAA	Same setting, even different frequency.
R 10	0x0A	0x08A_0200	Same setting, even different frequency.
R 11	0x0B	0x02C_0881	Same setting, even different frequency.
R 12	0x0C	0x0D8_600B	Same setting, even different frequency.
R 13	0x0D	0x1D8_0003	Same setting, even different frequency.
R 14	0x0E	0x091_8000	Same setting, even different frequency.
R 15	0x0F	0x000_0000	Same setting, even different frequency.
R 16	0x10	0x00A_A820	Same setting, even different frequency.
R 24	0x18	0x000_0006	Same setting, even different frequency.
R 25	0x19	0x008_0030	Same setting, even different frequency.
R 26	0x2A	0x07D_4000	Same setting, even different frequency.
R 27	0x2B	0x080_0002	Same setting, even different frequency.
R 28	0x2C	0x000_8002	Same setting, even different frequency.
R 29	0x2D	0x000_002D	Same setting, even different frequency.
R 30	0x2E	0x010_002D	Same setting, even different frequency.

*This resister setting is depended on what frequency is required.

- 4) Disable resister change: write 0x00000001 to R31

For more detail, please refer to data sheet.

4.8. FMC connector for stacking

This board has two FMC connectors. One is connecting to FPGA Evaluation board and other is stacking same TB-FMCH-DP3 board.

In this section, it shows that lower FMC is “base board” and upper FMC is “stack board”.

Following figure shows signal connection when stacking two boards.

Signal of stack board will connect CN3 of base board then signal name is changed as “EX_***”. “EX_***” signals connect to FPGA carrier board via CN4 of base board.

An exception, PLL control signal and clock are not connecting to FPGA carrier board via base board.

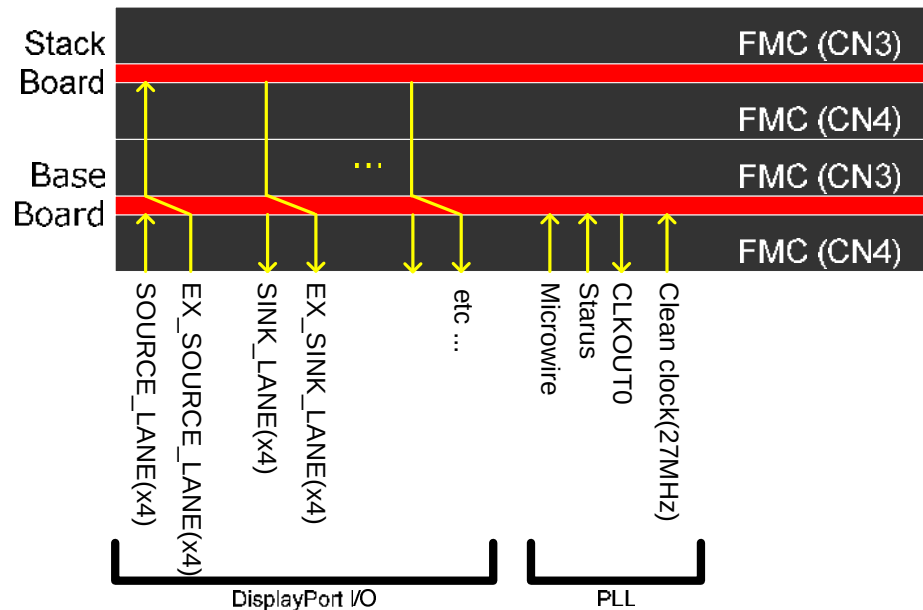


Figure 4-10 Signal connection of stacking two boards.



Figure 4-11 Stacked boards

Cation: Please confirm the notice of TB-FMCH-DP3.

4.9. Pin Assignment of CN4

Table 4-7 CN4 Pin assign (To carrier board) shows FMC pin assignment.

Signal direction is assigned as follows:

-"I": The signal came from carrier board to TB-FMCH-DP3.

-"O": The signal came from TB-FMCH-DP3 to carrier board.

Blue Character signal are connected to CN4 FMC Expansion connector.

Table 4-7 CN4 Pin assign (To carrier board)

A row in HPC pin assignment (CN4)				
#	FMC signal	I/O	Signal in schematic	Note
1	GND	-	GND	GND
2	DP1_M2C_P	O	SINK_ML_LANE1_P	SINK MainLink LANE1 (Positive)
3	DP1_M2C_N	O	SINK_ML_LANE1_N	SINK MainLink LANE1 (Negative)
4	GND	-	GND	GND
5	GND	-	GND	GND
6	DP2_M2C_P	O	SINK_ML_LANE2_P	SINK MainLink LANE2 (Positive)
7	DP2_M2C_N	O	SINK_ML_LANE2_N	SINK MainLink LANE2 (Negative)
8	GND	-	GND	GND
9	GND	-	GND	GND
10	DP3_M2C_P	O	SINK_ML_LANE3_P	SINK MainLink LANE3 (Positive)
11	DP3_M2C_N	O	SINK_ML_LANE3_N	SINK MainLink LANE3 (Negative)
12	GND	-	GND	GND
13	GND	-	GND	GND
14	DP4_M2C_P	O	EX_SINK_ML_LANE0_P	SINK MainLink LANE0 from expanded board(Positive)
15	DP4_M2C_N	O	EX_SINK_ML_LANE0_N	SINK MainLink LANE0 from expanded board (Negative)
16	GND	-	GND	GND
17	GND	-	GND	GND
18	DP5_M2C_P	O	EX_SINK_ML_LANE1_P	SINK MainLink LANE1 from expanded board(Positive)
19	DP5_M2C_N	O	EX_SINK_ML_LANE1_N	SINK MainLink LANE1 from expanded board (Negative)
20	GND	-	GND	GND
21	GND	-	GND	GND
22	DP1_C2M_P	I	SOURCE_ML_LANE2_P	SOURCE MainLink LANE2 (Positive)
23	DP1_C2M_N	I	SOURCE_ML_LANE2_N	SOURCE MainLink LANE2 (Negative)
24	GND	-	GND	GND
25	GND	-	GND	GND
26	DP2_C2M_P	I	SOURCE_ML_LANE1_P	SOURCE MainLink LANE1 (Positive)
27	DP2_C2M_N	I	SOURCE_ML_LANE1_N	SOURCE MainLink LANE1 (Negative)
28	GND	-	GND	GND
29	GND	-	GND -	GND
30	DP3_C2M_P	I	SOURCE_ML_LANE0_P	SOURCE MainLink LANE0 (Positive)
31	DP3_C2M_N	I	SOURCE_ML_LANE0_N	SOURCE MainLink LANE0 (Negative)
32	GND	-	GND	GND
33	GND	-	GND	GND
34	DP4_C2M_P	I	EX_SOURCE_ML_LANE0_P	SOURCE MainLink LANE0 (Positive, expanded board)
35	DP4_C2M_N	I	EX_SOURCE_ML_LANE0_N	SOURCE MainLink LANE0 (Negative, expanded board)
36	GND	-	GND	GND
37	GND	-	GND	GND
38	DP5_C2M_P	I	EX_SOURCE_ML_LANE1_P	SOURCE MainLink LANE1 (Positive, expanded board)
39	DP5_C2M_N	I	EX_SOURCE_ML_LANE1_N	SOURCE MainLink LANE1 (Negative, expanded board)
40	GND	-	GND	GND

B row in HPC pin assignment (CN4)				
#	FMC signal	I/O	Signal in schematic	Note
1	RES1	-	-	N.C
2	GND	-	GND	GND
3	GND	-	GND	GND
4	DP9_M2C_P	-	-	N.C
5	DP9_M2C_N	-	-	N.C
6	GND	-	GND	GND
7	GND	-	GND	GND
8	DP8_M2C_P	-	-	N.C
9	DP8_M2C_N	-	-	N.C
10	GND	-	GND	GND
11	GND	-	GND	GND
12	DP7_M2C_P	O	EX_SINK_ML_LANE3_P	SINK MainLink LANE3 (Positive, expanded board)
13	DP7_M2C_N	O	EX_SINK_ML_LANE3_N	SINK MainLink LANE3 (Negative, expanded board)
14	GND	-	GND	GND
15	GND	-	GND	GND
16	DP6_M2C_P	O	EX_SINK_ML_LANE2_P	SINK MainLink LANE2 (Positive, expanded board)
17	DP6_M2C_N	O	EX_SINK_ML_LANE2_N	SINK MainLink LANE2 (Negative, expanded board)
18	GND	-	GND	GND
19	GND	-	GND	GND
20	GBTCLK1_M2C_P	O	CLK_OUT_P	DP159 CDR Clock (Positive)
21	GBTCLK1_M2C_N	O	CLK_OUT_N	DP159 CDR Clock (Negative)
22	GND	-	GND	GND
23	GND	-	GND	GND
24	DP9_C2M_P	-	-	N.C
25	DP9_C2M_N	-	-	N.C
26	GND	-	GND	GND
27	GND	-	GND	GND
28	DP8_C2M_P	-	-	N.C
29	DP8_C2M_N	-	-	N.C
30	GND	-	GND	GND
31	GND	-	GND	GND
32	DP7_C2M_P	I	EX_SOURCE_ML_LANE3_P	SOURCE MainLink LANE3 (Positive, expanded board)
33	DP7_C2M_N	I	EX_SOURCE_ML_LANE3_N	SOURCE MainLink LANE3 (Negative, expanded board)
34	GND	-	GND	GND
35	GND	-	GND	GND
36	DP6_C2M_P	I	EX_SOURCE_ML_LANE2_P	SOURCE MainLink LANE2 (Positive, expanded board)
37	DP6_C2M_N	I	EX_SOURCE_ML_LANE2_N	SOURCE MainLink LANE2 (Negative, expanded board)
38	GND	-	GND	GND
39	GND	-	GND	GND
40	RES0	-	-	N.C

C row in HPC pin assignment (CN4)				
#	FMC signal	I/O	Signal in schematic	Note
1	GND	-	GND	GND
2	DP0_C2M_P	I	SOURCE_ML_LANE0_P	SOURCE MainLink LANE0 (Positive)
3	DP0_C2M_N	I	SOURCE_ML_LANE0_N	SOURCE MainLink LANE0 (Negative)
4	GND	-	GND	GND
5	GND	-	GND	GND
6	DP0_M2C_P	O	SINK_ML_LANE0_P	SINK MainLink LANE0 (Positive)
7	DP0_M2C_N	O	SINK_ML_LANE0_N	SINK MainLink LANE0 (Negative)
8	GND	-	GND	GND
9	GND	-	GND	GND
10	LA06_P	I	SINK_HPD	SINK Hot Plug Detect signal
11	LA06_N	I	SINK_EN	SINK DP159 Enable signal
12	GND	-	GND	GND
13	GND	-	GND	GND
14	LA10_P	I/O	SINK_I2C_SCL	SINK DP159 I2C SCL signal
15	LA10_N	I/O	SINK_I2C_SDA	SINK DP159 I2C SDA signal
16	GND	-	GND	GND
17	GND	-	GND	GND
18	LA14_P	I/O	SINK_AUX_P	SINK bi-direction AUX signal(Positive)
19	LA14_N	I/O	SINK_AUX_N	SINK bi-direction AUX signal(Negative)
20	GND	-	GND	GND
21	GND	-	GND	GND
22	LA18_P_CC	O	SINK_AUX_RX	SINK single-end AUX, receiver signal
23	LA18_N_CC	I	SINK_AUX_TX	SINK single-end AUX, transfer signal
24	GND	-	GND	GND
25	GND	-	GND	GND
26	LA27_P	I	SINK_AUX_DE	SINK single-end AUX, data enable signal
27	LA27_N	I	EX_SINK_AUX_DE	SINK single-end AUX, data enable signal (expanded board)
28	GND	-	GND	GND
29	GND	-	GND	GND
30	SCL	-	2Kb_EEPROM_SCL	I2C SCL signal for 2Kbit EEPROM
31	SDA	-	2Kb_EEPROM_SDA	I2C SDA signal for 2Kbit EEPROM
32	GND	-	GND	GND
33	GND	-	GND	GND
34	GA0	-	2Kb_EEPROM_E0	Address setting of 2Kbit EEPROM
35	12P0V	-	+12V	12P0V
36	GND	-	GND	GND
37	12P0V	-	+12V	12P0V
38	GND	-	GND	GND
39	3P3V	-	+3.3V	3P3V
40	GND	-	GND	GND

D row in HPC pin assignment (CN4)				
#	FMC signal	I/O	Signal in schematic	Note
1	PG_C2M	-	-	N.C
2	GND	-	GND	GND
3	GND	-	GND	GND
4	GBTCLK0_M2C_P	O	GCLK0_P	PLL Clock output 0(Positive)
5	GBTCLK0_M2C_N	O	GCLK0_N	PLL Clock output 0(Negative)
6	GND	-	GND	GND
7	GND	-	GND	GND
8	LA01_P_CC	I	EX_SINK_HPDP	SINK Hot Plug Detect signal(expanded board)
9	LA01_N_CC	I	EX_SINK_EN	SINK DP159 Enable signal(expanded board)
10	GND	-	GND	GND
11	LA05_P	I/O	EX_SINK_I2C_SCL	SINK DP159 I2C SCL(expanded board)
12	LA05_N	I/O	EX_SINK_I2C_SDA	SINK DP159 I2C SDA(expanded board)
13	GND	-	GND	GND
14	LA09_P	I/O	EX_SINK_AUX_P	SINK bi-direction AUX signal (Positive, expanded board)
15	LA09_N	I/O	EX_SINK_AUX_N	SINK bi-direction AUX signal (Negative, expanded board)
16	GND	-	GND	GND
17	LA13_P	O	EX_SINK_AUX_RX	SINK single-end AUX, receiver signal (expanded board)
18	LA13_N	I	EX_SINK_AUX_TX	SINK single-end AUX, transfer signal (expanded board)
19	GND	-	GND	GND
20	LA17_P_CC	I	PLL_REFCLKIN_P	PLL reference clock input(Positive)
21	LA17_N_CC	I	PLL_REFCLKIN_N	PLL reference clock input(Negative)
22	GND	-	GND	GND
23	LA23_P	I/O	EDID_I2C_SCL	EDID ROM I2C SCL signal
24	LA23_N	I/O	EDID_I2C_SDA	EDID ROM I2C SDA signal
25	GND	-	GND	GND
26	LA26_P	I/O	HDCP_I2C_SCL	HDCP ROM I2C SCL signal
27	LA26_N	I/O	HDCP_I2C_SDA	HDCP ROM I2C SDA signal
28	GND	-	GND	GND
29	TCK	-	-	N.C
30	TDI	-	-	N.C
31	TDO	-	-	N.C
32	3P3VAUX	-	+3.3V_AUX	3P3VAUX
33	TMS	-	-	N.C
34	TRST_L	-	-	N.C
35	GA1	-	2Kb_EEPROM_E1	Address setting of 2Kbit EEPROM
36	3P3V	-	+3.3V	3P3V
37	GND	-	GND	GND
38	3P3V	-	+3.3V	3P3V
39	GND	-	GND	GND
40	3P3V	-	+3.3V	3P3V

E row in HPC pin assignment (CN4)				
#	FMC signal	I/O	Signal in schematic	Note
1	GND	-	GND	GND
2	HA01_P_CC	-	-	N.C
3	HA01_N_CC	-	-	N.C
4	GND	-	GND	GND
5	GND	-	GND	GND
6	HA05_P	-	-	N.C
7	HA05_N	-	-	N.C
8	GND	-	GND	GND
9	HA09_P	-	-	N.C
10	HA09_N	-	-	N.C
11	GND	-	GND	GND
12	HA13_P	-	-	N.C
13	HA13_N	-	-	N.C
14	GND	-	GND	GND
15	HA16_P	-	-	N.C
16	HA16_N	-	-	N.C
17	GND	-	GND	GND
18	HA20_P	-	-	N.C
19	HA20_N	-	-	N.C
20	GND	-	GND	GND
21	HB03_P	-	-	N.C
22	HB03_N	-	-	N.C
23	GND	-	GND	GND
24	HB05_P	-	-	N.C
25	HB05_N	-	-	N.C
26	GND	-	GND	GND
27	HB09_P	-	-	N.C
28	HB09_N	-	-	N.C
29	GND	-	GND	GND
30	HB13_P	-	-	N.C
31	HB13_N	-	-	N.C
32	GND	-	GND	GND
33	HB19_P	-	-	N.C
34	HB19_N	-	-	N.C
35	GND	-	GND	GND
36	HB21_P	-	-	N.C
37	HB21_N	-	-	N.C
38	GND	-	GND	GND
39	VADJ	-	FMC_VADJ	VADJ Power
40	GND	-	GND	GND

F row in HPC pin assignment (CN4)				
#	FMC signal	I/O	Signal in schematic	Note
1	PG_M2C	-	-	PG_M2C
2	GND	-	GND	GND
3	GND	-	GND	GND
4	HA00_P_CC	-	-	N.C
5	HA00_N_CC	-	-	N.C
6	GND	-	GND	GND
7	HA04_P	-	-	N.C
8	HA04_N	-	-	N.C
9	GND	-	GND	GND
10	HA08_P	-	-	N.C
11	HA08_N	-	-	N.C
12	GND	-	GND	GND
13	HA12_P	-	-	N.C
14	HA12_N	-	-	N.C
15	GND	-	GND	GND
16	HA15_P	-	-	N.C
17	HA15_N	-	-	N.C
18	GND	-	GND	GND
19	HA19_P	-	-	N.C
20	HA19_N	-	-	N.C
21	GND	-	GND	GND
22	HB02_P	-	-	N.C
23	HB02_N	-	-	N.C
24	GND	-	GND	GND
25	HB04_P	-	-	N.C
26	HB04_N	-	-	N.C
27	GND	-	GND	GND
28	HB08_P	-	-	N.C
29	HB08_N	-	-	N.C
30	GND	-	GND	GND
31	HB12_P	-	-	N.C
32	HB12_N	-	-	N.C
33	GND	-	GND	GND
34	HB16_P	-	-	N.C
35	HB16_N	-	-	N.C
36	GND	-	GND	GND
37	HB20_P	-	-	N.C
38	HB20_N	-	-	N.C
39	GND	-	GND	GND
40	VADJ	-	FMC_VADJ	VADJ Power

G row in HPC pin assignment (CN4)				
#	FMC signal	I/O	Signal in schematic	Note
1	GND	-	GND	GND
2	CLK1_M2C_P	O	CLK1_P	PLL Clock output2 (Positive)
3	CLK1_M2C_N	O	CLK1_N	PLL Clock output2 (Negative)
4	GND	-	GND	GND
5	GND	-	GND	GND
6	LA00_P_CC	I/O	SOURCE_DDC_SDA	Please fixed to High(1)
7	LA00_N_CC	I/O	SOURCE_DDC_SCL	Please fixed to High(1)
8	GND	-	GND	GND
9	LA03_P	O	SOURCE_HPD	SOURCE Hot Plug Detect signal
10	LA03_N	O	SOURCE_CAD	SOURCE Cable Adapter Detect signal
11	GND	-	GND	GND
12	LA08_P	I	SOURCE_RST	SOURCE DP130 reset signal(Active High)
13	LA08_N	I	SOURCE_EN	SOURCE DP130 Enable signal(Active High)
14	GND	-	GND	GND
15	LA12_P	I/O	SOURCE_I2C_SDA	SOURCE DP130 I2C SDA signal
16	LA12_N	I/O	SOURCE_I2C_SCL	SOURCE DP130 I2C SCL signal
17	GND	-	GND	GND
18	LA16_P	I/O	SOURCE_AUX_P	SOURCE bi-direction AUX signal(Positive)
19	LA16_N	I/O	SOURCE_AUX_N	SOURCE bi-direction AUX signal(Negative)
20	GND	-	GND	GND
21	LA20_P	O	SOURCE_AUX_RX	SOURCE single-end AUX, receiver signal
22	LA20_N	I	SOURCE_AUX_TX	SOURCE single-end AUX, transfer signal
23	GND	-	GND	GND
24	LA22_P	I	SOURCE_DDC_EN	Not used
25	LA22_N	I	SOURCE_AUX_DE	SOURCE single-end AUX, data enable
26	GND	-	GND	GND
27	LA25_P	I/O	STATUS_HLD	PLL Status: default is Read Back signal
28	LA25_N	I/O	STATUS_LD	PLL Status: default is Lock signal
29	GND	-	GND	GND
30	LA29_P	I/O	STATUS_CLK0	PLL Status: default is CLKIn select signal
31	LA29_N	I/O	STATUS_CLK1	PLL Status: default is CLKIn select signal
32	GND	-	GND	GND
33	LA31_P	O	-	N.C
34	LA31_N	O	-	N.C
35	GND	-	GND	GND
36	LA33_P	I	-	N.C
37	LA33_N	I	-	N.C
38	GND	-	GND	GND
39	VADJ	-	FMC_VADJ	VADJ power
40	GND	-	GND	GND

H row in HPC pin assignment (CN4)				
#	FMC signal	I/O	Signal in schematic	note
1	VREF_A_M2C	-		N.C
2	PRSNT_M2C_L	-	-	N.C
3	GND	-	GND	GND
4	CLK0_M2C_P	O	CLK0_P	PLL Clock output1 (Positive)
5	CLK0_M2C_N	O	CLK0_N	PLL Clock output1 (Negative)
6	GND	-	GND	GND
7	LA02_P	I/O	EX_SOURCE_DDC_SDA	Please fixed to High(1)
8	LA02_N	I/O	EX_SOURCE_DDC_SCL	Please fixed to High(1)
9	GND	-	GND	GND
10	LA04_P	O	EX_SOURCE_HPD	SOURCE Hot Plug detect signal (expanded board)
11	LA04_N	O	EX_SOURCE_CAD	SOURCE Cable Adapter Detect signal (expanded board)
12	GND	-	GND	GND
13	LA07_P	I	EX_SOURCE_RST	SOURCE DP130 reset signal (expanded board)
14	LA07_N	I	EX_SOURCE_EN	SOURCE DP130 enable signal (expanded board)
15	GND	-	GND	GND
16	LA11_P	I/O	EX_SOURCE_I2C_SDA	SOURCE DP130 I2C SDA (expanded board)
17	LA11_N	I/O	EX_SOURCE_I2C_SCL	SOURCE DP130 I2C SCL (expanded board)
18	GND	-	GND	GND
19	LA15_P	I/O	EX_SOURCE_AUX_P	SOURCE bi-direction AUX signal (Positive, extended board)
20	LA15_N	I/O	EX_SOURCE_AUX_N	SOURCE bi-direction AUX signal (Negative, extended board)
21	GND	-	GND	GND
22	LA19_P	O	EX_SOURCE_AUX_RX	SOURCE single-end AUX, receiver signal (extended board)
23	LA19_N	I	EX_SOURCE_AUX_TX	SOURCE single-end AUX, transfer signal (extended board)
24	GND	-	GND	GND
25	LA21_P	I	EX_SOURCE_DDC_EN	Not used
26	LA21_N	I	EX_SOURCE_AUX_DE	SOURCE single-end AUX, data enable (extended board)
27	GND	-	GND	GND
28	LA24_P	I/O	STATUS_CLK2	PLL Status: default is CLKin select signal
29	LA24_N	I	STATUS_DIR	Direction control of Status_X
30	GND	-	GND	GND
31	LA28_P	I	LE_WR	Microwire: Enable signal
32	LA28_N	I	CLK_WR	Microwire: Clock signal
33	GND	-	GND	GND
34	LA30_P	I	DATA_WR	Microwire: Data signal
35	LA30_N	-	-	N.C
36	GND	-	GND	GND
37	LA32_P	-	-	N.C
38	LA32_N	-	-	N.C
39	GND	-	GND	GND
40	VADJ	-	FMC_VADJ	VADJ Power

J row in HPC pin assignment (CN4)				
#	FMC signal	I/O	Signal in schematic	note
1	GND	-	GND	GND
2	CLK3_M2C_P	-	-	N.C
3	CLK3_M2C_N	-	-	N.C
4	GND	-	GND	GND
5	GND	-	GND	GND
6	HA03_P	-	-	N.C
7	HA03_N	-	-	N.C
8	GND	-	GND	GND
9	HA07_P	-	-	N.C
10	HA07_N	-	-	N.C
11	GND	-	GND	GND
12	HA11_P	-	-	N.C
13	HA11_N	-	-	N.C
14	GND	-	GND	GND
15	HA14_P	-	-	N.C
16	HA14_N	-	-	N.C
17	GND	-	GND	GND
18	HA18_P	-	-	N.C
19	HA18_N	-	-	N.C
20	GND	-	GND	GND
21	HA22_P	-	-	N.C
22	HA22_N	-	-	N.C
23	GND	-	GND	GND
24	HB01_P	-	-	N.C
25	HB01_N	-	-	N.C
26	GND	-	GND	GND
27	HB07_P	-	-	N.C
28	HB07_N	-	-	N.C
29	GND	-	GND	GND
30	HB11_P	-	-	N.C
31	HB11_N	-	-	N.C
32	GND	-	GND	GND
33	HB15_P	-	-	N.C
34	HB15_N	-	-	N.C
35	GND	-	GND	GND
36	HB18_P	-	-	N.C
37	HB18_N	-	-	N.C
38	GND	-	GND	GND
39	VIO_B_M2C	-	-	N.C
40	GND	-	GND	GND

K row in HPC pin assignment (CN4)				
#	FMC signal	I/O	Signal in schematic	note
1	VREF_B_M2C	-	-	N.C
2	GND	-	GND	GND
3	GND	-	GND	GND
4	CLK2_M2C_P	O	VCXO_OUT_P	PLL VCXO Output (Positive)
5	CLK2_M2C_N	O	VCXO_OUT_N	PLL VCXO Output (Negative)
6	GND	-	GND	GND
7	HA02_P	-	-	N.C
8	HA02_N	-	-	N.C
9	GND	-	GND	GND
10	HA06_P	-	-	N.C
11	HA06_N	-	-	N.C
12	GND	-	GND	GND
13	HA10_P	-	-	N.C
14	HA10_N	-	-	N.C
15	GND	-	GND	GND
16	HA17_P_CC	-	-	N.C
17	HA17_N_CC	-	-	N.C
18	GND	-	GND	GND
19	HA21_P	-	-	N.C
20	HA21_N	-	-	N.C
21	GND	-	GND	GND
22	HA23_P	-	-	N.C
23	HA23_N	-	-	N.C
24	GND	-	GND	GND
25	HB00_P_CC	-	-	N.C
26	HB00_N_CC	-	-	N.C
27	GND	-	GND	GND
28	HB06_P_CC	-	-	N.C
29	HB06_N_CC	-	-	N.C
30	GND	-	GND	GND
31	HB10_P	-	-	N.C
32	HB10_N	-	-	N.C
33	GND	-	GND	GND
34	HB14_P	-	-	N.C
35	HB14_N	-	-	N.C
36	GND	-	GND	GND
37	HB17_P_CC	-	-	N.C
38	HB17_N_CC	-	-	N.C
39	GND	-	GND	GND
40	VIO_B_M2C	-	-	N.C

4.10. FMC connector for expanded Board (CN3)

From next page, Table 4-8 CN3 Pin assign (For expanded Board) shows FMC pin assignment.

Signal direction is assigned as follows:

- “I”: The signal came from carrier board to TB-FMCH-DP3.
- “O”: The signal came from TB-FMCH-DP3 to carrier board.

Table 4-8 CN3 Pin assign (For expanded Board)

A row in HPC pin assignment (CN3)				
#	FMC signal	I/O	Signal in schematic	Note
1	GND	-	GND	GND
2	DP1_M2C_P	I	EX_SINK_ML_LANE1_P	SINK MainLink LANE1 (Positive, extending board)
3	DP1_M2C_N	I	EX_SINK_ML_LANE1_N	SINK MainLink LANE1 (Negative, extending board)
4	GND	-	GND	GND
5	GND	-	GND	GND
6	DP2_M2C_P	I	EX_SINK_ML_LANE2_P	SINK MainLink LANE2 (Positive, extending board)
7	DP2_M2C_N	I	EX_SINK_ML_LANE2_N	SINK MainLink LANE2 (Negative, extending board)
8	GND	-	GND	GND
9	GND	-	GND	GND
10	DP3_M2C_P	I	EX_SINK_ML_LANE3_P	SINK MainLink LANE3 (Positive, extending board)
11	DP3_M2C_N	I	EX_SINK_ML_LANE3_N	SINK MainLink LANE3 (Negative, extending board)
12	GND	-	GND	GND
13	GND	-	GND	GND
14	DP4_M2C_P	-	-	N.C
15	DP4_M2C_N	-	-	N.C
16	GND	-	GND	GND
17	GND	-	GND	GND
18	DP5_M2C_P	-	-	N.C
19	DP5_M2C_N	-	-	N.C
20	GND	-	GND	GND
21	GND	-	GND	GND
22	DP1_C2M_P	O	EX_SOURCE_ML_LANE1_P	SOURCE MainLink LANE1 (Positive, extending board)
23	DP1_C2M_N	O	EX_SOURCE_ML_LANE1_N	SOURCE MainLink LANE1 (Negative, extending board)
24	GND	-	GND	GND
25	GND	-	GND	GND
26	DP2_C2M_P	O	EX_SOURCE_ML_LANE2_P	SOURCE MainLink LANE2 (Positive, extending board)
27	DP2_C2M_N	O	EX_SOURCE_ML_LANE2_N	SOURCE MainLink LANE2 (Negative, extending board)
28	GND	-	GND	GND
29	GND	-	GND	GND
30	DP3_C2M_P	O	EX_SOURCE_ML_LANE3_P	SOURCE MainLink LANE3 (Positive, extending board)
31	DP3_C2M_N	O	EX_SOURCE_ML_LANE3_N	SOURCE MainLink LANE3 (Negative, extending board)
32	GND	-	GND	GND
33	GND	-	GND	GND
34	DP4_C2M_P	-	-	N.C
35	DP4_C2M_N	-	-	N.C
36	GND	-	GND	GND
37	GND	-	GND	GND
38	DP5_C2M_P	-	-	N.C
39	DP5_C2M_N	-	-	N.C
40	GND	-	GND	GND

B row in HPC pin assignment (CN3)				
#	FMC signal	I/O	Signal in schematic	Note
1	RES1	-	-	N.C
2	GND	-	GND	GND
3	GND	-	GND	GND
4	DP9_M2C_P	-	-	N.C
5	DP9_M2C_N	-	-	N.C
6	GND	-	GND	GND
7	GND	-	GND	GND
8	DP8_M2C_P	-	-	N.C
9	DP8_M2C_N	-	-	N.C
10	GND	-	GND	GND
11	GND	-	GND	GND
12	DP7_M2C_P	-	-	N.C
13	DP7_M2C_N	-	-	N.C
14	GND	-	GND	GND
15	GND	-	GND	GND
16	DP6_M2C_P	-	-	N.C
17	DP6_M2C_N	-	-	N.C
18	GND	-	GND	GND
19	GND	-	GND	GND
20	GBTCLK1_M2C_P	-	-	N.C
21	GBTCLK1_M2C_N	-	-	N.C
22	GND	-	GND	GND
23	GND	-	GND	GND
24	DP9_C2M_P	-	-	N.C
25	DP9_C2M_N	-	-	N.C
26	GND	-	GND	GND
27	GND	-	GND	GND
28	DP8_C2M_P	-	-	N.C
29	DP8_C2M_N	-	-	N.C
30	GND	-	GND	GND
31	GND	-	GND	GND
32	DP7_C2M_P	-	-	N.C
33	DP7_C2M_N	-	-	N.C
34	GND	-	GND	GND
35	GND	-	GND	GND
36	DP6_C2M_P	-	-	N.C
37	DP6_C2M_N	-	-	N.C
38	GND	-	GND	GND
39	GND	-	GND	GND
40	RES0	-	-	N.C

C row in HPC pin assignment (CN3)				
#	FMC signal	I/O	Signal in schematic	Note
1	GND	-	GND	GND
2	DP0_C2M_P	O	EX_SOURCE_ML_LANE0_P	SOURCE MainLink LANE0 (Positive, extending board)
3	DP0_C2M_N	O	EX_SOURCE_ML_LANE0_N	SOURCE MainLink LANE0 (Negative, extending board)
4	GND	-	GND	GND
5	GND	-	GND	GND
6	DP0_M2C_P	I	EX_SINK_ML_LANE0_P	SOURCE MainLink LANE3 (Positive, extending board)
7	DP0_M2C_N	I	EX_SINK_ML_LANE0_N	SOURCE MainLink LANE3 (Negative, extending board)
8	GND	-	GND	GND
9	GND	-	GND	GND
10	LA06_P	O	EX_SINK_HPD	SINK Hot Plug Detect signal (extended board)
11	LA06_N	O	EX_SINK_EN	SINK SP159 enable signal (extended board)
12	GND	-	GND	GND
13	GND	-	GND	GND
14	LA10_P	I/O	EX_SINK_I2C_SCL	SINK DP159 I2C SCL(expanded board)
15	LA10_N	I/O	EX_SINK_I2C_SDA	SINK DP159 I2C SDA(expanded board)
16	GND	-	GND	GND
17	GND	-	GND	GND
18	LA14_P	I/O	EX_SINK_AUX_P	SINK bi-direction AUX signal (Positive, expanded board)
19	LA14_N	I/O	EX_SINK_AUX_N	SINK bi-direction AUX signal (Negative, expanded board)
20	GND	-	GND	GND
21	GND	-	GND	GND
22	LA18_P_CC	I	EX_SINK_AUX_RX	SINK single-end AUX, receiver signal (expanded board)
23	LA18_N_CC	O	EX_SINK_AUX_TX	SINK single-end AUX, transfer signal (expanded board)
24	GND	-	GND	GND
25	GND	-	GND	GND
26	LA27_P	O	EX_SINK_AUX_DE	SINK single-end AUX, data enable signal (expanded board)
27	LA27_N	-	-	-
28	GND	-	GND	GND
29	GND	-	GND	GND
30	SCL	-	-	N.C
31	SDA	-	-	N.C
32	GND	-	GND	GND
33	GND	-	GND	GND
34	GA0	-	-	N.C
35	12P0V	-	+12V	12P0V
36	GND	-	GND	GND
37	12P0V	-	+12V	12P0V
38	GND	-	GND	GND
39	3P3V	-	+3.3V	3P3V
40	GND	-	GND	GND

D row in HPC pin assignment (CN3)				
#	FMC signal	I/O	Signal in schematic	Note
1	PG_C2M	-	-	N.C
2	GND	-	GND	GND
3	GND	-	GND	GND
4	GBTCLK0_M2C_P	-	-	N.C
5	GBTCLK0_M2C_N	-	-	N.C
6	GND	-	GND	GND
7	GND	-	GND	GND
8	LA01_P_CC	-	-	N.C
9	LA01_N_CC	-	-	N.C
10	GND	-	GND	GND
11	LA05_P	-	-	N.C
12	LA05_N	-	-	N.C
13	GND	-	GND	GND
14	LA09_P	-	-	N.C
15	LA09_N	-	-	N.C
16	GND	-	GND	GND
17	LA13_P	-	-	N.C
18	LA13_N	-	-	N.C
19	GND	-	GND	GND
20	LA17_P_CC	-	-	N.C
21	LA17_N_CC	-	-	N.C
22	GND	-	GND	GND
23	LA23_P	-	-	N.C
24	LA23_N	-	-	N.C
25	GND	-	GND	GND
26	LA26_P	-	-	N.C
27	LA26_N	-	-	N.C
28	GND	-	GND	GND
29	TCK	-	-	N.C
30	TDI	-	-	N.C
31	TDO	-	-	N.C
32	3P3VAUX	-	+3.3V_AUX	3P3VAUX
33	TMS	-	-	N.C
34	TRST_L	-	-	N.C
35	GA1	-	-	N.C
36	3P3V	-	+3.3V	3P3V
37	GND	-	GND	GND
38	3P3V	-	+3.3V	3P3V
39	GND	-	GND	GND
40	3P3V	-	+3.3V	3P3V

E row in HPC pin assignment (CN3)				
#	FMC signal	I/O	Signal in schematic	Note
1	GND	-	GND	GND
2	HA01_P_CC	-	-	N.C
3	HA01_N_CC	-	-	N.C
4	GND	-	GND	GND
5	GND	-	GND	GND
6	HA05_P	-	-	N.C
7	HA05_N	-	-	N.C
8	GND	-	GND	GND
9	HA09_P	-	-	N.C
10	HA09_N	-	-	N.C
11	GND	-	GND	GND
12	HA13_P	-	-	N.C
13	HA13_N	-	-	N.C
14	GND	-	GND	GND
15	HA16_P	-	-	N.C
16	HA16_N	-	-	N.C
17	GND	-	GND	GND
18	HA20_P	-	-	N.C
19	HA20_N	-	-	N.C
20	GND	-	GND	GND
21	HB03_P	-	-	N.C
22	HB03_N	-	-	N.C
23	GND	-	GND	GND
24	HB05_P	-	-	N.C
25	HB05_N	-	-	N.C
26	GND	-	GND	GND
27	HB09_P	-	-	N.C
28	HB09_N	-	-	N.C
29	GND	-	GND	GND
30	HB13_P	-	-	N.C
31	HB13_N	-	-	N.C
32	GND	-	GND	GND
33	HB19_P	-	-	N.C
34	HB19_N	-	-	N.C
35	GND	-	GND	GND
36	HB21_P	-	-	N.C
37	HB21_N	-	-	N.C
38	GND	-	GND	GND
39	VADJ	-	FMC_VADJ	VADJ Power
40	GND	-	GND	GND

F row in HPC pin assignment (CN3)				
#	FMC signal	I/O	Signal in schematic	Note
1	PG_M2C	-	-	PG_M2C
2	GND	-	GND	GND
3	GND	-	GND	GND
4	HA00_P_CC	-	-	N.C
5	HA00_N_CC	-	-	N.C
6	GND	-	GND	GND
7	HA04_P	-	-	N.C
8	HA04_N	-	-	N.C
9	GND	-	GND	GND
10	HA08_P	-	-	N.C
11	HA08_N	-	-	N.C
12	GND	-	GND	GND
13	HA12_P	-	-	N.C
14	HA12_N	-	-	N.C
15	GND	-	GND	GND
16	HA15_P	-	-	N.C
17	HA15_N	-	-	N.C
18	GND	-	GND	GND
19	HA19_P	-	-	N.C
20	HA19_N	-	-	N.C
21	GND	-	GND	GND
22	HB02_P	-	-	N.C
23	HB02_N	-	-	N.C
24	GND	-	GND-	GND
25	HB04_P	-	-	N.C
26	HB04_N	-	-	N.C
27	GND	-	GND	GND
28	HB08_P	-	-	N.C
29	HB08_N	-	-	N.C
30	GND	-	GND	GND
31	HB12_P	-	-	N.C
32	HB12_N	-	-	N.C
33	GND	-	GND	GND
34	HB16_P	-	-	N.C
35	HB16_N	-	-	N.C
36	GND	-	GND	GND
37	HB20_P	-	-	N.C
38	HB20_N	-	-	N.C
39	GND	-	GND	GND
40	VADJ	-	FMC_VADJ	VADJ Power

G row in HPC pin assignment (CN3)				
#	FMC signal	I/O	Signal in schematic	Note
1	GND	-	GND	GND
2	CLK0_M2C_P	-	-	N.C
3	CLK0_M2C_N	-	-	N.C
4	GND	-	GND	GND
5	GND	-	GND	GND
6	LA00_P_CC	I/O	EX_SOURCE_DDC_SDA	Please fixed to High(1)
7	LA00_N_CC	I/O	EX_SOURCE_DDC_SCL	Please fixed to High(1)
8	GND	-	-	GND
9	LA03_P	I	EX_SOURCE_HPD	SOURCE Hot Plug detect signal (expanded board)
10	LA03_N	I	EX_SOURCE_CAD	SOURCE Cable Adapter Detect signal (expanded board)
11	GND	-	-	GND
12	LA08_P	O	EX_SOURCE_RST	SOURCE DP130 reset signal (expanded board)
13	LA08_N	O	EX_SOURCE_EN	SOURCE DP130 enable signal (expanded board)
14	GND	-	-	GND
15	LA12_P	I/O	EX_SOURCE_I2C_SDA	SOURCE DP130 I2C SDA (expanded board)
16	LA12_N	I/O	EX_SOURCE_I2C_SCL	SOURCE DP130 I2C SCL (expanded board)
17	GND	-	-	GND
18	LA16_P	I/O	EX_SOURCE_AUX_P	SOURCE bi-direction AUX signal (Positive, extended board)
19	LA16_N	I/O	EX_SOURCE_AUX_N	SOURCE bi-direction AUX signal (Negative, extended board)
20	GND	-	-	GND
21	LA20_P	I	EX_SOURCE_AUX_RX	SOURCE single-end AUX, receiver signal (extended board)
22	LA20_N	O	EX_SOURCE_AUX_TX	SOURCE single-end AUX, transfer signal (extended board)
23	GND	-	-	GND
24	LA22_P	O	EX_SOURCE_DDC_EN	Not used
25	LA22_N	O	EX_SOURCE_AUX_DE	SOURCE single-end AUX, data enable (extended board)
26	GND	-	GND	GND
27	LA25_P	-	-	N.C
28	LA25_N	-	-	N.C
29	GND	-	GND	GND
30	LA29_P	-	-	N.C
31	LA29_N	-	-	N.C
32	GND	-	GND	GND
33	LA31_P	-	-	N.C
34	LA31_N	-	-	N.C
35	GND	-	GND	GND
36	LA33_P	-	-	N.C
37	LA33_N	-	-	N.C
38	GND	-	GND	GND
39	VADJ	-	FMC_VADJ	VADJ power
40	GND	-	GND	GND

H row in HPC pin assignment (CN3)				
#	FMC signal	I/O	Signal in schematic	Note
1	VREF_A_M2C	-	-	N.C
2	PRSNT_M2C_L	-	-	N.C
3	GND	-	-	GND
4	CLK0_M2C_P	-	-	N.C
5	CLK0_M2C_N	-	-	N.C
6	GND	-	GND	GND
7	LA02_P	-	-	N.C
8	LA02_N	-	-	N.C
9	GND	-	GND	GND
10	LA04_P	-	-	N.C
11	LA04_N	-	-	N.C
12	GND	-	GND	GND
13	LA07_P	-	-	N.C
14	LA07_N	-	-	N.C
15	GND	-	GND	GND
16	LA11_P	-	-	N.C
17	LA11_N	-	-	N.C
18	GND	-	GND	GND
19	LA15_P	-	-	N.C
20	LA15_N	-	-	N.C
21	GND	-	GND	GND
22	LA19_P	-	-	N.C
23	LA19_N	-	-	N.C
24	GND	-	GND	GND
25	LA21_P	-	-	N.C
26	LA21_N	-	-	N.C
27	GND	-	GND	GND
28	LA24_P	-	-	N.C
29	LA24_N	-	-	N.C
30	GND	-	GND	GND
31	LA28_P	-	-	N.C
32	LA28_N	-	-	N.C
33	GND	-	GND	GND
34	LA30_P	-	-	N.C
35	LA30_N	-	-	N.C
36	GND	-	GND	GND
37	LA32_P	-	-	N.C
38	LA32_N	-	-	N.C
39	GND	-	GND	GND
40	VADJ	-	FMC_VADJ	VADJ power

J row in HPC pin assignment (CN3)				
#	FMC signal	I/O	Signal in schematic	Note
1	GND	-	GND	GND
2	CLK3_M2C_P	-	-	N.C
3	CLK3_M2C_N	-	-	N.C
4	GND	-	GND	GND
5	GND	-	GND	GND
6	HA03_P	-	-	N.C
7	HA03_N	-	-	N.C
8	GND	-	GND	GND
9	HA07_P	-	-	N.C
10	HA07_N	-	-	N.C
11	GND	-	GND	GND
12	HA11_P	-	-	N.C
13	HA11_N	-	-	N.C
14	GND	-	GND	GND
15	HA14_P	-	-	N.C
16	HA14_N	-	-	N.C
17	GND	-	GND	GND
18	HA18_P	-	-	N.C
19	HA18_N	-	-	N.C
20	GND	-	GND	GND
21	HA22_P	-	-	N.C
22	HA22_N	-	-	N.C
23	GND	-	GND	GND
24	HB01_P	-	-	N.C
25	HB01_N	-	-	N.C
26	GND	-	GND	GND
27	HB07_P	-	-	N.C
28	HB07_N	-	-	N.C
29	GND	-	GND	GND
30	HB11_P	-	-	N.C
31	HB11_N	-	-	N.C
32	GND	-	GND	GND
33	HB15_P	-	-	N.C
34	HB15_N	-	-	N.C
35	GND	-	GND	GND
36	HB18_P	-	-	N.C
37	HB18_N	-	-	N.C
38	GND	-	GND	GND
39	VIO_B_M2C	-	-	VIO_B_M2C
40	GND	-	GND	GND

K row in HPC pin assignment (CN3)				
#	FMC signal	I/O	Signal in schematic	Note
1	VREF_B_M2C	-	-	N.C
2	GND	-	GND	GND
3	GND	-	GND	GND
4	CLK2_M2C_P	-	-	N.C
5	CLK2_M2C_N	-	-	N.C
6	GND	-	GND	GND
7	HA02_P	-	-	N.C
8	HA02_N	-	-	N.C
9	GND	-	GND	GND
10	HA06_P	-	-	N.C
11	HA06_N	-	-	N.C
12	GND	-	GND	GND
13	HA10_P	-	-	N.C
14	HA10_N	-	-	N.C
15	GND	-	GND	GND
16	HA17_P_CC	-	-	N.C
17	HA17_N_CC	-	-	N.C
18	GND	-	GND	GND
19	HA21_P	-	-	N.C
20	HA21_N	-	-	N.C
21	GND	-	GND	GND
22	HA23_P	-	-	N.C
23	HA23_N	-	-	N.C
24	GND	-	GND	GND
25	HB00_P_CC	-	-	N.C
26	HB00_N_CC	-	-	N.C
27	GND	-	GND	GND
28	HB06_P_CC	-	-	N.C
29	HB06_N_CC	-	-	N.C
30	GND	-	GND	GND
31	HB10_P	-	-	N.C
32	HB10_N	-	-	N.C
33	GND	-	GND	GND
34	HB14_P	-	-	N.C
35	HB14_N	-	-	N.C
36	GND	-	GND	GND
37	HB17_P_CC	-	-	N.C
38	HB17_N_CC	-	-	N.C
39	GND	-	GND	GND
40	VIO_B_M2C	-	-	N.C

**TOKYO ELECTRON DEVICE**

Inrevium Company

URL: <http://solutions.inrevium.com/>
<http://solutions.inrevium.com/jp>

E-mail: psd-support@teldevice.co.jp

HEAD Quarter: Yokohama East Square, 1-4 Kinko-cho, Kanagawa-ku, Yokohama City,
Kanagawa, Japan 221-0056

TEL: +81-45-443-4016 FAX: +81-45-443-4058