Memory FRAM

64K (8K × 8) Bit SPI

MB85RS64VY

■ **DESCRIPTION**

MB85RS64VY is a FRAM (Ferroelectric Random Access Memory) chip in a configuration of 8,192 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.
MB85RS64VY adopts the Serial Peripheral Interface (SPI).
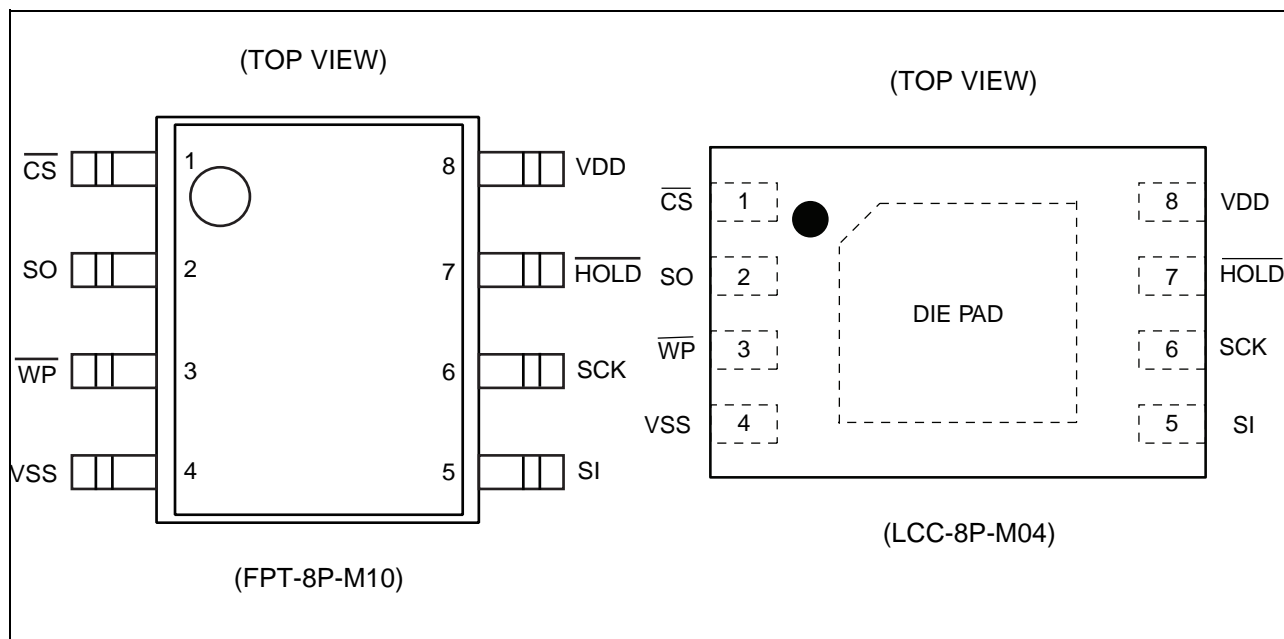The MB85RS64VY is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85RS64VY can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E²PROM.
As MB85RS64VY does not need any waiting time in writing process, the write cycle time of MB85RS64VY is much shorter than that of Flash memories or E²PROM.

■ **FEATURES**

- Bit configuration   : 8,192 words × 8 bits
- Serial Peripheral Interface   : SPI (Serial Peripheral Interface)
     Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency   : 25 MHz (Max,@2.7V to 4.5V), 33MHz(Max,@4.5V to 5.5V)
- High endurance   : 10^{13} times / byte
- Data retention   : 30 years (+85 °C),

     10.9 years (+105 °C)

      3.3 years (+125 °C) or more

     Under evaluation for more than 3.3 years(+125 °C)
- Operating power supply voltage : 2.7V to 5.5V
- Low power consumption   : Operating power supply current
     1.8 mA (Max@25 MHz),2.3 mA (Max@33MHz)
     Standby current 30 μA (Max)
     Sleep current 12 μA (Max)
- Operation ambient temperature range : − 40 °C to +125 °C
- Package   : 8-pin plastic SOP (FPT-8P-M10)
   : 8-pin plastic SON (LCC-8P-M04)
   RoHS compliant

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■ PIN ASSIGNMENT

(TOP VIEW)

$\overline{CS}$ 1
SO 2
$\overline{WP}$ 3
VSS 4
8 VDD
7 $\overline{HOLD}$
6 SCK
5 SI

(FPT-8P-M10)

(TOP VIEW)

$\overline{CS}$ 1
SO 2
$\overline{WP}$ 3
VSS 4
DIE PAD
8 VDD
7 $\overline{HOLD}$
6 SCK
5 SI

(LCC-8P-M04)

■ PIN FUNCTIONAL DESCRIPTIONS

| Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is "L" level, device is in select (active) status. $\overline{CS}$ has to be "L" level before inputting op-code.
3	$\overline{WP}$	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with $\overline{WP}$ and WPEN. See "■ WRITING PROTECT" for detail.
7	$\overline{HOLD}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. See "■ HOLD OPERATION" for detail.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin
DIE PAD	—	It is allowed for the DIE PAD on the bottom of the SON8 package to be floating (no connection to anything) or to be connected to VSS.

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■ BLOCK DIAGRAM
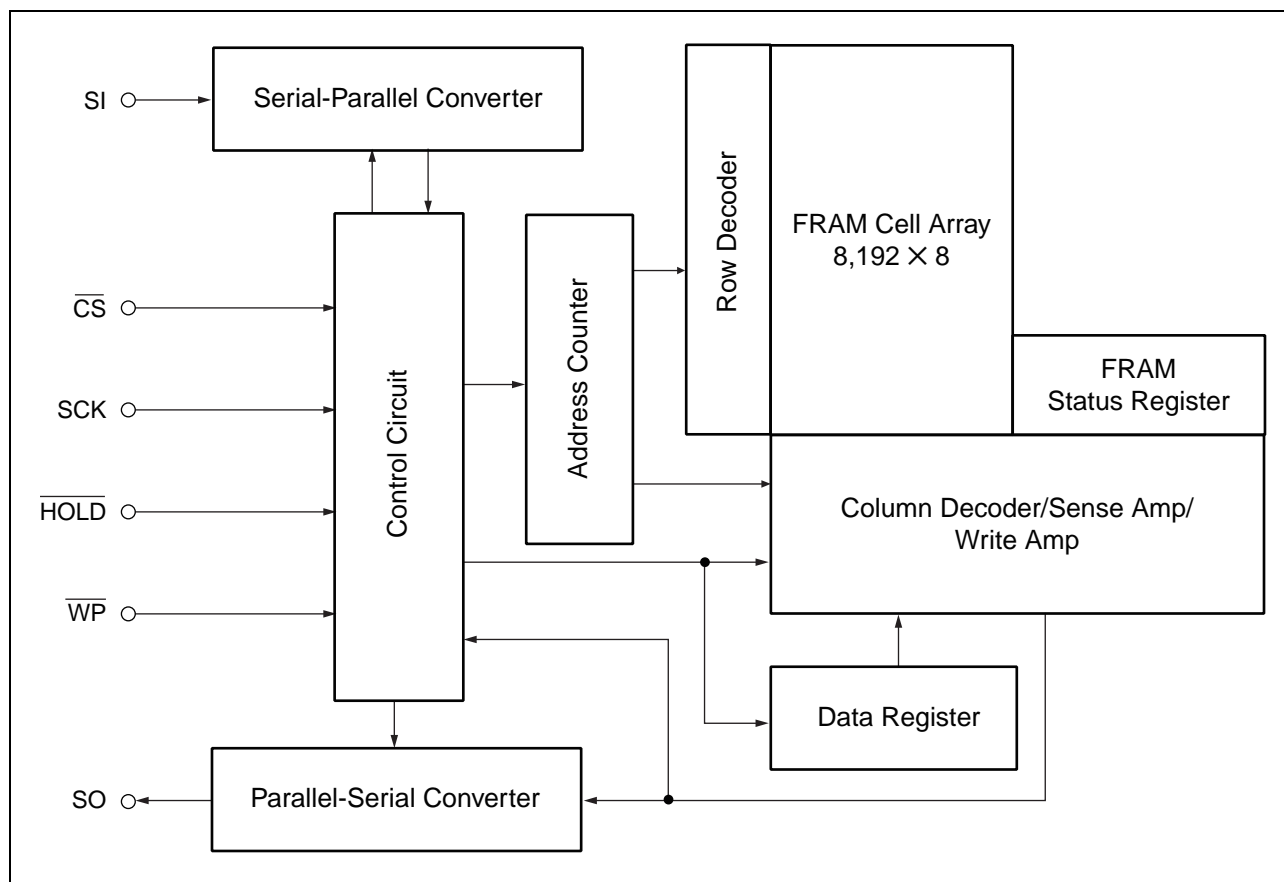
■ SPI MODE

MB85RS64VY corresponds to the SPI mode 0 (CPOL=0, CPHA=0), and SPI mode 3 (CPOL=1, CPHA=1).

SPI Mode 0
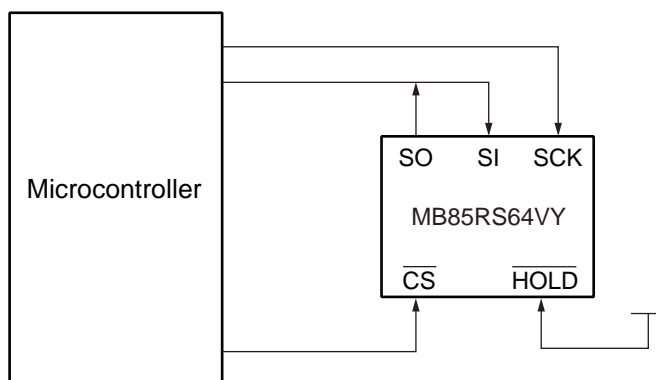
SPI Mode 3

FUJITSU
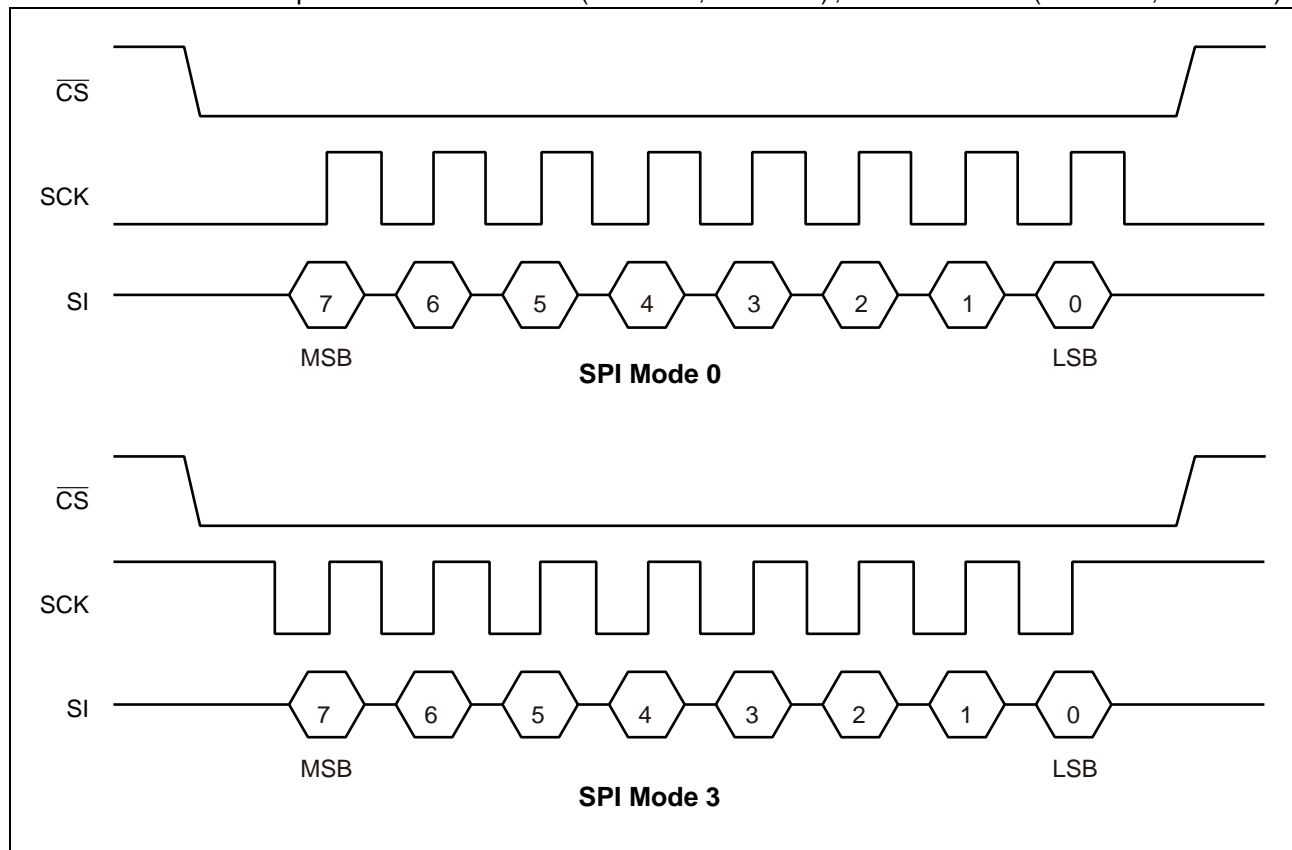
■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS64VY works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.

MOSI : Master Out Slave In
MISO : Master In Slave Out
SS   : Slave Select
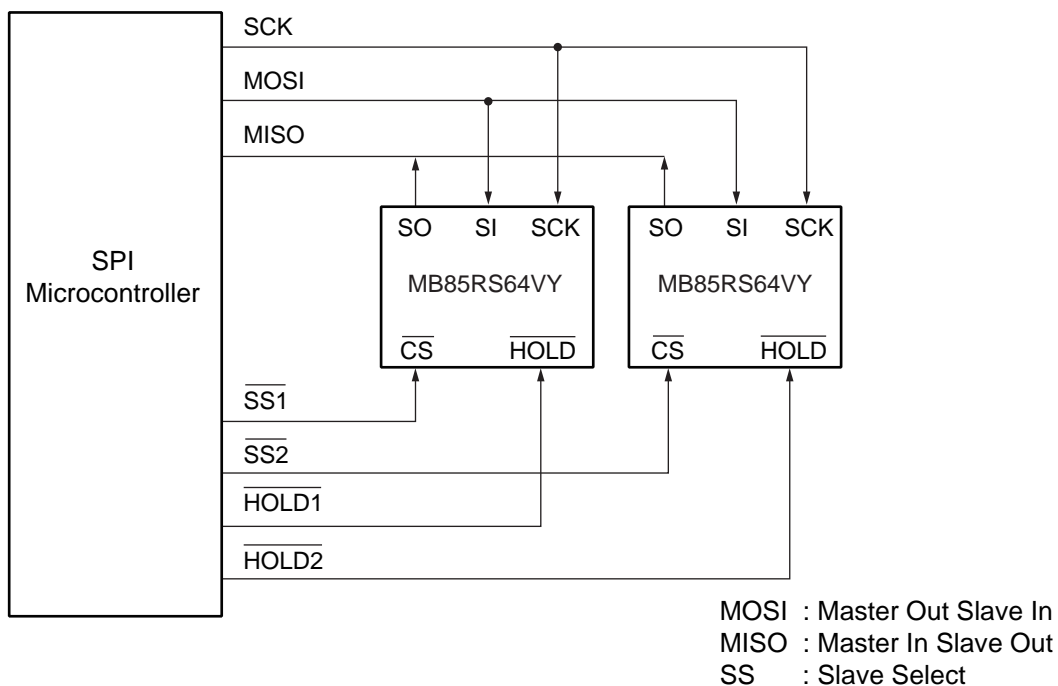
System Configuration with SPI Port

System Configuration without SPI Port

■ STATUS REGISTER

| Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FRAM). WPEN protects writing to a status register (refer to "■ WRITING PROTECT") relating with WP input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to "■ BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. 　　After power ON. 　　After WRDI command recognition. The following rising edges do not reset WEL. 　　The rising edge of CS after WRSR command recognition. 　　The rising edge of CS after WRITE command recognition.
0	0	This is a bit fixed to "0".

■ OP-CODE

MB85RS64VY accepts 8 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If CS is risen while inputting op-code, the command are not performed.

| Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110$_B$
WRDI	Reset Write Enable Latch	0000 0100$_B$
RDSR	Read Status Register	0000 0101$_B$
WRSR	Write Status Register	0000 0001$_B$
READ	Read Memory Code	0000 0011$_B$
WRITE	Write Memory Code	0000 0010$_B$
RDID	Read Device ID	1001 1111$_B$
SLEEP	Sleep Mode	1011 1001$_B$
RFU	Reserved for future use	1100 0011$_B$
		1100 0110$_B$
		1100 1110$_B$
		1100 1111$_B$

■ COMMAND

• WREN

The WREN command sets WEL (Write Enable Latch) bit to 1. WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) .
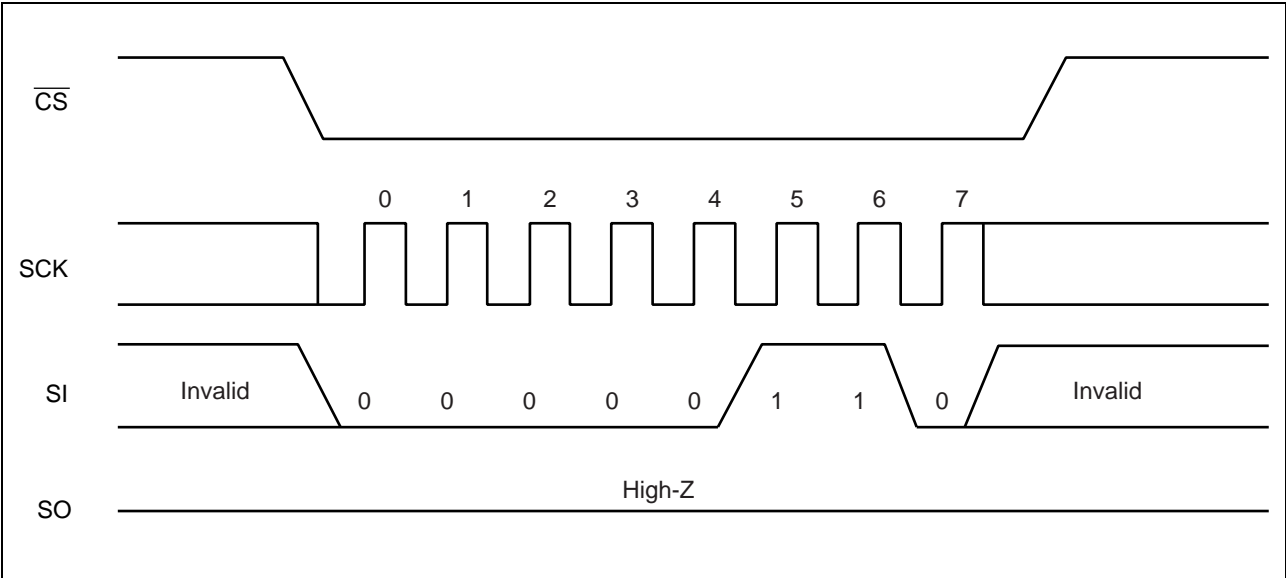

• WRDI

The WRDI command resets WEL (Write Enable Latch) bit to 0. Writing operation (WRSR command and WRITE command) are not performed when WEL is reset.
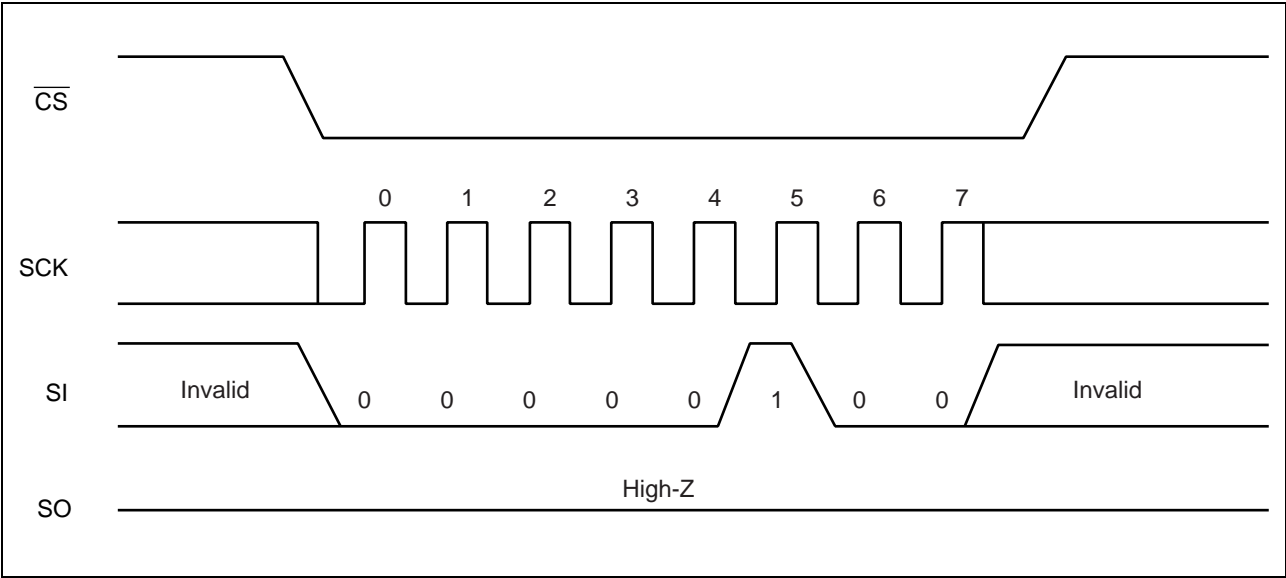
- **RDSR**

    The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of $\overline{CS}$.
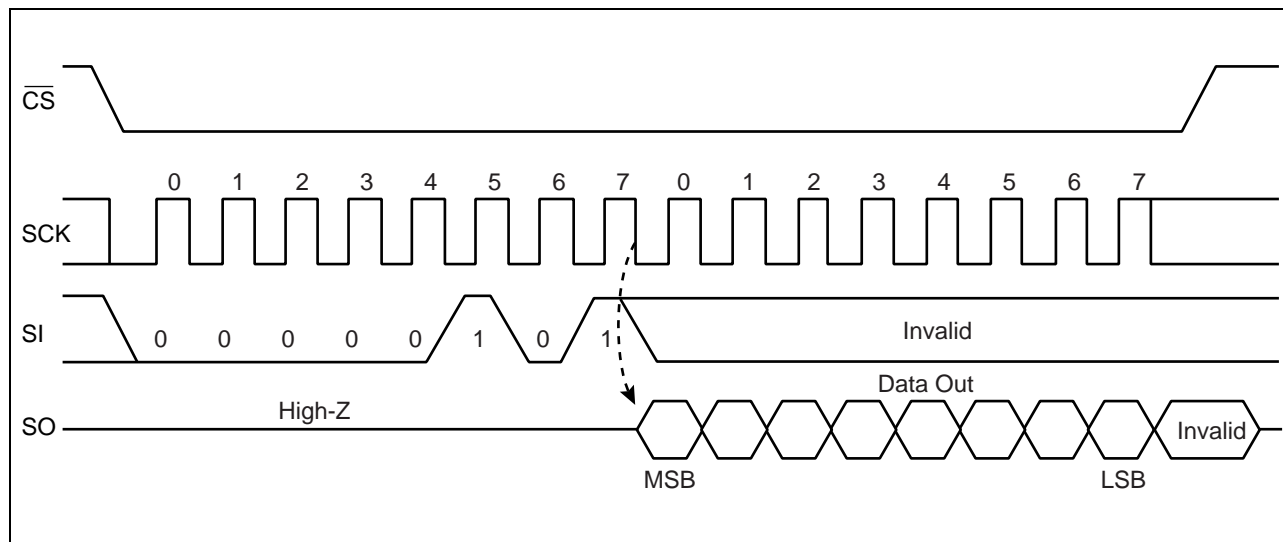
- **WRSR**

    The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored. $\overline{WP}$ signal level shall be fixed before performing WRSR command, and do not change the $\overline{WP}$ signal level until the end of command sequence.
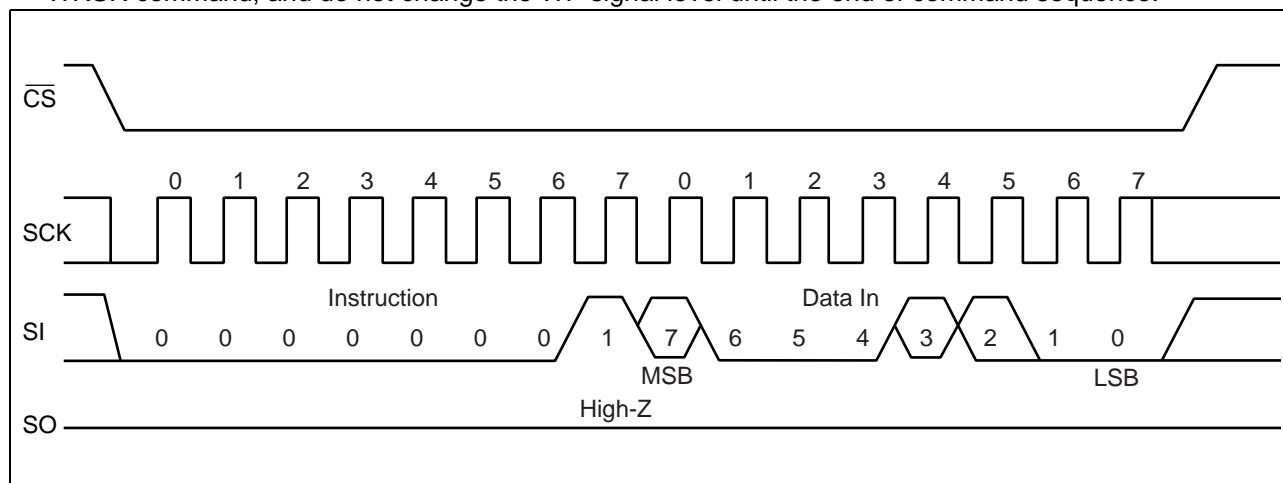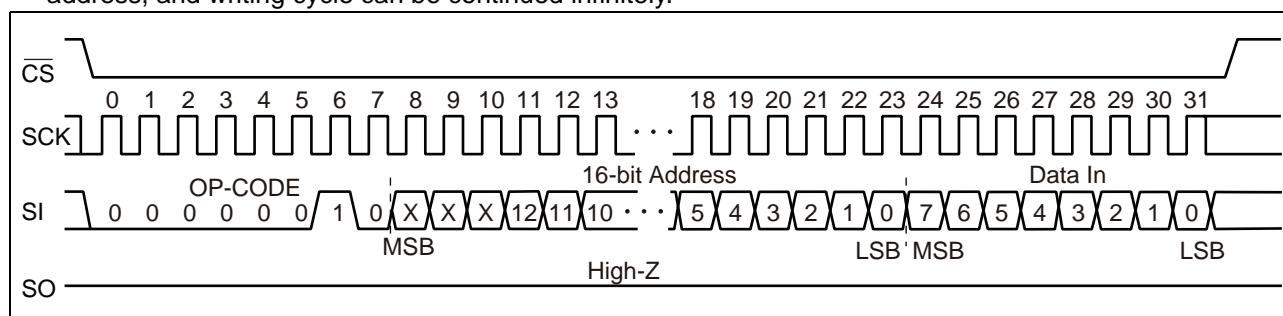
- **READ**

    The READ command reads FRAM memory cell array data. Arbitrary 16 bits address and op-code of READ are input to SI. The upper three address bits are invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.
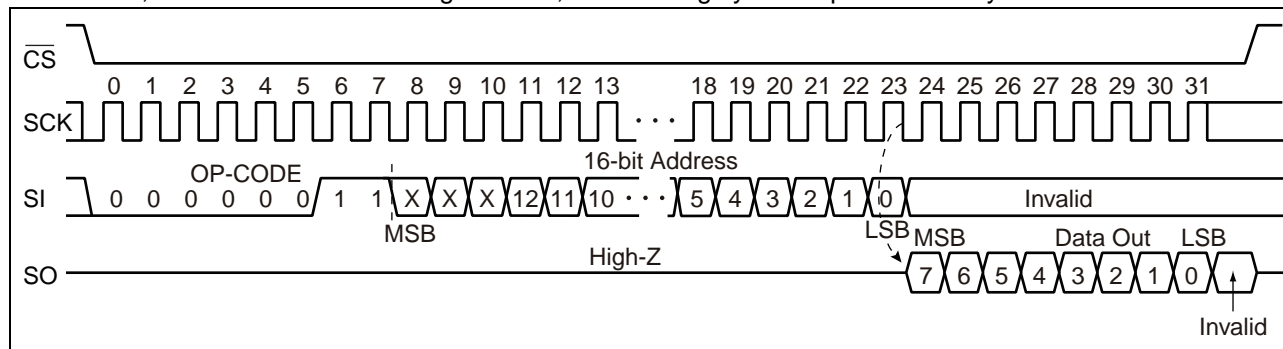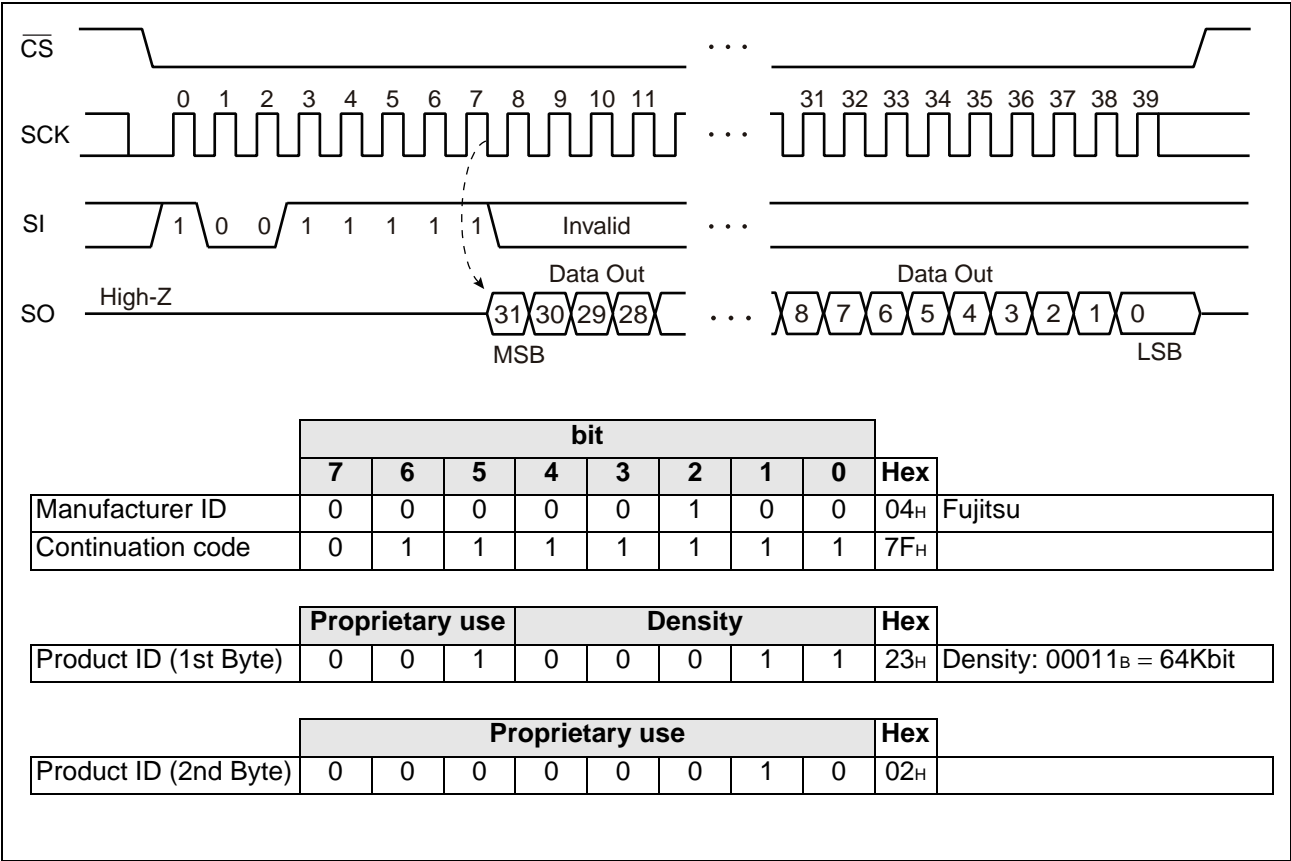

- **WRITE**

    The WRITE command writes data to FRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The upper three address bits are invalid. When 8 bits of writing data is input, data is written to FRAM memory cell array. Risen $\overline{CS}$ will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely.

- **RDID**

  The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, 32-bit Device ID is output by continuously sending SCK clock, and SO holds the output state of the last bit until CS is risen.


bit									Hex	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**			
Manufacturer ID	0	0	0	0	0	1	0	0	04$_H$	Fujitsu
Continuation code	0	1	1	1	1	1	1	1	7F$_H$	

	Proprietary use			Density					Hex	
Product ID (1st Byte)	0	0	1	0	0	0	1	1	23$_H$	Density: 00011$_B$ = 64Kbit

	Proprietary use								Hex	
Product ID (2nd Byte)	0	0	0	0	0	0	1	0	02$_H$	

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• **SLEEP**

The SLEEP command shifts the LSI to a low power mode called "SLEEP mode". The transition to the SLEEP mode is carried out at the rising edge of $\overline{CS}$ after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of $\overline{CS}$ after operation code in the SLEEP command, this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are logically ignored and SO changes to a High-Z state.

When inputs other than $\overline{CS}$ are not fixed to VCC or VDD, in some case a shoot-through current may flow.

Sleep Mode Entry
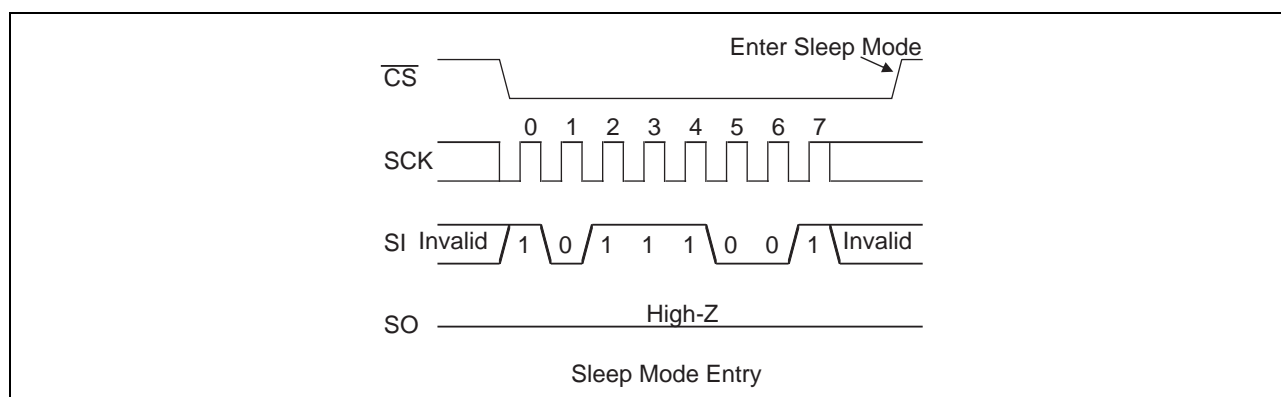
Returning to an normal operation from the SLEEP mode is carried out after t_{REC} (Max 400 μs) time from the falling edge of $\overline{CS}$ (see the figure below). It is possible to return $\overline{CS}$ to H level before t_{REC} time. However, it is prohibited to bring down $\overline{CS}$ to L level again during t_{REC} period.

Sleep Mode Exit
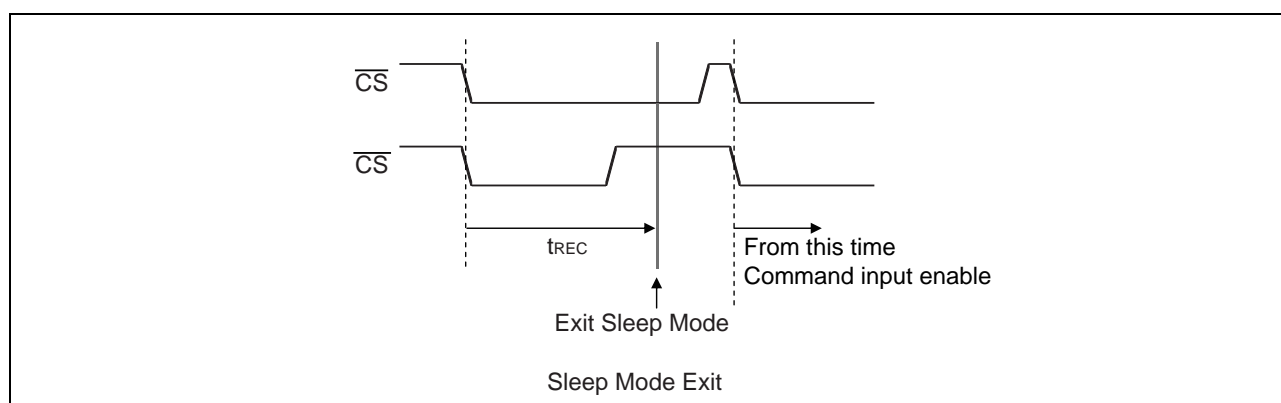
■ **BLOCK PROTECT**

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

| BP1	BP0	Protected Block
0	0	None
0	1	1800$_H$ to 1FFF$_H$ (upper 1/4)
1	0	1000$_H$ to 1FFF$_H$ (upper 1/2)
1	1	0000$_H$ to 1FFF$_H$ (all)

■ **WRITING PROTECT**

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, $\overline{WP}$ as shown in the table.

WEL	WPEN	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ **HOLD OPERATION**

Hold status is retained without aborting a command if $\overline{HOLD}$ is "L" level while $\overline{CS}$ is "L" level. The timing for starting and ending hold status depends on the SCK to be "H" level or "L" level when a $\overline{HOLD}$ pin input is transited to the hold condition as shown in the diagram below. In case the $\overline{HOLD}$ pin transited to "L" level when SCK is "L" level, return the $\overline{HOLD}$ pin to "H" level at SCK being "L" level. In the same manner, in case the $\overline{HOLD}$ pin transited to "L" level when SCK is "H" level, return the $\overline{HOLD}$ pin to "H" level at SCK being "H" level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If $\overline{CS}$ is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.
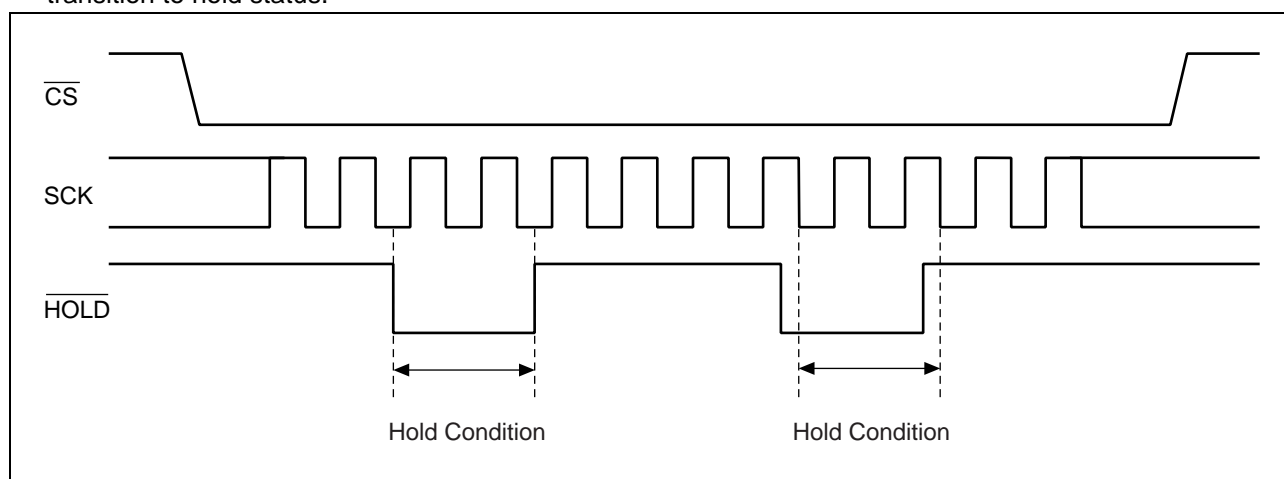
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 6.0	V
Input voltage*	V_{IN}	− 0.5	$V_{DD} + 0.5(\leq 6.0)$	V
Output voltage*	V_{OUT}	− 0.5	$V_{DD} + 0.5(\leq 6.0)$	V
Operation ambient temperature	T_A	− 40	+ 125	°C
Storage temperature	Tstg	− 55	+ 150	°C

*: These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	V_{DD}	2.7	—	5.5	V
Operation ambient temperature*2	T_A	− 40	—	+ 125	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Input leakage current[*1]	$|I_{LI}|$	$\overline{WP}$, $\overline{HOLD}$, SCK, $\overline{CS}$ SI $= 0$ V to V_{DD}	25 °C	—	—	1	μA
			125 °C	—	—	2	
Output leakage current[*2]	$|I_{LO}|$	SO $= 0$ V to V_{DD}	25 °C	—	—	1	μA
			125 °C	—	—	2	
Operating power supply current[*3]	I_{DD}	SCK $= 33$MHz		—	1.9	2.3	mA
		SCK $= 25$MHz		—	1.5	1.8	
Standby current	I_{SB}	$SCK = SI = \overline{CS} =$ $\overline{WP} = \overline{HOLD} = V_{DD}$		—	13	30	μA
Sleep current	I_{ZZ}	$\overline{CS} = V_{DD}$ All other inputs V_{SS} or V_{DD}		—	5	12	μA
Input high voltage	V_{IH}	$V_{DD} = 2.7$ V to 5.5 V		$V_{DD} \times 0.7$	—	$V_{DD} + 0.3$	V
Input low voltage	V_{IL}	$V_{DD} = 2.7$ V to 5.5 V		-0.3	—	$V_{DD} \times 0.3$	V
Output high voltage	V_{OH}	$I_{OH} = -2$ mA		$V_{DD} - 0.5$	—	V_{DD}	V
Output low voltage	V_{OL}	$I_{OL} = 2$ mA		—	—	0.4	V

*1 : Applicable pin : $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$, SCK, SI

*2 : Applicable pin : SO

*3 : Input voltage magnitude : VDD − 0.2 V or VSS

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2. AC Characteristics

Parameter	Symbol	Value (V_{DD}= 2.7 V to 4.5 V)		Value (V_{DD}= 4.5 V to 5.5 V)		Unit
		Min	Max	Min	Max	
SCK clock frequency	f_{CK}	0	25	0	33	MHz
Clock high time	t_{CH}	15	—	13	—	ns
Clock low time	t_{CL}	15	—	13	—	ns
Chip select set up time	t_{CSU}	10	—	10	—	ns
Chip select hold time	t_{CSH}	10	—	10	—	ns
Output disable time	t_{OD}	—	16	—	16	ns
Output data valid time	t_{ODV}	—	18	—	13	ns
Output hold time	t_{OH}	0	—	0	—	ns
Deselect time	t_D	40	—	40	—	ns
Data in rising time	t_R	—	50	—	50	ns
Data falling time	t_F	—	50	—	50	ns
Data set up time	t_{SU}	5	—	5	—	ns
Data hold time	t_H	5	—	5	—	ns
$\overline{HOLD}$ set uptime	t_{HS}	10	—	10	—	ns
$\overline{HOLD}$ hold time	t_{HH}	10	—	10	—	ns
$\overline{HOLD}$ output floating time	t_{HZ}	—	20	—	20	ns
$\overline{HOLD}$ output active time	t_{LZ}	—	20	—	20	ns
SLEEP recovery time	t_{REC}	—	400	—	400	μs

AC Test Condition

Power supply voltage	: 2.7 V to 5.5 V Operation
Operation ambient temperature	: $-40\,°C$ to $+125\,°C$
Input voltage magnitude	: $V_{DD} \times 0.7 \le V_{IH} \le V_{DD}$
	$0 \le V_{IL} \le V_{DD} \times 0.3$
Input rising time	: 5 ns
Input falling time	: 5 ns
Input judge level	: $V_{DD}/2$
Output judge level	: $V_{DD}/2$

AC Load Equivalent Circuit

VDD

1.2 kΩ

Output

30 pF   0.95 kΩ
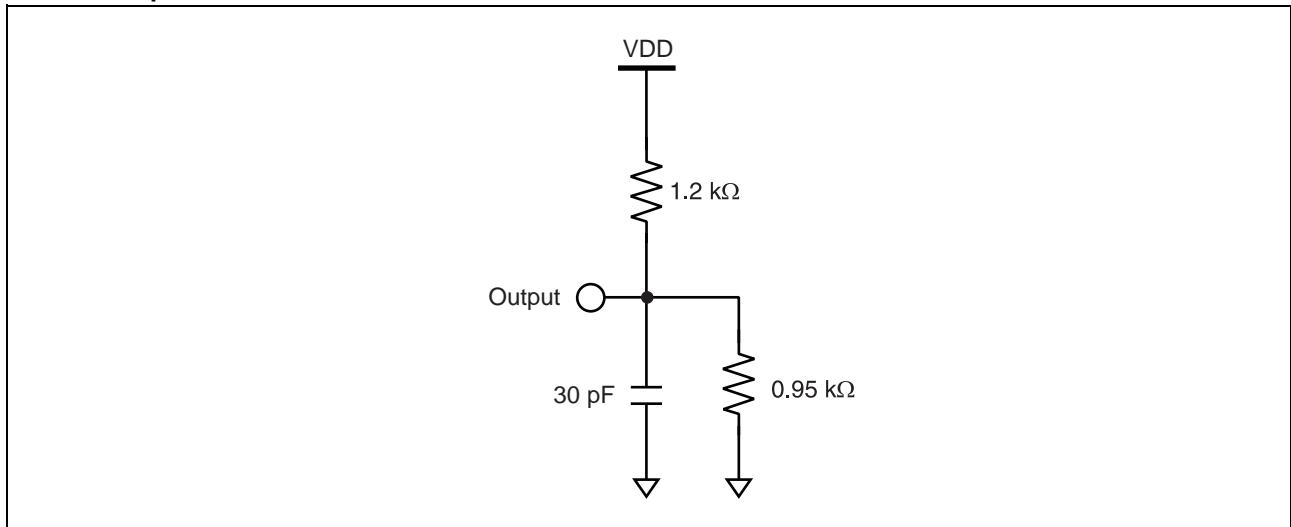
3. Pin Capacitance

Parameter	Symbol	Condition	Value		Unit
			Min	**Max**	
Output capacitance	C_O	$V_{DD} = 5.0$ V, $V_{IN} = V_{OUT} = 0$ V to V_{DD}, f = 1 MHz, $T_A = +25$ °C	—	8	pF
Input capacitance	C_I		—	6	pF

■ TIMING DIAGRAM

• **Serial Data Timing**

• **Hold Timing**

MB85RS64VY
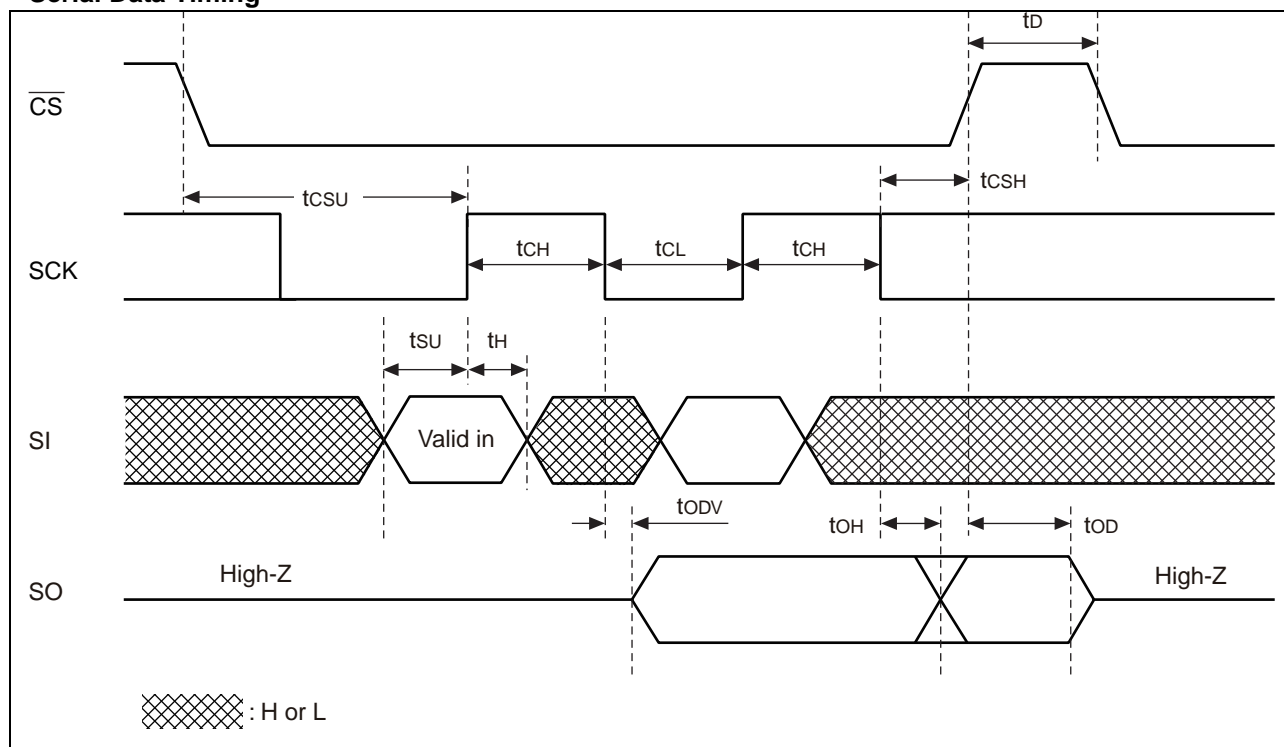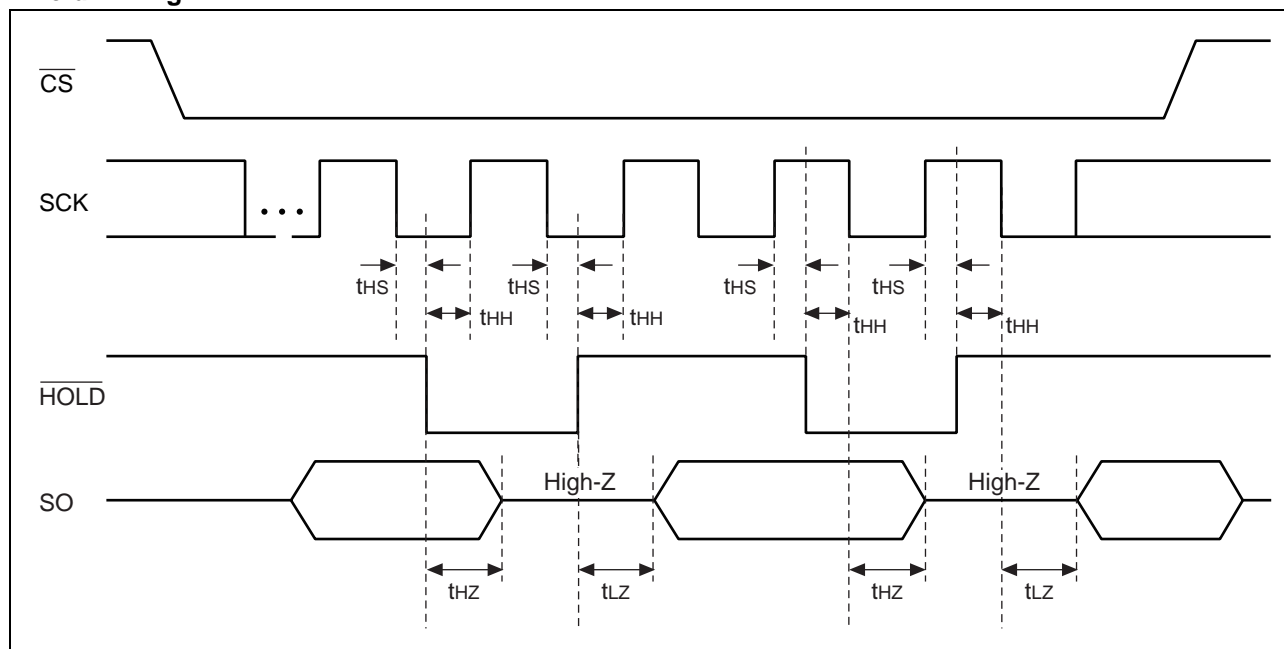
■ POWER ON/OFF SEQUENCE
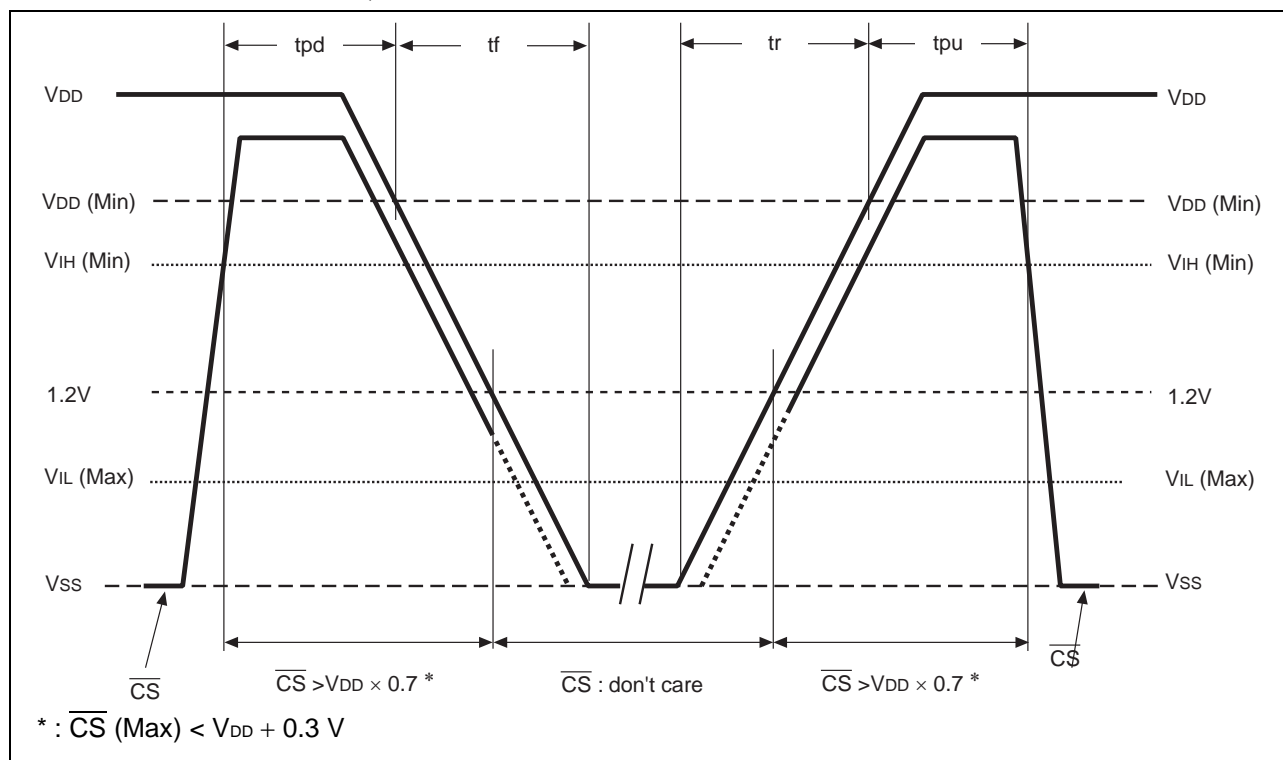
Parameter	Symbol	Value		Unit
		Min	Max	
$\overline{CS}$ level hold time at power OFF	tpd	400	—	ns
$\overline{CS}$ level hold time at power ON	tpu	250	—	µs
Power supply rising time	tr	0.05	—	ms/V
Power supply falling time	tf	0.1	—	ms/V

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Read/Write Endurance[1]	10^{13}	—	Times/byte	Operation Ambient Temperature $T_A = +125\ °C$
Data Retention[2]	3.3 or more[3]	—	Years	Operation Ambient Temperature $T_A = +125\ °C$
	10.9	—		Operation Ambient Temperature $T_A = +105\ °C$
	30	—		Operation Ambient Temperature $T_A = +85\ °C$

[1] : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

[2]: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

[3]: Under evaluation for more than 3.3 year(+125 °C).

■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

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■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RS64VYPNF-G-BCE1 MB85RS64VYPNF-G-BCERE1 MB85RS64VYPN-G-AMEWE1	≥ |2000 V|
ESD MM (Machine Model) JESD22-A115 compliant		≥ |200 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		≥ |1000 V|
Latch-Up JESD78 (I-test) compliant		≥ |125 mA|

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

■ Current status on Contained Restricted Substances

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.
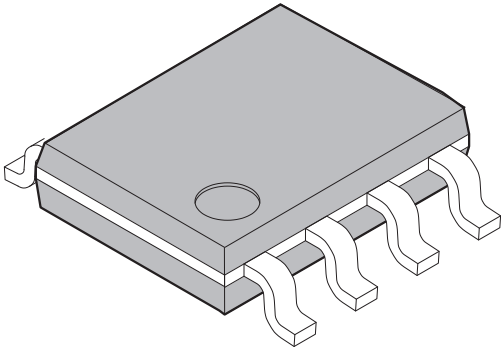
■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RS64VYPNF-G-BCE1	8-pin plastic SOP (FPT-8P-M10)	Tube	— *
MB85RS64VYPNF-G-BCERE1	8-pin plastic SOP (FPT-8P-M10)	Embossed Carrier tape	1500
MB85RS64VYPN-G-AMEWE1	8-pin plastic SON (LCC-8P-M04)	Embossed Carrier tape	1500

* : Please contact our sales office about minimum shipping quantity.
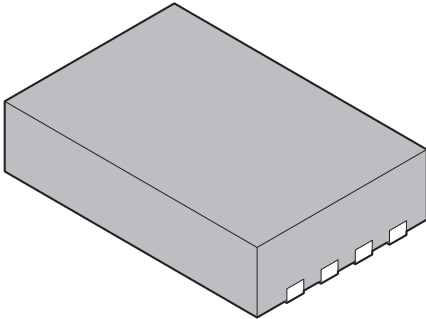
■ PACKAGE DIMENSION

8-pin plastic SOP		
Lead pitch	1.27 mm
Package width × package length	3.9 mm×4.89 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting heigth	1.73 mm MAX

(FPT-8P-M10)

8-pin plastic SOP
（FPT-8P-M10）

Note 1) *1: These dimensions do not include resin protrution.
Note 2) *2: These dimensions do not include resin protrution.

8pin   5pin
0.12MAX
0.17MAX
3.81～3.99*2
5.84～6.20
4×R0.05
1pin   4pin
1.27(Typ)   0.41～0.43

"F"

5.30MAX
4.80～4.98*1
1.5(Typ)
1.55～1.73

0.10 MIN
0.406～0.889
0.21～0.23

Details of "F" part

Dimenssions in mm

(Continued)

8-pin plastic SON	Lead pitch	0.5 mm
	Package width × package length	2.0 mm × 3.0 mm
	Sealing method	Plastic mold
	Mounting height	0.75 mm MAX
(LCC-8P-M04)		

8-pin plastic SON
(LCC-8P-M04)

2.00±0.07
(.079±.003)

3.00±0.07
(.118±.003)

INDEX AREA

1.6±0.10
(.063±.004)

0.40±0.07
(.016±.003)

1.40±0.10
(.055±.004)

1PIN CORNER
(C0.30(C.012))

0.50(.020)
TYP

0.25±0.05
(.010±.002)

0.70±0.05
(.028±.002)

0.15(.006)

0.05(.002) MAX

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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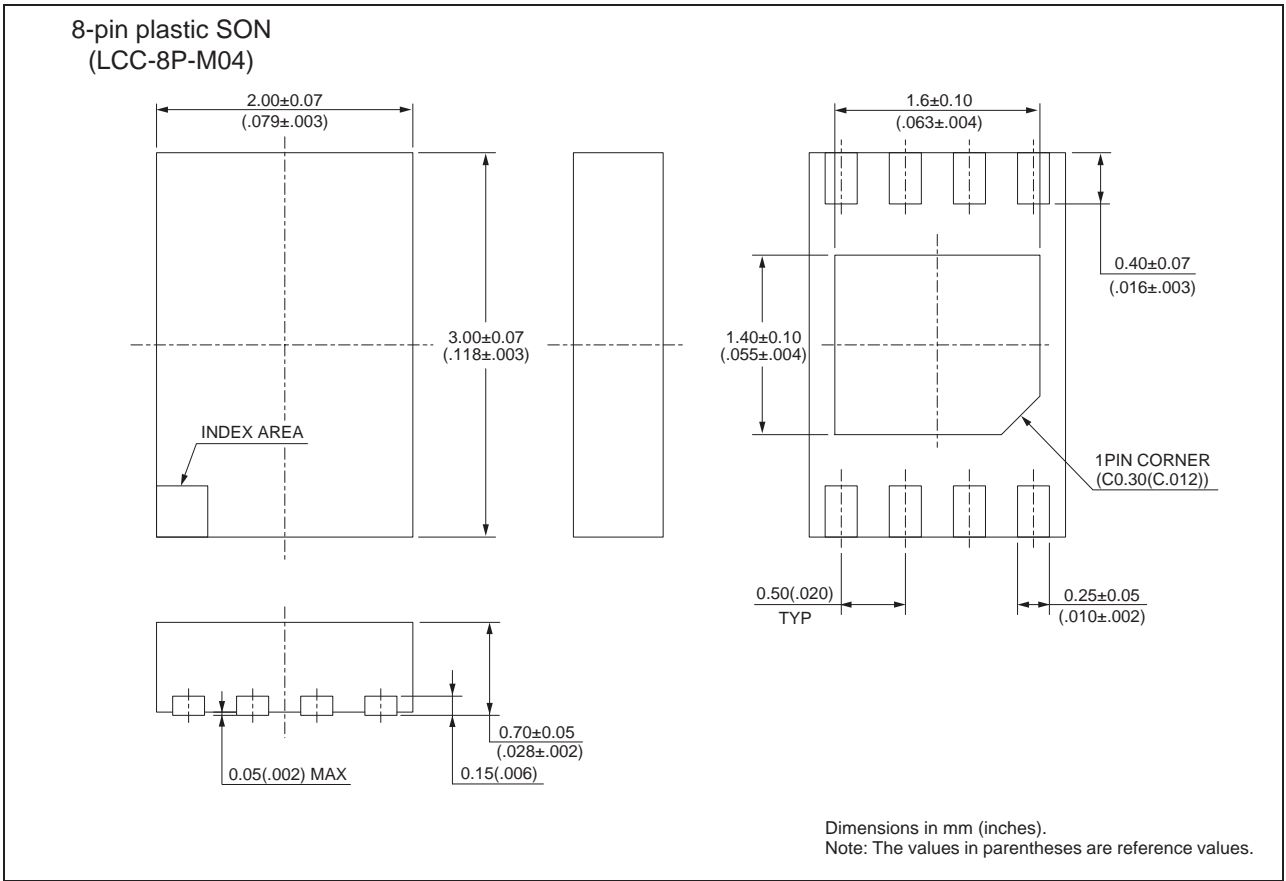
■ **MARKING (Example)**

[MB85RS64VYPNF-G-BCE1]
[MB85RS64VYPNF-G-BCERE1]
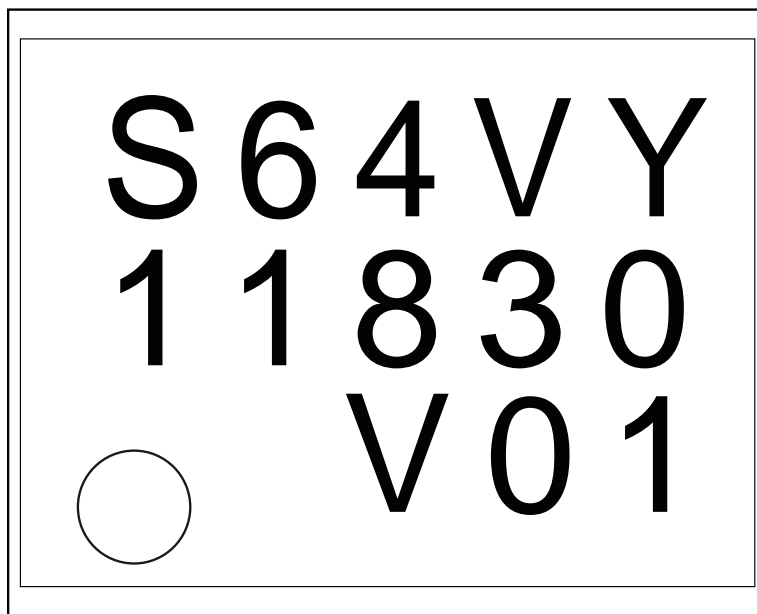
S 6 4 V Y
1 1 8 3 0
V 0 1

[FPT-8P-M10]

S64VY: Product Name
11830: 1(CS code) + 1830 (Year and Week code)
V01: V(Factory code) + 01(Trace code)

[MB85RS64VYPN-G-AMEWE1]
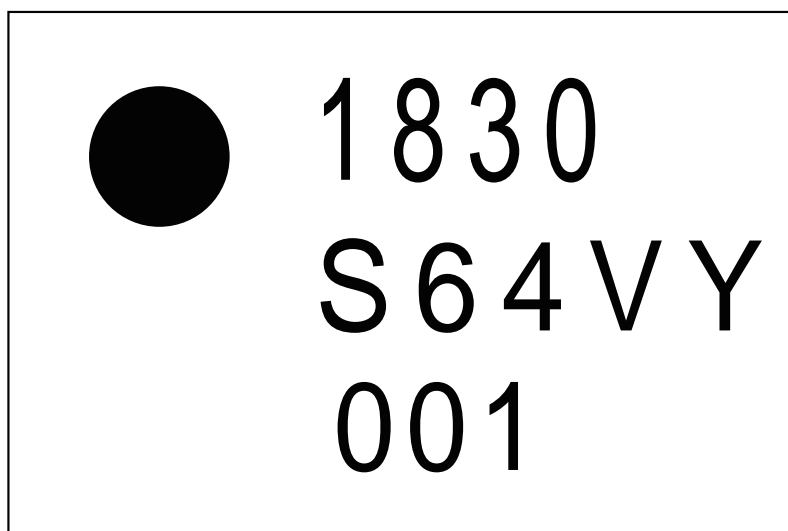
1 8 3 0
S 6 4 V Y
0 0 1

[LCC-8P-M04]

1830: Year and Week code
S64VY: Product Name
001: 0(Factory code) + 01(Trace code)

MB85RS64VY

■ PACKING INFORMATION
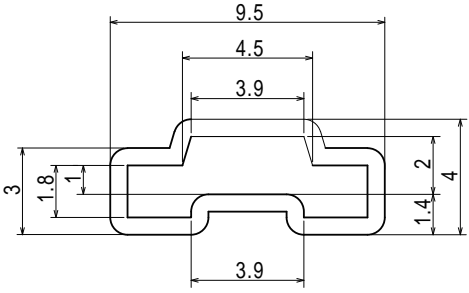
1. Tube

1.1 Tube Dimensions
• Tube/stopper shape

Tube

Transparent polyethylene terephthalate
(treated to antistatic)

Stopper
(treated to antistatic)

Tube length: 500 mm
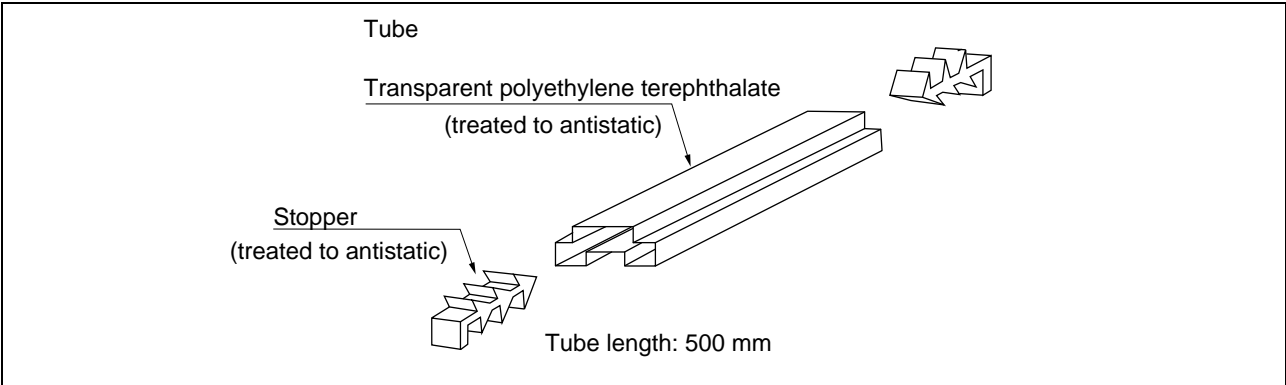
• **Tube cross-sections** and Maximum quantity

Package form	Package code	Maximum quantity		
		pcs/tube	pcs/inner box	pcs/outer box
SOP, 8, plastic (2)	FPT-8P-M10	85	4250	17000

9.5
4.5
3.9
3
1.8
1
2
4
1.4
3.9
t = 0.6
Transparent polyethylene terephthalate

(Dimensions in mm)

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1.2 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

```
XXXXXXXXXXXXXX        (Customer part number or FJ part number)
                                    [G] (Pb)              ◄──── C-3 Label
(3N)1 XXXXXXXXXXXXXX XXX        (LEAD FREE mark)
|||||||||||||||||||||||||||       (Part number and quantity)
                                    QC  PASS
(3N)2 XXXXXXXXXX XXXXXX
|||||||||||||||||||||||||||       (FJ control number)
        XXX  pcs          (Quantity)
XXXXXXXXXXXXXX          (Customer part number or FJ part number)
|||||||||||||||||||||||||||       (Customer part number or FJ part number
                                           bar code)
XXXX/XX/XX (Packed years/month/day)     ASSEMBLED IN xxxx
XXXXXXXXXXXXXX  (Customer part number or FJ part number)    ◄──── Perforated line
(FJ control number bar code)                                ◄──── Supplemental Label
        XX/XX               XXXX-XXX   XXX
||||||||||||       (Package count)      XXXX-XXX   XXX
   XXXXXXXXXX  (FJ control number )   (Lot Number and quantity)
XXXXXXXXXXXXXX  (Comment)
```

1.3 Dimensions for Containers

(1) Dimensions for inner box
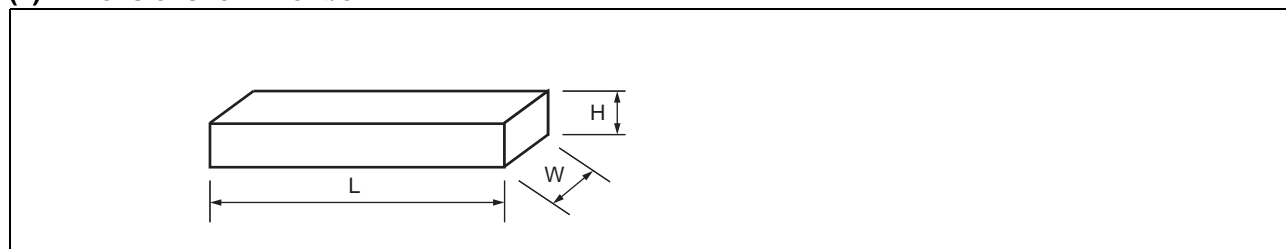
L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box
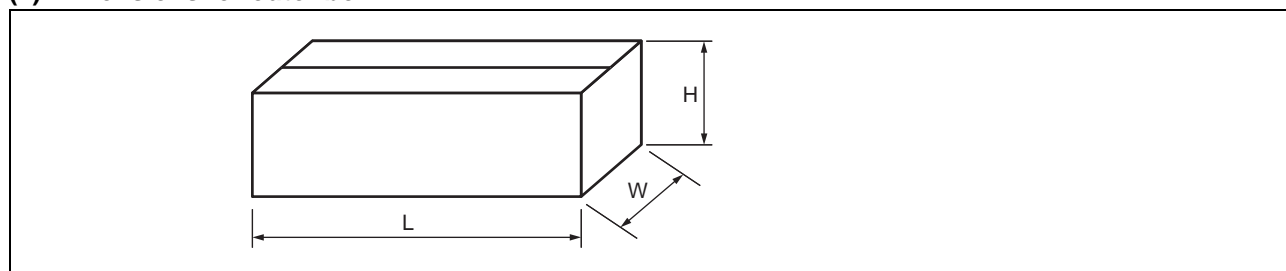
L	W	H
549	277	180

(Dimensions in mm)

2. Emboss Tape
2.1 FPT-8P-M10

2.1.1Tape Dimensions

PKG code	Maximum storage capacity		
	pcs/reel	pcs/inner box	pcs/uter boxo
FPT-8P-M10	1500	1500	9000

SEC.B-B

SEC.A-A

(Dimensions in mm)

Material : Conductive polystyrene
Heat proof temperature : No heat resistance.
　　　　　　　　　　　Package should not be baked
　　　　　　　　　　　by using tape and reel.

MB85RS64VY

2.1.2IC orientation

• ER type

Index mark

(User Direction of Feed)   (Feed side)   (User Direction of Feed)

2.1.3Reel dimensions

Reel cutout dimensions

A

B

C

W1

W2
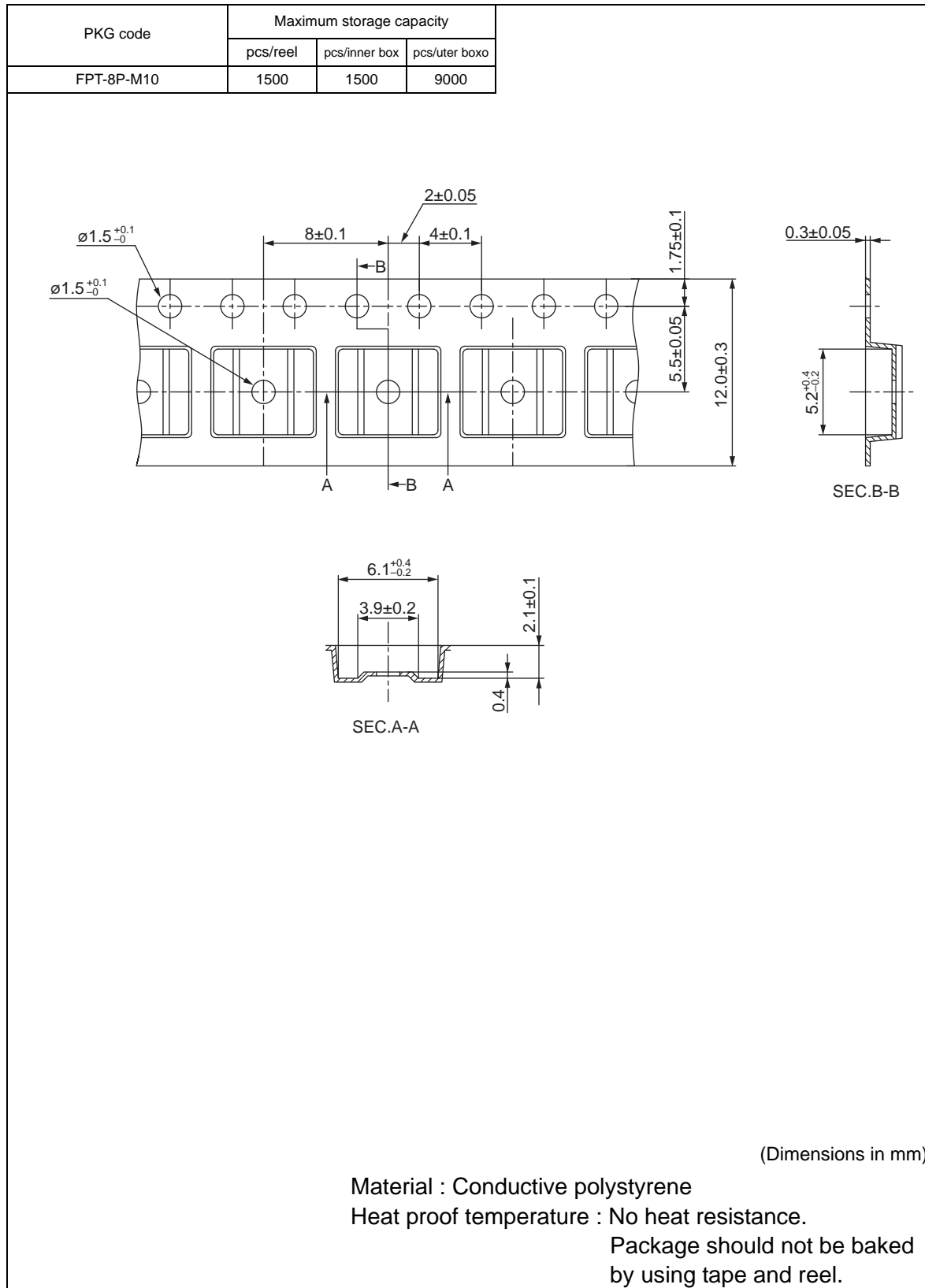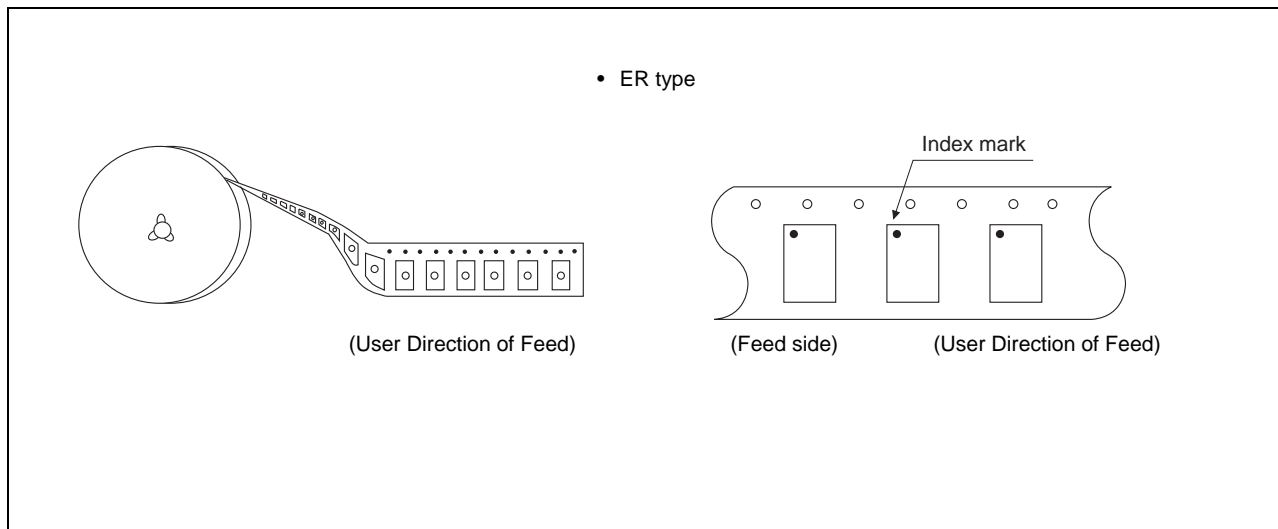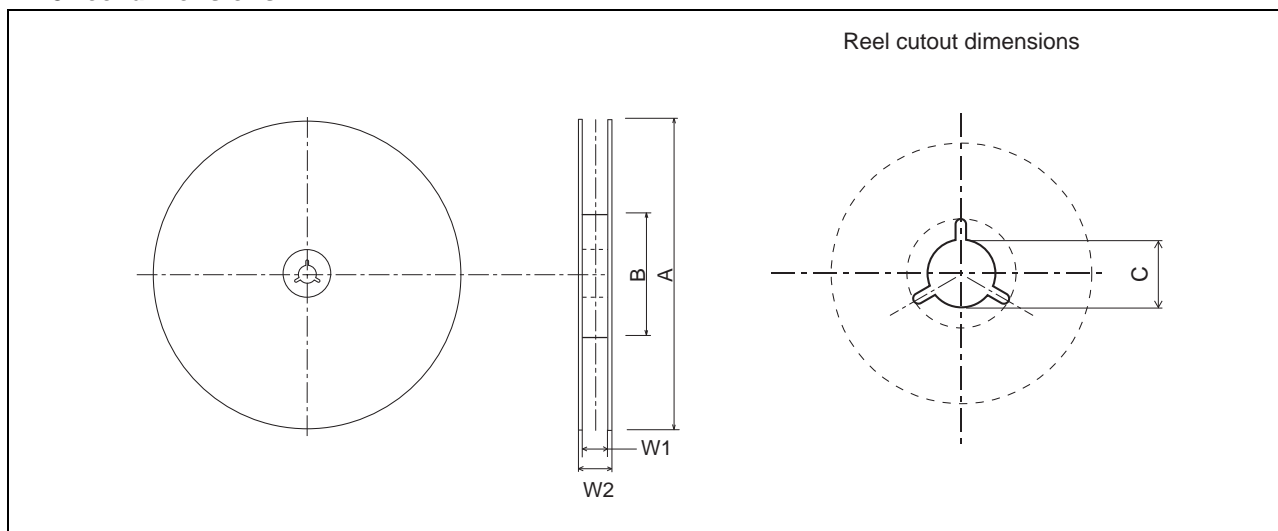
Dimensions in mm

Tape width	A	B	C	W1	W2
12	254±2	100±1	13±0.2	13.5±1.0	17.5±1.0

2.2 LCC-8P-M04

FUJITSU

2.2.1 Tape Dimensions

PKG code	Maximum storage capacity		
	pcs/reel	pcs/inner box	pcs/uter boxo
FPT-8P-M10	1500	1500	9000

SEC.B-B

SEC.A-A

(Dimensions in mm)

Material : Conductive polystyrene
Heat proof temperature : No heat resistance.
Package should not be baked
by using tape and reel.

2.2.2IC orientation

• EW type

Index mark

(User Direction of Feed)   (Feed side)   (User Direction of Feed)

2.2.3Reel dimensions

Reel cutout dimensions

B

A

W1

W2

C
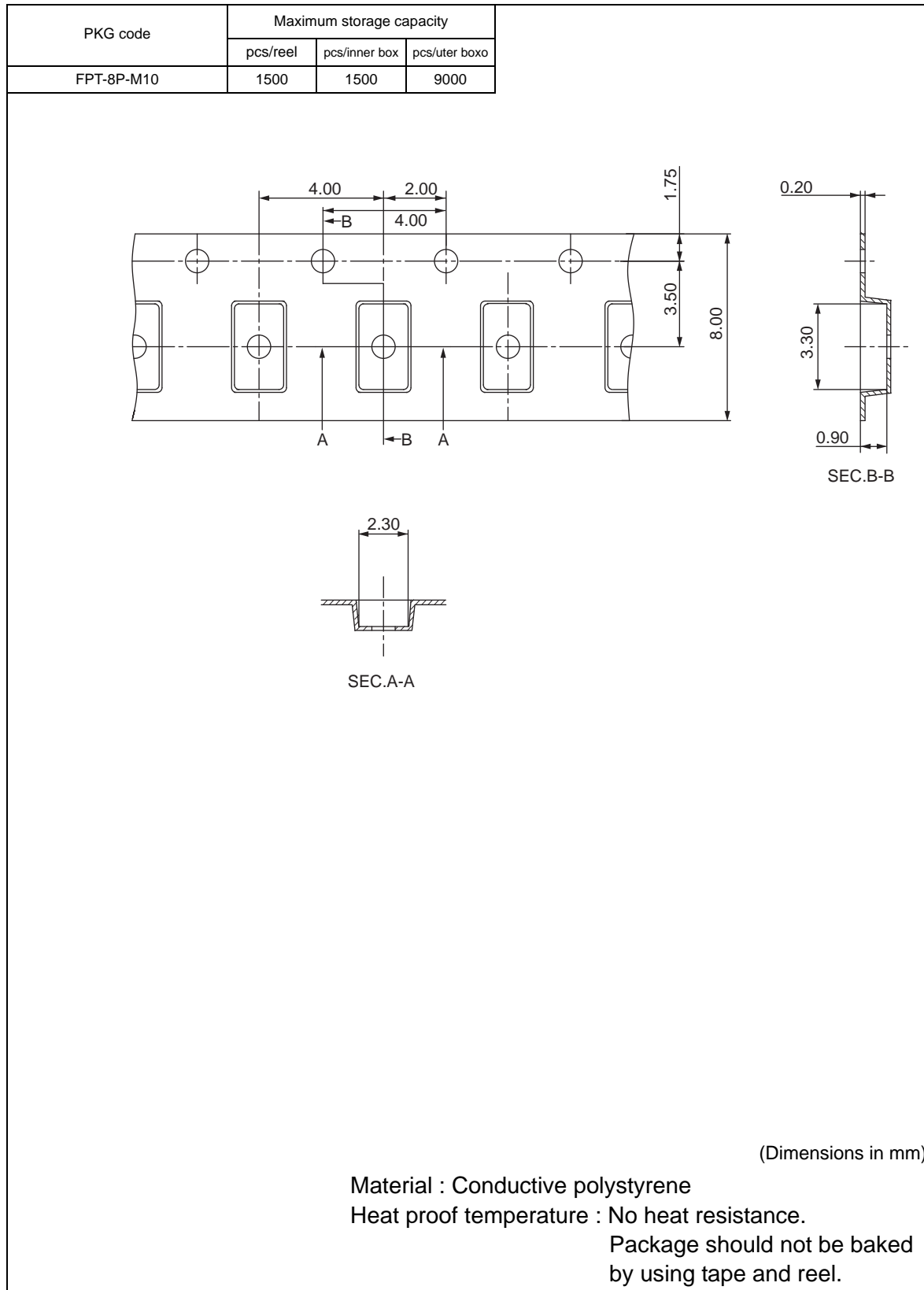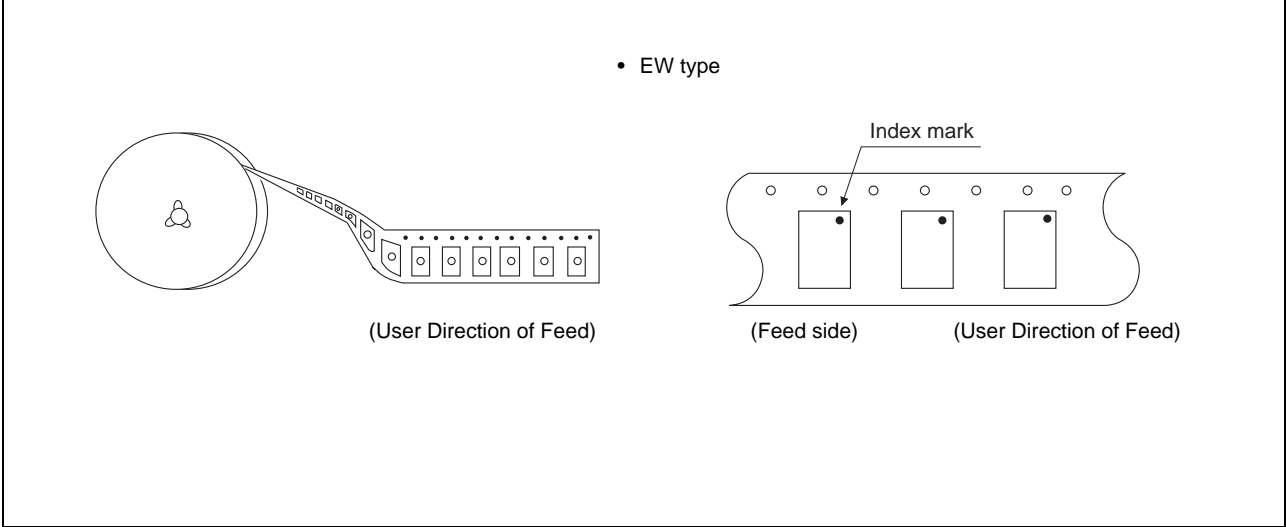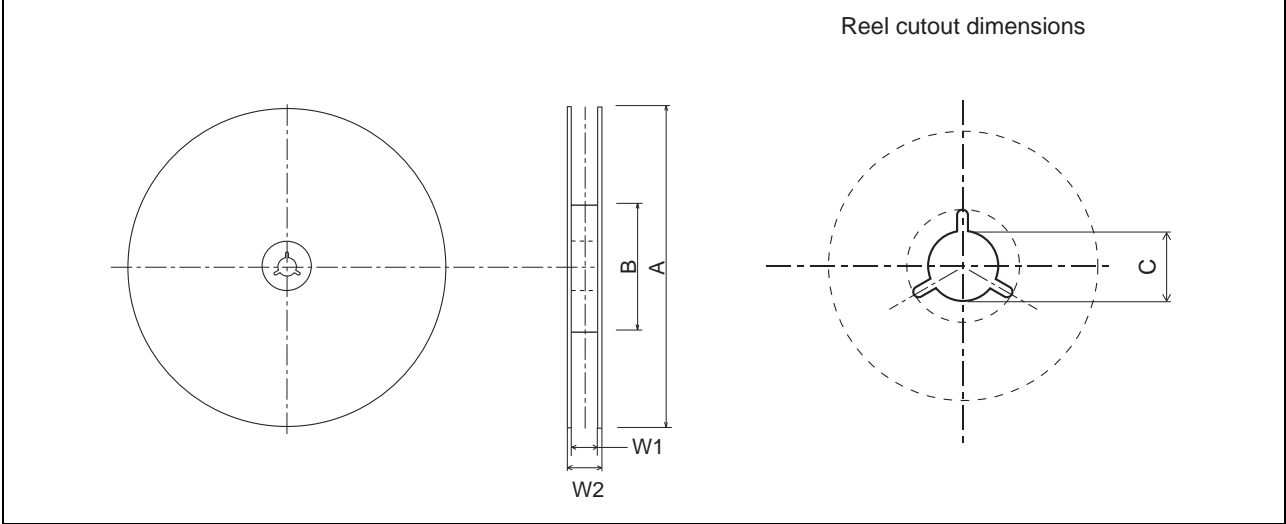
Dimensions in mm

Tape width	A	B	C	W1	W2
8	254	100	13	9.5	13.5

2.3 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

```
XXXXXXXXXXXXXX       (Customer part number or FJ part number)
                                        [G]  (Pb)              ◄─── C-3 Label
(3N)1 XXXXXXXXXXXXXXX XXX           (LEAD FREE mark)
|||||||||||||||||||||||||||||     (Part number and quantity)
                                             QC  PASS
(3N)2 XXXXXXXXXX  XXXXXX
|||||||||||||||||||||||||||||     (FJ control number)
            XXX  pcs            (Quantity)
XXXXXXXXXXXXXX       (Customer part number or FJ part number)
|||||||||||||||||||||||||||||  (Customer part number or FJ part number
                                                        bar code)
XXXX/XX/XX (Packed years/month/day)     ASSEMBLED IN xxxx      ◄─── Perforated line

XXXXXXXXXXXXXX  (Customer part number or FJ part number)        ◄─── Supplemental Label
(FJ control number bar code)
||||||||||||        XX/XX                XXXX-XXX   XXX
                  (Package count)        XXXX-XXX   XXX
  XXXXXXXXXX  (FJ control number )   (Lot Number and quantity)
XXXXXXXXXXXXXX  (Comment)
```

Label II: Moisture Barrier Bag *(It sticks it on the Aluminum laminated bag)
[MSL Label (100mm × 70mm)]

◄─── MSL label

*: MLS label is attached only to following part number.
　MB85RS64VYPNF-G-BCERE1

2.4 Dimensions for Containers

(1) Dimensions for inner box
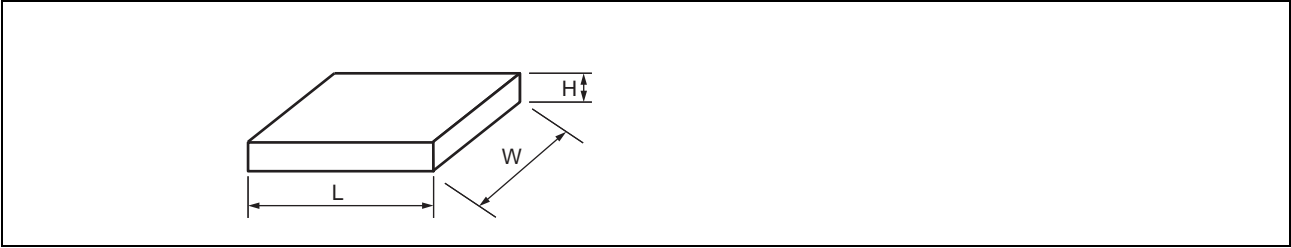
Tape width	L	W	H
8,12	265	262	51

(Dimensions in mm)

(2) Dimensions for outer box
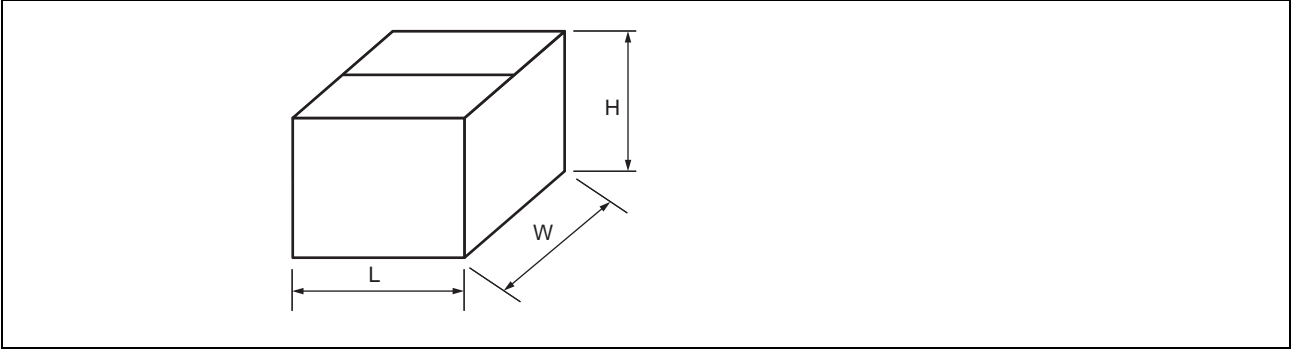
L	W	H
549	277	180

(Dimensions in mm)

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