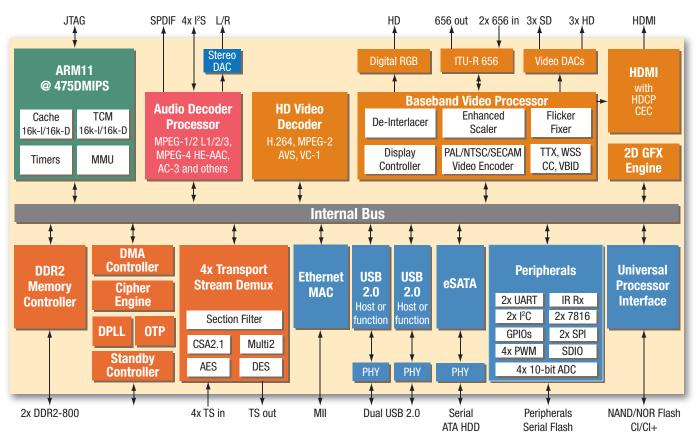# MB86H61 HD multi-standard decoder highly integrated SoC for HDTV receivers

MB86H61 block diagram

Description

The MB86H61 is a fully featured HD decoder SoC incorporating all the processing functions required by next generation HDTV receivers including advanced security for CI+ and embedded CAS and a low-power stand-by controller - ideal for set-top boxes, PVR and car TV receivers. It incorporates the high performance ARM processor 1176JZF-STM featuring an integrated memory management unit (MMU), a floating point co-processor, ARM's Jazelle® technology and Thumb® instruction set extensions for compact code. The ARM11 provides all the processing power needed to enable a whole host of middleware software. This cost-effective, low power, high definition media processor is able to decode MPEG-2, H.264/AVC, AVS and VC-1 compressed video up to HD resolution. HD video can be provided either via the copy-protected HDMI output, analogue component outputs or the digital RGB interface. The chip features a de-interlacer for converting interlaced standard definition video signals up to 1080p50/60. Simultaneously, the video signal can be scaled-down and offered in SD resolution.

The integrated audio processor can decode a wide variety of audio standards required by the broadcast market such as MPEG-1/2 Layer 1, 2, 3, MPEG-4 HE-AAC. Furthermore, support for Dolby® Digital and Dolby® Digital Plus is planned. Available audio outputs are four I²S, S/P-DIF and stereo analogue outputs.

Advanced connectivity is provided by two USB 2.0 interfaces, a 10/100 Base-T Ethernet MAC and a SATA II interface for connecting an internal or external HDD. Each USB controller can operate either as host or function.

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Integrated peripherals include two serial ports, two ISO7816 smart card interfaces, two I²C controllers, front-panel and keypad controller, IR receiver, two SPI outputs, four PWM outputs and 96 GPIOs. The number of usable GPIOs depends on the system configuration since they are shared among other I/O functions.

For evaluating the device and starting software development, Fujitsu offers the MB86H61 development kit. It comprises the evaluation board, documentation, schematics and a comprehensive software package including drivers, sample applications, tools, an operating system and more.

The MB86H61 is available in the following main variations:

MB86H610 Standard version of Free-To-Air STB/PVR including support for CI+

MB86H611 Embedded CAS version for PayTV applications

MB86H615 Shrunk version with reduced features set and QFP256 package

MB86H618 Extended temperature version, AEC-Q100 compliant

Features

- ARM1176JZF-S™ @ 475DMIPS with 16k-I/16k-D cache, 16k-I/16k-D TCM, FPU, MMU
- Bootable from parallel NOR, NAND or serial flash
- 2x 16-bit DDR2-800 SDRAM interface
- HD video decoder supporting H.264/AVC Level 4.1 high profile, MPEG-2 HD/SD MP@HL, AVS Jizhun Profile 6.0 and VC-1 AP Level 3
- Programmable audio processor, audio firmware available or planned for MPEG-1/2 Layer 1, 2 and 3 (MP3), HE-AAC, Dolby® Digital and Dolby® Digital Plus
- Advanced security features such as secure boot, OTP, secure control word handling, memory encryption, debug port control
- 2x USB 2.0 controller and PHY configurable as host or function
- Ethernet 10/100 Base-T MAC
- SATA II interface
- Universal processor interface (NAND/NOR flash, DVB-CI/CI+)
- 4x transport stream decoder and descramblers (DVB CSA 2.1, AES/DES, Multi2)
- 2D graphics accelerator
- Display controller supporting 7 layers with programmable order: Background, video, cursor, 4x OSD (up to true colour in HD resolution, one layer scalable with flicker fixer, YCrCb or RGB colour space)

- 1080p @ 50/60Hz video output
- Teletext, WSS, CC, VBID insertion
- Cross colour and luminance filters
- PAL/NTSC/SECAM digital encoder
- HDMI Link and PHY with HDCP and CEC
- 3x DAC for HD (YPrPb) and 3x DAC for SD video output
- 1x ITU-R 656 output and 2x ITU-R 656 input
- Digital RGB888 video output (HD)
- Stereo audio DAC and S/P-DIF output
- 4x I²S output and 4x I²S input
- 2x UART, 2x ISO7816 smart card, 2x I²C, 4x PWM, IR Rx, 2x SPI, SDIO
- Up to 96 GPIO (shared with other I/O functions, flexible pin assignment)
- 5 digit 7-segment LED display and keypad controller
- 10-bit ADC with 4 channels
- Internal clock recovery (no external VCXO required)
- On-chip stand-by controller (powered separately)
- PBGA 484 package, 27 x 27mm
- Fujitsu CMOS 90nm technology
- Operating temperature range: 0 to +70°C (optional -40 to +85°C)

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