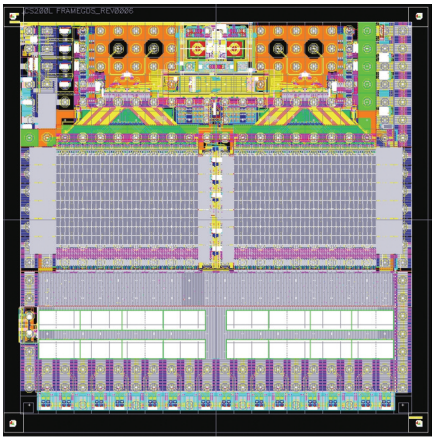
FACTSHEET
56GSa/s 8-BIT ADC

FUJITSU

56GSa/s 8-bit analogue-to-digital converter



Two channel version of 56GSa/s ADC using CHAIS architecture

Description

Fujitsu's ultra-fast CMOS ADC enables upcoming telecommunication applications, such as 100G Ethernet and OTU-4 transport systems using coherent receivers. The ADC uses Fujitsu's revolutionary Charge-mode Interleaved Sampler technology (CHAIS), which allows the implementation of extremely fast and high resolution ADCs in CMOS process technology.

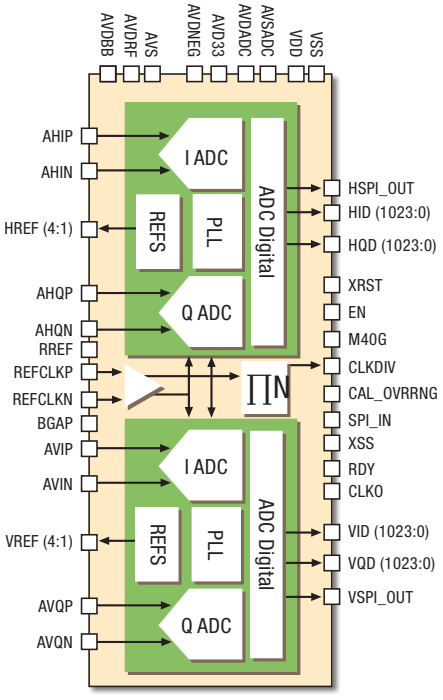
Major benefits of the CHAIS ADC are low power consumption and the option to be integrated with millions of gates onto the same die using Fujitsu's standard 65nm CMOS process technology. In combination with Fujitsu's leading flip-chip packaging technology, the ultra-fast ADC is ideal for applications that require high performance analogue and huge digital processing power while maintaining a reliable and proven manufacturing flow.

With an effective resolution bandwidth of >15GHz and a sample rate of 56GSa/s the ADC is at the leading-edge of converter performance.

The macro employs a self-contained background calibration technique for sampler interleave timing skew as well as linearity and offset. The calibration block also contains an alarm function, which can be used as an interrupt to warn the system when internal calibration reaches a pre-defined or programmable percentage of its calibration range.

The first customer evaluation silicon (ROBIN) for the CHAIS technology contains a two channel 56GSa/s version of the ADC. The on-chip RAM of ROBIN is used to store 16k x 8-bit samples for each ADC. The data can be accessed by reading this memory as there is no external output from the converter. There are several storage modes available that enable control of the RAMs from external triggers.

ADC block diagram



Four channel version of high-speed ADC

Other versions of the ADC with lower and higher sampling rate as well as different channel configurations are in development or planned.

Applications

- Fast data conversion
- 40G/100G communications systems
- Test equipment

Features

- Fujitsu 65nm CMOS process technology
- Resolution: 8-bit
- Sampling rate: 56GSa/s
- Power supply: -1.2V, 1.2V, 3.3V
- Power consumption: 2W per channel (typical)
- DNL: ±0.5 LSB, INL : ±1.0 LSB
- SNDR: 40dBFS @Fin=1GHz 36dBFS @Fin=17GHz
- Differential analogue Input: $1.0V_{PPD}$
- >15GHz -3dB input bandwidth
- Two's complement data format
- Output rate: 128 samples x 8-bit @437.5MHz
- 1.75GHz input reference clock
- Internal 14GHz VCO/PLL per I/Q ADC pair
- 56GSa/s ADCs configured as two I/Q Pairs
- <100fs rms jitter, <500fs I/Q sample time error
- Continuous background calibration for sampler interleave timing skew as well as linearity and offset
- Calibration warning and over-range flags
- Designed for Flip-Chip

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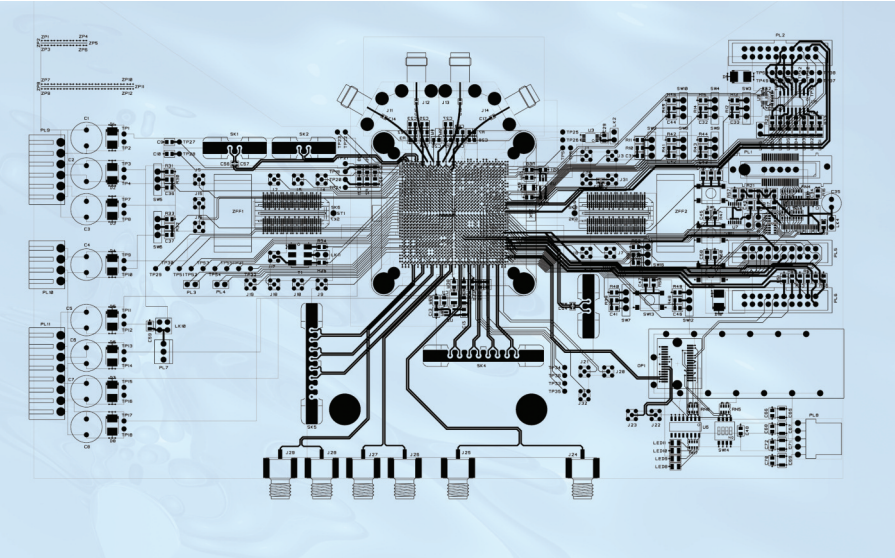

BATBOARD PCB layout

Development kits

A development kit is available for the two-channel 56GSa/s ADC evaluation test chip in a ceramic package (ROBIN).

Each kit includes:

- BATBOARD evaluation board with choice of ROBIN being solder mounted or with socket
- Calibration board with device mounted on it
- High frequency splitter board
- Interconnect boards
- PC programming interface board
- Software

The kit includes everything needed to minimise the time to get started, including evaluation board, PC-USB interface and PC software utility.

Description of development kits

The 56GSa/s ADC evaluation board (BATBOARD) is intended to allow rapid characterisation of the ADC. Two variants of the board are available. The first board is mounted with a low inductance socket, which allows rapid replacement of the device under test. The socket incorporates a heat-sink for increased heat dissipation. This can also be used with temperature forcing systems to precisely control the die temperature. The second board has a device mounted directly onto it. Special attention has been given to the connector choice to allow connection to instrumentation, which will perform the design verification tests. The printed circuit board utilises high performance materials to optimise the integrity of the signals. The development kit also includes Fujitsu's serial interface cable (ref DKSERIAL-1) that allows the device to be programmed through a Windows® application running on a host PC.

Key features of development kits

- Device mounted to a high performance printed circuit board
- Superior signal integrity by using low-loss PCB materials
- 2 channel 56GSa/s ADC
- On-chip memory to capture ADC output data
- Software for control of the device from host PC
- Option to mount a low inductance socket to allow replacement of device under test

Development kit part numbers

- BATBOARD-DK
  This evaluation board is supplied with a device mounted directly onto it
- BATBOARD-DK-SOCKET
  This evaluation board is supplied with a low inductance socket

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