Fujitsu has developed an ARM11 SoC prototyping chip based on the ARM1176 and the AXI bus. This chip allows customers to evaluate the performance of an ARM1176JZF-S, the AXI components and the CoreSight in real silicon.

**Process technology**
- 90nm CMOS

**Evaluation chip features**

**CPU cores**
- 4 Cores (ARM1176JZF-S x2, ARM926EJ-S x1, ARM946E-S x1)

**AXI extension**
- AXI Master Port and AXI Slave Port
- 32-bit Data width
- Double Data Rate (Max. 125MHz)
DMAC
• AXI Compatible, 8ch
• 8-bit, 16-bit, 32-bit, 64-bit width transfer
• 16 Double-word FIFO
• Un-aligned transfer, descriptor chain DMA

DMC (DDR controller)
• Mobile DDR (max. 125MHz)

MEMC (memory controller)
• 8 chip selects for ROM/Flash/SRAM and other memory mapped devices
• Supports NAND and NOR type Flash

Internal SRAM
• 64kB SRAM x2 (total 128kB)
• 64kB with secure adapter (for TrustZone)
• 64kB without secure adapter

Ethernet MAC
• 10/100base

Other I/O peripherals
• GPIO (32ch), UART (3ch)

CPU dedicated peripherals
• Vectored interrupt controller (64ch)
• Secure interrupt controller (TZIC)
• External interrupt controller (24ch)
• Timer (32-bit counter x2)
• Watchdog timer

System peripherals
• Clock and reset generator
• Remap and boot controller
• TrustZone protection controller
• Multi-core controller
• Inter-processor communication module

Low power modes
• STOP mode (CHIP clock is stopped)
• Sleep mode (ARM core clock is stopped)
• Dynamic clock control for DMAC and DDR controller
  • Stop the clock of DMAC and DDRC when these macros are inactive

Debug features
• Debugging via CoreSight DAP (Debug Access Port)
• Direct access to the system memory and registers without halting the core
• Cross-triggering between cores for multi-core debugging
• Multi-core simultaneous Trace

Max. operating frequency
• ARM1176JZF-S 500MHz
• ARM926EJ-S 250MHz
• ARM946E-S 250MHz
• Bus AXI 250MHz, AHB 125MHz, APB 62.5MHz

Package
• FCBGA 1156