Fujitsu Semiconductor Europe

Factsheet
Fujitsu ARM Cortex Design Support

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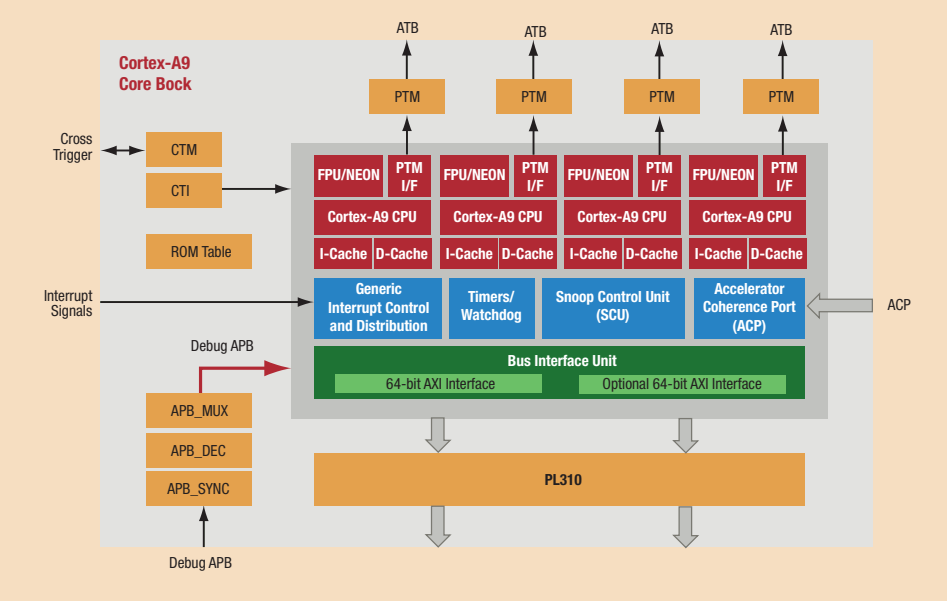
FASP Support (Fujitsu ARM® based SoC Prototyping Kit)

- FASP is a reference design concept of ARM based SoC
- All Fujitsu IPs are integrated into a reference design
- FASP consists of a reference design (RTL), simulation environment, example program (boot code), synthesis environment, net list, verification environment (FV script and example STA scripts)
- FASP enables the customer to shorten the design TAT and verification TAT
- FASP will support the following ARM cores:
  - Cortex™-M3
  - Cortex-A9
  - Cortex-R4F
  - Cortex-A5 (planned)
  - Cortex-A15 (planned)

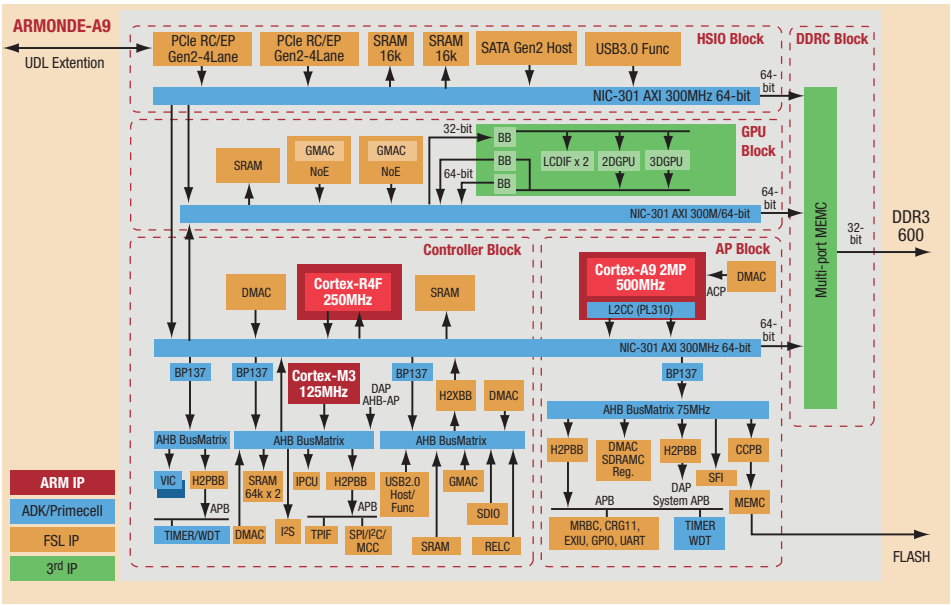


Cortex-A9 Block diagram

ARMONDE-A9 (ARM Evaluation Chip)

This ARM evaluation chip is targeted to develop high performance ARM based SoCs and contains therefore the Cortex-A9, Cortex-R4 and Cortex-M3 cores. In the future, the EV chip will have implemented Fujitsu advanced IPs like PCIgen2, SATAgen2, USB3.0, etc.
This EV chip enables designers to develop IP drivers and OS. Also, the TAT for SoC prototyping will be much shorter.
An Evaluation Board will also be provided with the ARMONDE-A9. This board is available with an LCD monitor (touch panel) and FPGA for user logic extension. The following deliverables are available with the board:

- FPGA reference design
- Software (OS: Linux, ITRON or Android)
- Drivers for IPs
- ARMONDE-A9 Block Diagram
- IPs used on ARMONDE-A9 (see table on P2)



Operating frequency (except as otherwise stated) AXI= 64-bit/300MHz, AHB= 32-bit/150MHz, APB= 32-bit/75MHz

ARMONDE-A9 Block diagram

IPs on ARMONDE-A9

Category	IP Name	Descriptions
Processor	Cortex-A9 MPcore	Dual-core, 500MHz, L1 cache I/D=32KB/32KB, L2 cache = 512KB, ACP-DMA
	Cortex-R4F	250MHz, L1 cache =16KB/16KB, TCM_A=64KB, TCM_B0=32KB, TCM_B1=32KB
	Cortex-M3	125MHz
	GPU	OpenGL ES1.1/OpenGL ES2.0/OpenVG1.1, LCD Controller (2-ch)
Interface Macro	PCIe	PCI Express Gen2, Root/Endpoint, 4-lanes (2-ch/SoC IF + FPGA extension)
	SATA	Serial ATA Host Gen2
	USB3.0	USB3.0 Function
	USB2.0 HDC	USB2.0 Host/Function DMAC
	GMAC	Ethernet MAC 1000/100base, 802.3az (LPI), GMII, IEEE1588
	SDIO	UHS-1(eMMC)
	UART	UART (2-ch)
	I^2C	I^2C (1-ch)
	I^2S	I^2S (1-ch) + DMAC
	SSP (PL022)	Compatible with Motorola SPI, TI SSI and National Semiconductor Microwire
	NoE	2ch IPSec Network Off-load Engine with GMAC4MT (700Mbps half duplex IPSEC)
	TPIF	Touch Panel Interface (Multi-touch detection)
Memory I/F	SDRAMC	DDR2/3-600MHz 32-bit
	MEMCS	Flash/SRAM Controller
	SPI	Quad Serial Flash Controller
CPU Peripherals	–	VIC (Vectored Interrupt Controller), CRG11 (ClockReset Generator), IPCU (Inter-processor Communication Unit), GPIO, Watchdog, Timer, MRBC (Remap and Boot Controller), SYSOC (System Operation Controller), SRAM on AXI (128KB), SRAM on AHB (64KB x2)
Bus Interconnect	NIC-301	ARM Network Interconnect (AXI, AHB, APB)
	AHB BusMatrix	AHB Interconnect
Others	OPAL/RELC/ADC	Instruction encryption/data compression and decompression / ADC 2ch for touch panel control

High-speed Cortex-A9 HLB (Hierarchical Layout Block)

- 65nm: 600MHz
- 40nm: 800MHz
- 28nm: 1000MHz

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