ASSP
EPCglobal Class1 Generation2 Compliant
FRAM Embedded UHF Band RFID LSI

MB97R8120/8130

1. OVERVIEW

This specification provides LSI specifications for the passive RFID Tag LSI "MB97R8110" (user bank 60kbits) based on "EPCglobal Class 1 Generation 2."

In this specification, the term “interrogator” used in the EPCglobal standard is changed to R/W (reader/writer) in accordance with customary practice. The term “Tag” is used as is.

1.1 FEATURES

- Compliant with EPCglobal Class 1 Generation 2 (C1G2)
  - −Carrier frequency: 860 to 960 MHz
  - −Data rate
    - R/W → Tag: 26.7 kbps to 128 kbps (when the counts of data 0 and data 1 are equal)
    - Tag → R/W: 40 kbps to 640 kbps
- Serial Interface (SPI) :MB97R8130
  - −Slave mode operation : User memory area can be read/written through SPI.
  - −Arbitration feature between RF and SPI access controlled by SPIREQ and SPIACK.
- High speed read/write Non-volatile memory (FRAM)
  - −USER bank size: 61,440 bits
  - −EPC length: up to 480bits
  - −Block Permalock: User memory area can be locked from writing in units of 512 words (=8,192bits).
  - −Read/Write Endurance: 10^{13} times
  - −Memory data retention: 10 years (+85 ºC)

・ 1.2 BLOCK DIAGRAM

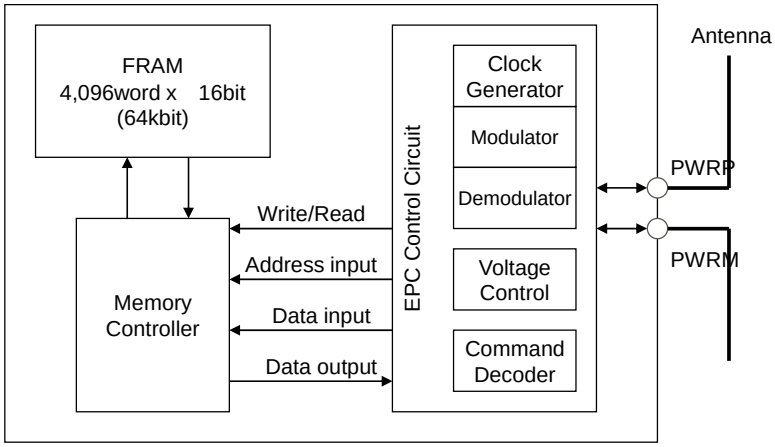


Figure1.2.1.1 - BLOCK DIAGRAM (MB97R8120)

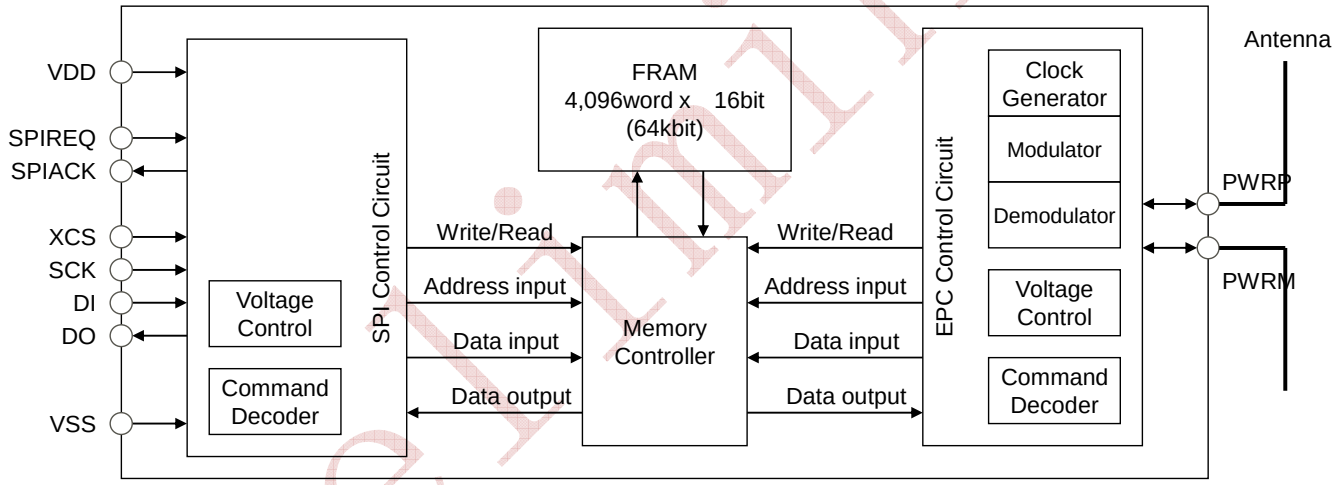


Figure1.2.1.2 - BLOCK DIAGRAM(Mb97R8130)

1.3 PAD CONFIGURE (MB97R8130)

1.3.1 Pad Configure

The following is PAD configure for this LSI.

Table1.3.1 TSSOP16 package pad location

No.	Pin	In/Out	Function
1	VSS	In	Ground
2	VDD	In	Voltage apply for SPI communication
3	SPIREQ	In	SPI Slave Request
4	SPIACK	Out	SPI Slave Acknowledgement
5	SCK	In	Serial Clock
6	DI	In	Serial Data Input
7	DO	Out	Serial Data Output
8	XCS	In	Chip Select
12	PWRP	In/Out	Antenna
14	PWRM	In/Out	Antenna
9,10, 11,13 15,16	NC	—	No connection Recommended to be open

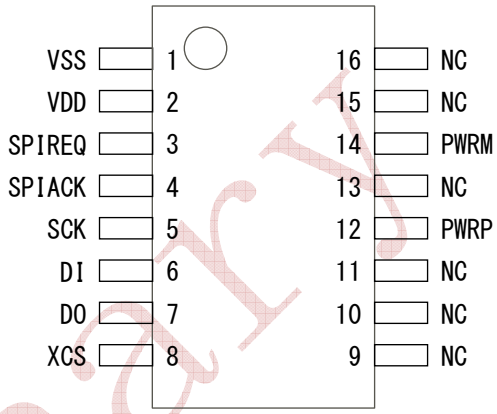


Fig. 1.3.1 TSSOP16 Package

2 RF INTERFACE

RF signal interface is compliant with EPCglobal Class 1 Generation 2 Ver.1.2.0.

2.1 Modulation type, communications timing

Compliant with EPCglobal Class 1 Generation 2 Ver.1.2.0.

2.2 Inventory, Tag selection

Compliant with EPCglobal Class 1 Generation 2 Ver.1.2.0.

2.3 Tag state-transition

Compliant with EPCglobal Class 1 Generation 2 Ver.1.2.0.

2.4 RF communication error code

This LSI responds the error code as shown in Table2.4 if it encounters an error when executing a handle-based command under Open state or Secured state. The reply format and the error code is compliant with EPCglobal Class 1 Generation 2 Ver.1.2.0 (as described in AnnexI)

Table 2.4 Error code

Error code	Error code name	Error description
00h	Other errors	Other errors not covered by the following errors
03h	Out of memory	The specified memory location does not exist.
04h	Memory lock	The specified memory location is locked or permalocked

3 SPI interface

3.1 Overview

This LSI has SPI (Serial Peripheral Interface) interface that can be operated as follows.

・This LSI is able to access FRAM User memory through the SPI interface (External power supply required).

・The external SPI slave device can be controlled by this LSI (Power supplied by this LSI).

3.2 SPI Mode

This LSI is only corresponding to the SPI mode 0 (CPOL=0, CPHA=0).

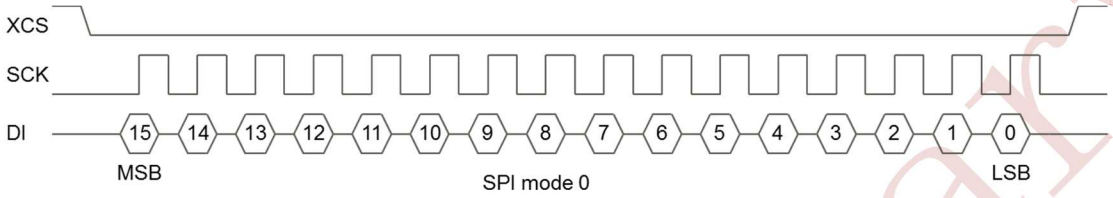


Figure 3.2.1 – SPI mode

3.3 SPI Slave Interface

3.3.1 Connection to SPI Interface

This LSI can work as a slave mode of SPI. It can be connected to the microcontroller equipped with SPI port as shown in the figure 3.3.1.

SPIREQ should be set to “H” before starting the slave communication. Then SPI slave communication is enabled, and SPIACK shall output “H”. SPI slave communication shall be executed as XCS=”L” and SPIREQ is required to hold “H” until SPI slave communication is completed. The SPI slave command is executed continuously without any interruption by RF communication during the period of SPIACK "H".

SPI communication will not be started if SPIACK signal is “L”.

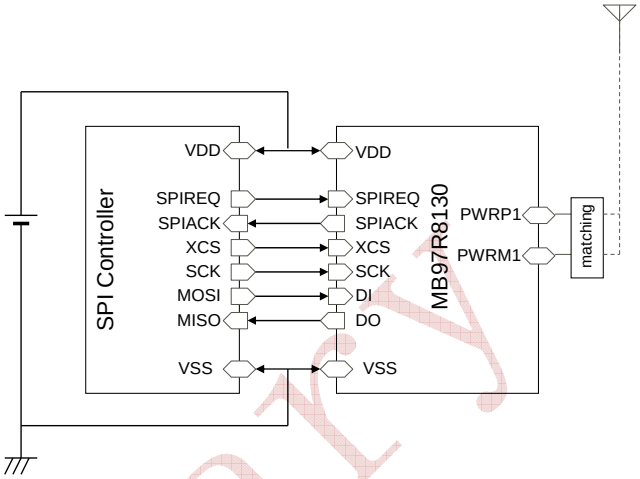


Figure 3.3.1 - SPI Slave interface connection

3.3.2 Power down mode

This LSI implements Power down mode if SPIREQ is switched to “L”, which enables to reduce current consumption of the battery connected between VDD-VSS. (refer to 8.4.1) When the voltage is applied on VDD, and SPIREQ=”L” without RF carrier, the output of both SPIACK and DO becomes undefined, it is recommended for controller to deactivate the signal to SPIACK and DO. All the control pin (including XCS) excepting VDD must be “L” in power down mode.

3.3.3 Usage

Please refer to Chapter 5.2 and 5.3.regarding the usage of SPI slave interface.

3.4 Power sequence and interface arbitration

3.4.1 Arbitration between RF and SPI slave communication

The arbitration feature to control the access through RF and SPI slave interface is managed by SPIREQ and SPIACK signals. The state of SPIACK, which is normally “L”, shall be set to “H” before starting SPI slave communication. After SPIACK is “H”, power can be applied to VDD. The controller inputs “H” to SPIREQ pin and requests MB97R8110 to get start SPI communication. SPI slave communication starts after MB97R8110 outputs “H” to SPIACK and then makes XCS “L”. During the period when SPIACK is “H”, SPI communication is prioritized and any request through RF interface is ignored. Therefore SPIACK needs to be back to “L” after completing SPI communication in order to receive new request through RF interface.

The arbitration sequence between RF communication and SPI slave communication is shown as Figure 3.4.1.

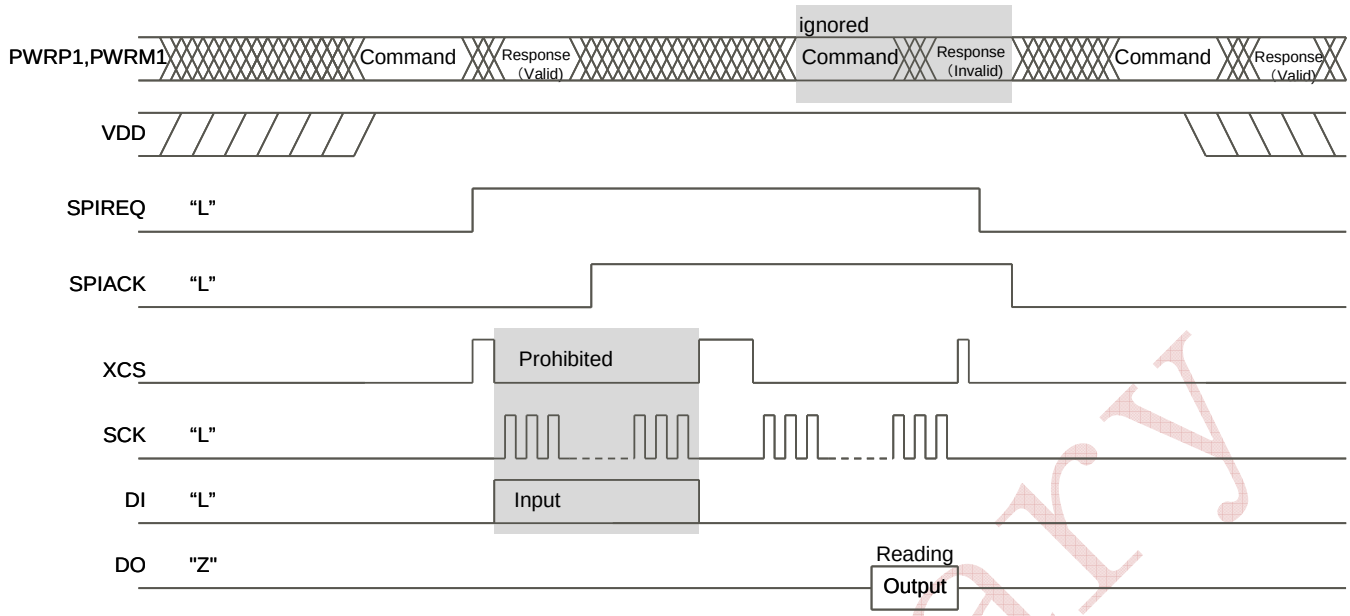


Figure 3.4.1 －The arbitration sequence between RF communication and SPI slave communication

4 Memory

4.1 Memory address

4.1.1 Address description

Data is stored in units of word (16bits). The logical address each memory bank is described as WordAdr in this document. WordPtr is the address used in the RF command format, which is described with EBV format as specified in EPCglobal Gen2 specification.

Address range	WordAdr (Serial access)	WordPtr (RF access)	Correlation between WordPtr and WordAdr
0000h～007Fh	0000h～007Fh	00h～7Fh	WordPtr={0, WordAdr[6:0]}
0080h～3FFFh	0080h～3FFFh	8100h～FF7Fh	WordPtr={1,WordAdr[13:7], 0,WordAdr[6:0]}

4.2 Memory Map

4.2.1 Memory bank

The Non-volatile memory (FRAM) of this LSI is divided into the following four banks.

Table 4.2.1 Four memory banks

Bank	Memm Bank	WordAdr	BANK specifiable or not							
			RF communication						SPI communication	
			Read	Write	BlockWrite	BlockErase	BlockPermalock	Select	SpiRead	SpiWrite
USER	11	12'h000h～12'hEFFh	○	○	○	○	○	○	○	○
TID	10	7'h00h～7'h0Ch	○	–	–	–	–	○	○	–
EPC	01	7'h00h～7'h1Fh	○	○	○	○	–	○	○	–
Reserved	00	7'h00h～7'h3Fh	○	○	–	–	–	–	–	–

The User, TID, EPC, and Reserved memory banks contain the data that is defined by the EPCglobal C1G2 specification (6.3.2.1 item). In each memory bank, the logical address (WordAdr) starts from zero (00H).

4.2.2 TID bank

TID bank of this LSI is specified in Table 4.2.2. TID bank memory can only be read and cannot be written. Refer to EPC global『Tag Data Standard』specification in 16.1～16.3 item for details

Table 4.2.2 TID bank set value

	MSB															LSB	
WordAdr	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Set Value
00h	Allocation Class								Designer								E281h
01h	Designer							Product ID							Version		0081h
02h	XTID header																3C00h
03h	Serial Number																*unique*
04h	Serial Number																*unique*
05h	Serial Number																*unique*
06h	optional command support																1DDEh
07h	BlockErase parameter																0002h
08h	BlockErase parameter																0310h
09h	BlockWrite parameter																0002h
0Ah	BlockWrite parameter																0310h
0Bh	Permalock Block size																0200h
0Ch	User memory size																0F00h

4.2.3 EPC bank

The EPC bank value of this LSI is initialized as shown in Table 4.2.3 when shipped.

Table 4.2.3 EPC bank initial value

	MSB															LSB	
WordAdr	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Intial Value
00h	Stored CRC																
01h	Stored PC																3400h
02h	EPC data																0000h
03h	Serial Number																*unique*
04h	Serial Number																*unique*
05h	Serial Number																*unique*
06h	EPC data																0000h
07h	EPC data																0000h
08h	(EPC data)																0000h
09h	(EPC data)																0000h
0Ah	(EPC data)																0000h
0Bh	(EPC data)																0000h
0Ch	(EPC data)																0000h
0Dh	(EPC data)																0000h
0Eh	(EPC data)																0000h
0Fh	(EPC data)																0000h
10h	(EPC data)																0000h
・・・	(EPC data)																0000h
1Fh	(EPC data)																0000h

The length of Stored PC is set to 6 (word) when shipped. The same Serial Number data of WordAdr 03h～05h is also written into WordAdr 03h～05h in TID bank. It is possible to use the address of WordAdr 08h～1Fh (max 30word) if the setting value is larger than 6, however, the sensibility of the LSI will decrease possibly if the length is not 6.

This LSI does not support XPC_W1 and XPC_W2.

Stored CRC is not fixed value, because it is calculated value on the response ACK command.

4.2.4 USER bank

The User memory bank of this LSI consists of 8 Area Group as shown in Table 4.2.4.

Table 4.2.4.1 USER bank configure

	MSB															LSB	
WordAdr	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Initial Value
000h～1FFh	User data (Area0)																0000h
200h～3FFh	User data (Area1)																0000h
400h～5FFh	User data (Area2)																0000h
600h～7FFh	User data (Area3)																0000h
800h～9FFh	User data (Area4)																0000h
A00h～BFFh	User data (Area5)																0000h
C00h～DFFh	User data (Area6)																0000h
E00h～EFFh	User data (Area7)																0000h

The access control such as PermaLock and Password can be applied by Area units. The Permalock block and the Area is exactly the same in this LSI. Please refer to “BlockPermalock”(Chapter 5.1.3) and “Data protection for USER bank”(Chapter 6.2).

Multiple words access across the Areas can be specified by RF command(BlockWrite, BlockErase, and Read command). SPI slave communication command cannot access to the WordAdr ”7FFh” through “800h” with one continuous command and the address is rolled over to “000h”.

4.2.6 Reserved bank

Reserved bank is used for Password data management.

32bits Password can be set by 2steps of 16bits writing, 1st for [31:16] and 2nd for [15:0] by Req_RN and Write command as a set of sequence respectively without any other command between the steps.

Table 4.2.6 Reserved bank constructure

	MSB															LSB	
WordAdr	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Initial Value
00h	Kill password [31:16]																0000h
01h	Kill password [15:0]																0000h
02h	Access password [31:16]																0000h
03h	Access password [15:0]																0000h
04h	RFU																0000h
・・・																	0000h
1Fh	RFU																0000h
20h	Area password (Setting) (Area0) [31:16]																0000h
21h	Area password (Setting) (Area0) [15:0]																0000h
22h	Area password (Setting) (Area1) [31:16]																0000h
23h	Area password (Setting) (Area1) [15:0]																0000h
24h	Area password (Setting) (Area2) [31:16]																0000h
25h	Area password (Setting) (Area2) [15:0]																0000h
26h	Area password (Setting) (Area3) [31:16]																0000h
27h	Area password (Setting) (Area3) [15:0]																0000h
28h	Area password (Setting) (Area4) [31:16]																0000h
29h	Area password (Setting) (Area4) [15:0]																0000h
2Ah	Area password (Setting) (Area5) [31:16]																0000h
2Bh	Area password (Setting) (Area5) [15:0]																0000h
2Ch	Area password (Setting) (Area6) [31:16]																0000h
2Dh	Area password (Setting) (Area6) [15:0]																0000h
2Eh	Area password (Setting) (Area7) [31:16]																0000h
2Fh	Area password (Setting) (Area7) [15:0]																0000h
30h	Area password (Authentification) (Area0) [31:16]																0000h
31h	Area password (Authentification) (Area0) [15:0]																0000h
32h	Area password (Authentification) (Area1) [31:16]																0000h
33h	Area password (Authentification) (Area1) [15:0]																0000h
34h	Area password (Authentification) (Area2) [31:16]																0000h
35h	Area password (Authentification) (Area2) [15:0]																0000h
36h	Area password (Authentification) (Area3) [31:16]																0000h
37h	Area password (Authentification) (Area3) [15:0]																0000h
38h	Area password (Authentification) (Area4) [31:16]																0000h
39h	Area password (Authentification) (Area4) [15:0]																0000h
3Ah	Area password (Authentification) (Area5) [31:16]																0000h
3Bh	Area password (Authentification) (Area5) [15:0]																0000h
3Ch	Area password (Authentification) (Area6) [31:16]																0000h
3Dh	Area password (Authentification) (Area6) [15:0]																0000h
3Eh	Area password (Authentification) (Area7) [31:16]																0000h
3Fh	Area password (Authentification) (Area7) [15:0]																0000h

5 Command (Tag operation)

5.1 RF communication command

All mandatory commands and optional commands specified in EPCglobal C1G2 Ver.1.2.0. (Chapter 6.3.2.11) are supported as described in Table 5.1.0.

However, Parts of the specification of BlockWrite, BlockErase, BlockPermalock command (Optional command), and Read command (Mandatory command) are different form EPC C1G2 standard as described in Chapter 5.1.1, 5.1.2, 5.1.3, and 5.1.4.

Table 5.1.0 – RF mode command

Type	Command name	Command code
Mandatory	QueryRep	00
	ACK	01
	Query	1000
	QueryAdjust	1001
	Select	1010
	NAK	1100 0000
	Req_RN	1100 0001
	Read	1100 0010
	Write	1100 0011
	Kill	1100 0100
	Lock	1100 0101
Optional	Access	1100 0110
	BlockWrite	1100 0111
	BlockErase	1100 1000
	BlockPermalock	1100 1001

※Differences from EPCglobal C1G2 Ver. 1.2.0

(1) About CRC-16

If Stored PC and/or EPC data stored in EPC bank are renewed, StoredCRC-16 won't be updated when the power is turned on, but it is updated on the response to ACK command without truncation.

(2)About UMI

UMI stored in bit[10] of StoredPC in EPC bank is calculated by OR of bit[12:8] of WordAdr=00h in User bank according to EPCglobal C1G2 Ver. 1.2.0. UMI is fixed to "1" on this LSI.

(3) About Memory access by Read command

According to EPCglobal C1G2 Ver. 1.2.0, if WordCount=00h on Read command, the tag shall respond the whole data starting at specified WordPtr and ending at the end of the bank. The User bank is divided into 8 areas which enable to be protected by Area password. If part of specified area is protected, any data cannot be read and an error code (Memory locked "04h") is replied.

(4)The password data for data protection is stored in the WordAdr=20h-3Fh of Reserved bank.

5.1.1 BlockWrite (Optional command; partly supported)

BlockWrite command format is shown in Table5.1.1. Parts of the function are different from what is specified in the EPCglobal C1G2 Ver.1.2.0 as following.

• MemBank specifies only EPC and USER bank. If BlockWrite command is executed on Reserved and TID bank, an error code (Memory overrun “03h”) is replied. In this case, the data will not be written into the specified address.

• WordCount specifies the number of data to be written. If 00h is specified, the command will be ignored. The data can be specified up to 255(FFh) if WordPtr specifies WordAdr between 800h and EFFh in USER bank. If WordPtr specifies WordAdr between 000h and 7FFh, the data can only be specified below 16(10h), and if it is specified above 17(11h), an error code (Memory overrun “03h”) is replied. If part or all the words to be written is locked by the BlockPermaLock command or they are protected by AreaPassword, the unlocked words will not be changed and an error code (Memory locked “04h”) is replied.

Table 5.1.1 — BlockWrite command

	Command	MemBank	WordPtr	WordCount	Data	RN	CRC-16
Number of bits	8	2	EBV	8	WordCount *16	16	16
Description	1100 0111	01:EPC 11:USER	Starting Address Pointer	Number of word to write	Data to be written	Handle	

Multiple words write to the WordAdr ”7FFh” through “800h” can be specified by this command. On the other hands, SPI slave communication command cannot count up to “800h” but roll over to “000h”.

5.1.2 BlockErase (Optional command; partly supported)

BlockErase command format is shown in Table5.1.2. Parts function of BlockErase command are different from the EPCglobal C1G2 Ver.1.2.0 as described as follows.

・MemBank specifies only EPC and USER bank. If BlockErase command is executed on Reserved and TID bank, an error code (Memory overrun”03h”) is replied. In this case, the data will not be erased in the specified address.

・WordCount specifies the number of data to be erased. If 00h is specified, the command will be ignored. If part or all the words to be erased is locked by the BlockPermaLock command or they are protected by AreaPassword, the unlocked words will not be changed and an error code (Memory locked”04h”).

Table 5.1.2 - BlockErase Command

	Command	MemBank	WordPtr	WordCount	RN	CRC-16
Number of bits	8	2	EBV	8	16	16
Description	1100 1000	01:EPC 11:USER	Starting Address Pointer	Number of word to erase	Handle	

5.1.3 BlockPermaLock (Optional command; partly supported)

The unit of Block to be locked is defined as 512 words for this LSI. The Permalock command can be executed to the 8 blocks of User bank which is 7 areas of 8k bits and 1 area of 4k bits.

5.1.3.1 BlockPermaLock（Setting）

The format of the BlockPermaLock command for Permalock setting is shown in Table 5.1.3.1. The Read/Lock value is set to “1”, and the specified bock will be locked permanently. Lock data field is described in Chapter 5.1.3.3.

Table 5.1.3.1 – BlockPermaLock command (Permalock)

	Command	RFU	Read /Lock	Mem Bank	BlockPtr	Block Range	Lock data	RN	CRC-16
Number of bits	8	8	1	2	8	8	16	16	16
Description	1100 1001	00h	1:Perma Lock	11:User	00h	01h	0:Retain current permalock setting 1:Assert permalock	Handle	

There is a limitation as follows. If any other value is set, error code (Memory overrun “03h”) will be responded and permalock operation is terminated.

- MemBank: Only executed for User bank.
- BlockPtr: Only 00h is supported.
- BlockRange: Only 01h is supported.

5.1.3.2 BlockPermaLock（Read）

The format of the BlockPermaLock command for reading permalock status is shown in Table 5.1.3.2.1. The Read/Lock value is set to “0”, and the permalock status of 8blocks of user bank can be read. The response is shown in Table 5.1.3.2.2.

Table 5.1.3.2.1 – BlockPermaLock command (Read)

	Command	RFU	Read /Lock	Mem Bank	BlockPtr	Block Range	RN	CRC-16
Number of bits	8	8	0	2	8	8	16	16
Description	1100 1001	00h	0:Read	11:User	00h	01h	Handle	

Table 5.1.3.2.2 – Response to BlockPermaLock command (Read)

	Header	Lock data	RN	CRC-16
Number of bits	1	16	16	16
Description	1100 1001	00h	Handle	

There is a limitation as follows. If any other value is set, error code (Memory overrun16 “03h”) will be responded and reading operation is terminated.

- MemBank: Only executed for User bank.
- BlockPtr: Only 00h is supported.
- BlockRange: Only 01h is supported.

5.1.3.3 BlockPermaLock and Permalocked Block

16bits of Lock data and corresponded block is shown in Table 5.1.3.3.

Table 5.1.3.3 – BlockPermaLock data

bit		Area	WordAdr
bit15	MSB	0	000h-1FFh
bit14		1	200h-3FFh
bit13		2	400h-5FFh
bit12		3	600h-7FFh
bit11		4	800h-9FFh
bit10		5	A00h- BFFh
bit9		6	C00h- DFFh
bit8		7	E00h- EFFh
bit7		—	—
bit6		—	—
bit5		—	—
bit4		—	—
bit3		—	—
bit2		—	—
bit1		—	—
bit0	LSB	—	—

When Lock data is set by BlockPermaLock command(see Chapter 5.1.3.1), Bit[7:0] shall be set to “0” because of no target block.

5.1.4 Read (Mandatory; partly supported)

The command format is shown in Table 5.1.4.1

Table 5.1.4.1– Read command

	Command	Mem Bank	WordPtr	WordCount	RN	CRC-16
Number of bits	8	2	EBV	8	16	16
Description	1100 0010	00:Reserved 01:EPC 10:TID 11:User	Starting Address Pointer	Number of words to read	Handle	

WordCount specifies the number of data to be read. Multiple words read to the WordAdr ”7FFh” through “800h” can be specified by this command. On the other hand, SPI slave communication command cannot count up to “800h” but roll over to “000h”.

When WordCount is set to “00h”, the response will be as shown in Table 5.1.4.2.

Table 5.1.4.2– Response to Read command with WordCount “00h”

MemBank	AreaPassword	Response
11:User	Zero password (All Area)	The data starting at specified WordPtr (Table 5.1.4.1) and ending at WordAdr “EFFh” are responded as normal response.
	Non zero Password (Some Area)	No data is read. Error code (Memory locked “04h”) is responded. (see Chapter 2.4)
10:TID	—	The data starting at specified WordPtr (Table 5.1.4.1) and ending at WordAdr “0Fh” are responded as normal response.
01:EPC	—	The data starting at specified WordPtr (Table 5.1.4.1) and ending at WordAdr corresponding to the length of EPC are responded as normal response.
00:Reserved	—	The data starting at specified WordPtr (Table 5.1.4.1) and ending at WordAdr “3Fh” are responded as normal response.

5.1.5 Lock (Mandatory; partly extended)

The command format is shown in Table 5.1.5. When the Access password (WordAdr=02h-03h of Reserved bank) is locked by setting Payload bit [17,16] and [7,6], Area passwords (WordAdr=20h-3Fh of Reserved bank) are also locked at the same time. Even if the password is locked, area access control with password authentication by Write command is effective as described in Chapter 6.2.

Table 5.1.5– Lock command

	Command	Payload	RN	CRC-16
Number of bits	8	20	16	16
Description	1100 0101	Mask and Action Fields	Handle	

5.2 SPI slave communication command

This LSI will support 3 types of operate-code for SPI slave interface. The operate-code is 8bits code described in Table 5.2.0. If other codes are input, this command is ignored. If XCS is raised during the input sequence of operate-code, the command cannot be executed.

Table 5.2.0 - Operate-code for SPI slave interface

Code name	Function	Operate-code
SpiRead	Read data in units of 16bits from user memory area.	0000 0011
SpiWrite	Write data in units of 16bits into user memory area.	0000 0010
SpiRDSR	Read 16bits of Error information register(SPI slave)	0000 0101

5.2.1 SpiRead

SpiRead command will be executed to read memory data in units of 16bits (1word). The address shall be specified as 2bits of MemBank followed by 14bits WordAdr (Total 16bits). The command sequence is described in Figure 5.2.1.

Through DI pin, the following data is received synchronously to the rising edge of SCK after falling XCS.

READ operate code (8bit:03h)

MemBankAddress (2bit)

WordAddress (14bit)

User bank, TID bank and EPC bank are readable banks. The upper 2 bit of Word address should be fixed to “00”.

DO will be output synchronously to the falling edge of SCK after the above data input. Value of DI will be ignored when DO is being output. SpiRead command will end after XCS is raised.

The reading address is automatically incremented by each 16-cycle clock input until XCS is rising. The read data will not be continued after XCS is rising and the output will be “Z” if XCS is rising in the different timing of 16 clock cycle. If the Word address is specified within 000h~7FFh of User bank, the counter rolls over to “0000H” after WordAdr reaches the most significant address 7FFh. If the Word address is specified within 800h~EFFh of User bank, the counter will not roll over to “000H” or “800h” even if SCK is toggled when WordAdr reaches the most significant address 7FFh. If the specified bank is other than User bank and Word address reaches to the most significant address, read operation ends even if XCS=”L” and DO output will be “0”.

The specified memory data will not be read out and output of DO pin will be “0” for the following cases.

1) This LSI is in Kill state
2) The specified address is in the protect area by Password
3) MemBank is specified with RSV bank

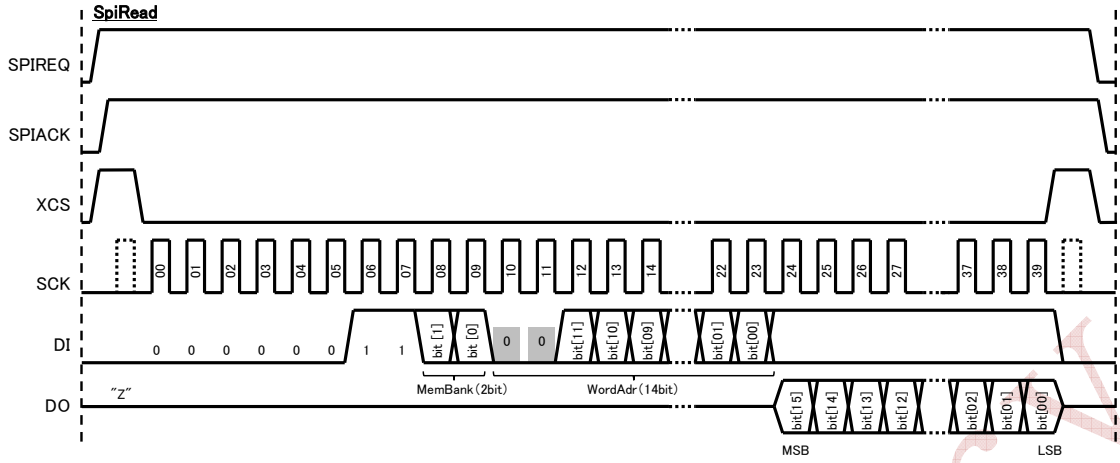


Figure5.2.1 – SpiRead command sequence

If part or all the words to be read are protected by AccessPassword or AreaPassword, the protected data cannot be read but the unprotected data can be read.

5.2.2 SpiWrite

SpiWrite command is executed to write data into memory in units of 16 bits (1 word). The specified address shall be 14bits WordAdr after 2bits of MemBank (Total 16bits) for RF communication. The sequence for SpiWrite command will be described in Figure 5.2.2.

The following data is input through DI pin synchronously to the rising edge of SCK after falling of XCS.

WRITEoperate-code (8bit:02h)

MemBankaddress (2bit)

Word address (14bit)

Written data (N*16bit)

USER bank is the only writable bank. The upper 2 bit of Word address should be fixed to “00”. SpiWrite command will end if XCS is raised.

The writing address is automatically incremented by the 16bits continuous data sending before XCS rising. If WordAdr reaches the most significant address “7FFh”, the counter will roll over to “0000H” and write cycle will continue to be operated. The Write operation will end and error information will be stored in error information register if XCS becomes “L” and the WordAdr in the specified bank reaches the most significant address which is described in Chapter 4.2 Memory map. If the Word address is specified in USER bank and within “800h”~“EFFh”, the counter will not roll over to “000H” or “800h” but write operation will be executed until “EFFh” even if SCK is toggled when WordAdr reaches the most significant address “EFFh”.

The data will not be written into memory and error information will be written into SPI error information register for the following cases (Refer to Chapter 5.3.1).

1) This LSI is in Kill state
2) The specified address is in the protect area by Password
3) The specified MemBank is not User bank
4) WordAdr is over EFFh
5) The specified address is in the locked area

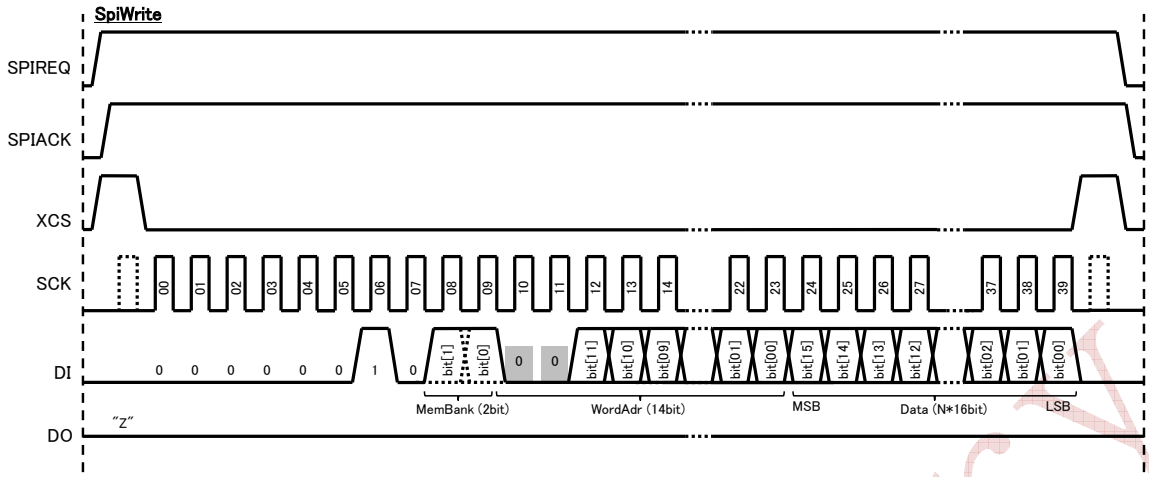


Figure 5.2.2 – SpiWrite command sequence

If part or all the words to be written are locked by BlockPermaLock or Lock command, or they are protected by AccessPassword or AreaPassword, any data cannot be written in those words but command is executed in the word that is not locked nor protected.

5.2.3 SpiRDSR

The SpiRDSR command is executed to read 16 bits data of error information register for SPI slave communication (refer to Chapter 5.3.1). The sequence for SpiRDSR command will be described in Figure 5.2.3.

The following data is input through DI pin synchronously to the rising edge of SCK after falling of XCS.

SpiRDSR operate-code (8bit：05h)

DO will output 16 bit error information register (Regarding to SPI slave communication) synchronously to the falling edge of SCK after the above data input. The read data will not be continued after XCS is rising and the output will be “Z” if XCS is rising with clock other than 16-cycle. Value of DI will be ignored when DO is being output. SpiRDSR command will end after XCS is raised.

DO will output “L” When XCS continue to output “L” after the 16bit error information register data is output from DO.

The data of 16bit error information register will be cleared after SpiRDSR command is executed.

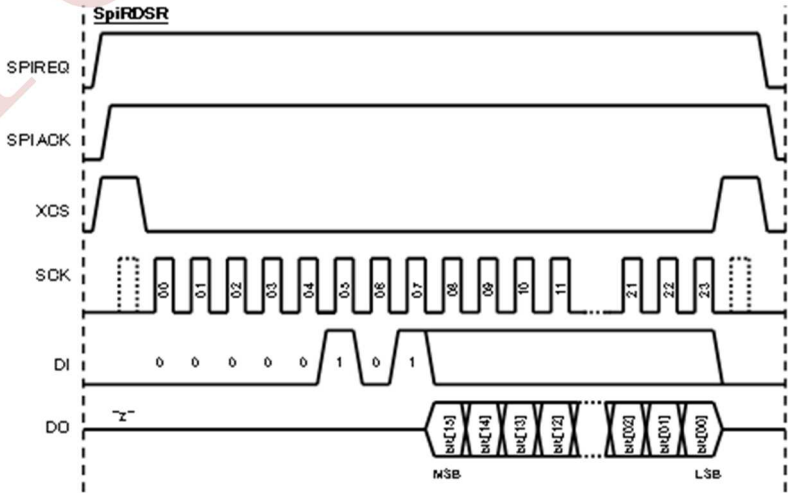


Figure 5.2.3 – SpiRDSR command sequence

5.3 Error handling to SPI slave communication

On SPI slave communication, an error occurs under the following condition. If an error occurs in SPIRead command operation, DO output will be “0” and error information will be stored in error information register.

・Specified memory are is locked.

・Killed status

The data stored in error information register can be read by SpiRDSR command.

5.3.1 Error information register (SPI slave communication)

Error information during SPI slave communication will be stored in the error information as shown in Table 5.3.1. These information can be read by SpiRDSR command.

The information will be cleared after the following operation.

・SpiRDSR command execution

・Power is off

Writing operation to error information register is ignored.

Table 5.3.1 Error information register format

Bit	Description
15	0 (Fixed)
14	0 (Fixed)
13	0 (Fixed)
12	0 (Fixed)
11	0 (Fixed)
10	0 (Fixed)
9	0 (Fixed)
8	0 (Fixed)
7	0 (Fixed)
6	0 (Fixed)
5	0 (Fixed)
4	0 (Fixed)
3	0 (Fixed)
2	0 (Fixed)
1	0: Normal 1: Specified address partly locked
0	0: Normal

6 Data protection

6.1 LOCK Command and BlockPermalock Command and Data protection area

This chapter describes the access control (hereinafter referred to as “Data protection”) for writing and reading memory. LOCK command can protect data in units of Bank except Reserved Bank. And Kill Password and Access Password stored in Reserved bank is protected. Area Password (refer to Chapter 6.2) stored in word address 20h-2Fh of Reserved bank are also protected by the same payload [7:6] of Lock command as Access Password protection.

Table 6.1.1 Memory bank and Lock/Block Permalock

MemBank	LOCK	WordAdr	BlockPermalock	Remarks
00:Reserved	payload[9:8]	00h-01h	—	Kill Password
	payload[7:6]	02h-03h	—	Access Password
		20h-2Fh	—	Area Password
01:EPC	payload[5:4]	all	—	
10:TID	payload[3:2]	all	—	
11:USER	payload[1:0]	000h-1FFh	Mask[15]	Area0
		200h-3FFh	Mask[14]	Area1
		400h-5FFh	Mask[13]	Area2
		600h-7FFh	Mask[12]	Area3
		800h-9FFh	Mask[11]	Area4
		A00h-BFFh	Mask[10]	Area5
		C00h-DFFh	Mask[9]	Area6
		E00h-EFFh	Mask[8]	Area7

Please refer to EPCglobal C1G2 Ver.1.2.0 6.3.2.11.3.9) for the action with combination of Lock command and BlockPermalock command.

6.2 Data Protection for USER bank

User bank is divided by 8 areas and each area can be access-controlled by Password Authentication.

6.2.1 AreaPassword setting

AreaPassword can be set into the WordPtr=20h-2Fh of Reserved bank (refer to Table 4.2.5) by Write command as described in Table 6.2.1. This command is executed only in Secured state.

Table 6.2.1 Write command (AreaPassword setting)

	Command	MemBank	WordPtr	Data	RN	CRC-16
Number of bits	8	2	EBV	16	16	16
Content	1100 0011	00:RSV	Starting Address Pointer (20h-2Fh)	RN16 Password to be set	Handle	

6.2.2 AreaPassword Authentication

AreaPassword authentication can be set into the WordPtr=30h-3Fh of Reserved bank (refer to Table 4.2.5) by Write command as described in Table 6.2.2. 16bit Password data will be sent twice for authentication as well as Access command. This command is executed only in Secured state.

Table 6.2.2 Write command(AreaPassword authentication)

	Command	MemBank	WordPtr	Data	RN	CRC-16
Number of bits	8	2	EBV	16	16	16
Content	1100 0011	00:RSV	Starting Address Pointer (30h-3Fh)	RN16 ⊗ (1/2 Password)	Handle	

When the authentication is failed, LSI will not respond as same as the failure case in authentication by Access command. When the authentication is succeeded, LSI transfers into AreaSecured state, and then the authenticated area will be readable and writeable.

If the Password is set to 0, this LSI will return to Secured state even if the LSI is in AreaSecured state.

The area authentication is only applied to one area each time. If reading from or writing into the other protected area, it is necessary to execute AreaPassword authentication command again once the LSI returns to Secured state.

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

Table 7.1 - Absolute Maximum Rating

Parameter	Symbol	Value			Unit	Conditions/Remarks
		MIN	TYP	MAX		
Maximum input voltage	Vmax	—	—	3.0	V	PWRP1-PWRM1,PWRP3-PWRM3
Power supply voltage	VDD	-0.5	—	+4.0	V	
Input voltage	VIN	-0.5	—	V_{DD}+0.5	V	
Output voltage	VOUT	-0.5	—	V_{DD}+0.5	V	
ESD voltage immunity	VESD	-	—	±1200	V	Human Body Model
Storage temperature	Tstg	-40	—	+85	℃	

7.2 Recommended Operation Conditions

Table 7.2 - Recommended Operation Conditions

Parameter	Symbol	Value			Unit	Conditions/Remarks
		MIN	TYP	MAX		
Operating ambient temperature	Ta	-40	—	+85	℃	
Retention guarantee temperature	Trtn1	-40	—	+85	℃	Retention guarantee period: 10years
RF communication						
Antenna input frequency	Fclk	860	—	960	MHz	According to the Radio Law
Reception modulation depth	(A-B)/A	80	90	100	%	
Receiving bit rate	F_fwd	26.7	—	128	kbps	PIE code: mark rate =1/2
Receiving waveform rise time	Tr	1	—	500	µs	
Receiving waveform settling time	Ts	—	—	1500	µs	

Receiving waveform fall time	Tf	1	—	500	µs	
SPI slave communication						
Power supply voltage	VDD	1.8	—	3.6	V	
level input voltage	VIH	V_{DD}−0.2	—	V_{DD} +0.3	V	
“L” level input voltage	VIL	−0.3	—	+0.4	V	

7.3 RF Communication Characteristics

Table 7.3 – RF Communication Characteristics

Parameter	Symbol	Value			Unit	Conditions/Remarks
		MIN	TYP	MAX		
Minimum operating power when reading	PR_MIN	—	-11	—	dBm	Measured for bare die Tari=25USERTcal=3Tari,TRcal=2.6RTcal, DR=8,FM0,BLF=41kbps, DSB-ASK, Modulation depth==90% memory access length≦6Word (※1)
Minimum operating power when writing	PW_MIN	—	-11	—	dBm	
Maximum operating power	PMAX		+20		dBm	
Equivalent input capacitance	CP	—	0.8	—	pF	Input power= -11dBm, parallel model (At 920MHz)
		—	3.2	—	pF	Input power= +6dBm, parallel model (At 920MHz)
Equivalent input resistance	RP	—	3.6	—	KΩ	Input power= -11dBm, parallel model (At 920MHz)
		—	0.19	—	KΩ	Input power= +6dBm, parallel model (At 920MHz)
Returning bit rate	F_rtrn	40		640	kbps	

※1These characteristics are the values for the standalone LSI, and do not specify the values when the LSI is connected to other circuits such as a microcomputer.

7.4 SPI Slave Communication

7.4.1 DC Characteristics

Table 7.4.1 – DC Characteristics

Parameter		Symbol	Value			Unit	Conditions
			MIN	TYP	MAX		
Input leakage current		ILI	—	—	±5	μA	VIN = VDD (SPIREQ pin)
			—	—	±1	μA	VIN = 0V (SPIREQ pin) VIN = 0V ～ VDD (the other pins※1)
Output leakage current		ILO	—	—	±1	μA	VOUT = 0V ～ VDD, when output is Z(output pin ※2)
Power supply	ICC	ICC	—	70	200	μA	SCK = 2MHz, Vdd=3.0V
	IPD1	IPD1	—	1	10	μA	SPIREQ ＝ 0V or open No RF reception
	ISB	ISB	—	10	30	μA	SPIREQ ＝ VDD XCS=VDD
Iutput voltage at “H” level		VIH	VDD×0.7	—	VDD +0.5	V	※3
Iutput voltage at “L” level		VIL	−0.5	—	VDD×0.3	V	※3
Output voltage at “H” level		VOH	VDD−0.5	—	VDD	V	IOH＝−2mA ※2
Output voltage at “L” level		VOL	0	—	0.4	V	IOL＝ 2mA ※2
SPI pin pull-down resistance		RIN	0.8	1	1.2	MΩ	VIN = VDD SPIREQ Pin

※1：XCS、SCK、DI Pin ※2：DO、SPIACK Pin ※3：SPIREQ、XCS、SCK、DI Pin

7.4.2 AC Characteristics

Table 7.4.2 – AC Characteristics

Parameter	Symbol	Value			Unit	Pin
		MIN	TYP	MAX		
SCK clock frequency	f_{CK}	—	—	2	MHz	SCK
Clock high time	t_{CH}	200	—	—	ns	SCK
Clock low time	t_{CL}	200	—	—	ns	SCK
Chip select set time	t_{CSU}	60	—	—	ns	XCS,SCK
Chip select hold time	t_{CSH}	20	—	—	ns	XCS,SCK
Output enable time	t_{ODLZ}	20			ns	DO,SCK
Output disable time	t_{ODz}	—	—	60	ns	DO,SCK
Output data valid time	t_{ODV}	—	—	80	ns	DO,XCS
Output hold time	t_{OH}	0	—	—	ns	DO,SCK

Deselect time	t_D	230	—	—	ns	XCS
Data rise time	t_R	—	—	5	ns	DI,XCS,SPIREQ
Data fall time	t_F	—	—	5	ns	DI,XCS,SPIREQ
Data set up time	t_{DIS}	20	—	—	ns	DI,SCK
Data hold time	T_{DIH}	20	—	—	ns	DI,SCK

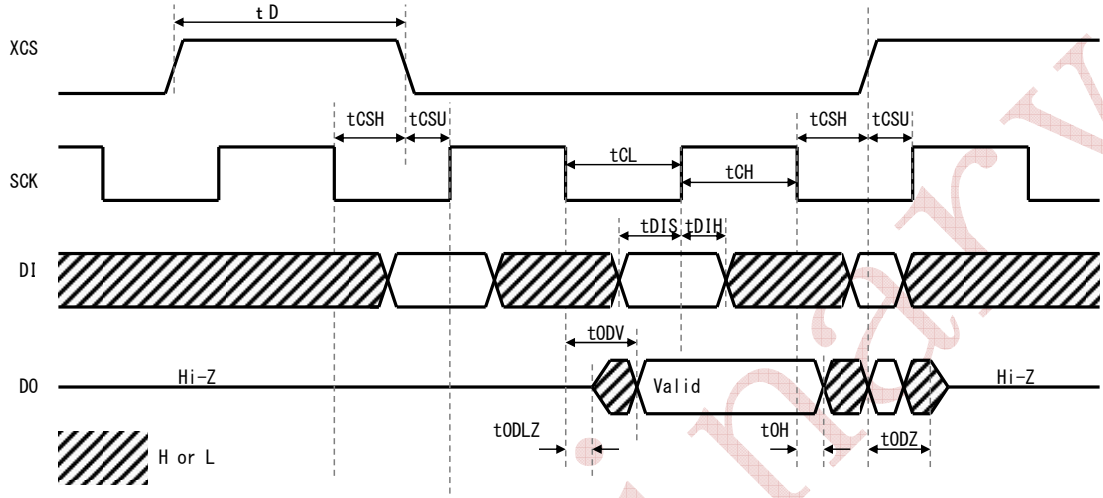


Figure7.4.2 – SPI slave timing

7.4.3 Power Sequence for SPI Slave Communication Mode

The power sequence in SPI slave communication mode is shown in Figure7.4.3.1 (with VDD off control), and Figure 7.4.3.2 (without VDD off control).

Assert SPIREQ after asserting VDD for communication start. “H” will be output to SPIACK pin for tOAV duration time after asserting SPIREQ. Set XCS to “H” within the period of tCUS from rising edge of SPIACK after asserting SPIREQ. Wait tPU after confirming “H” of SPIACK and release XCS and then SPI slave communication can be started.

Set SPIREQ to “L” in more than tPD period after asserting XCS. The output of SPIACK will be “L” in tOHA after SPIREQ input becomes “L”. It is recommended to set XCS input “L” within the period of tCHS from the falling edge of SPIACK. In order to turn off VDD, it is recommended to wait more than tPH period after outputting “L” to SPIACK.

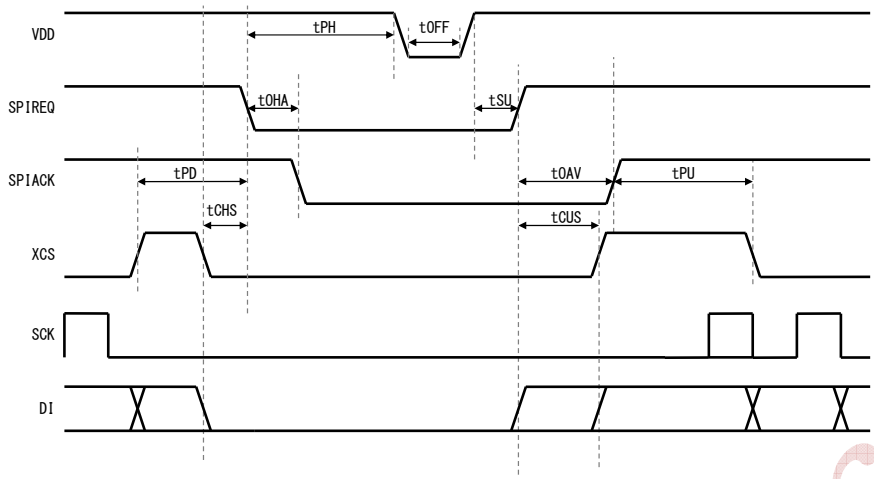


Figure 7.4.3.1 Power sequence (with VDD off control)

Table 7.4.3 Timing specifications during SPI slave communication

Parameter	Symbol	Value			Unit
		MIN	TYP	MAX	
SPIREQ rising start time	tSU	500	—	—	µs
SPIREQ low time	tRQL	1000	—	—	µs
Power hold time	tPH	0	—	—	µs
XCS level hold time at power ON	tPU	10	—	—	µs
XCS level hold time at power OFF	tPD	1	—	—	µs
Power off time	tOFF	1000	—	—	µs
Output SPIACK definite time	tOAV	1	—	20000	µs
Output SPIACK hold time	tOHA	5	—	10000	µs
XCS setup time(start)	tCUS	—	—	1	µs
XCS hold time(start)	tCHS	—	—	1	µs

If the device does not operate within the specified conditions of cycle or power on/off sequence, memory data cannot be guaranteed.

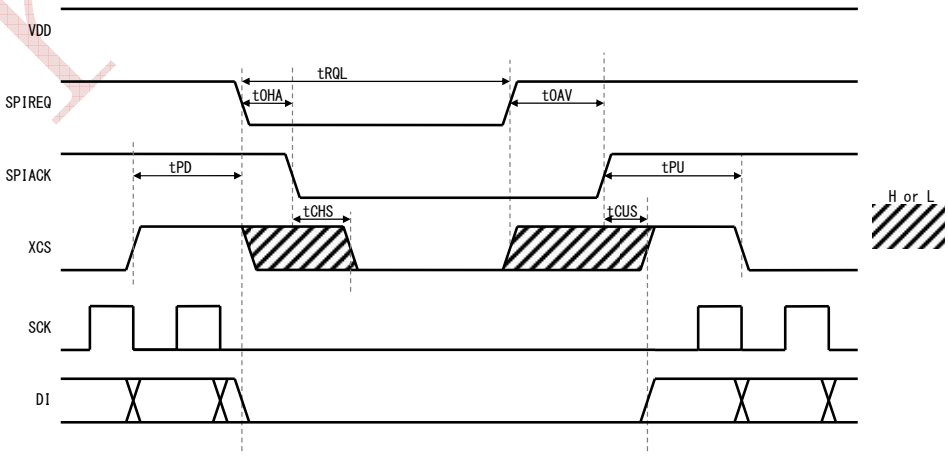
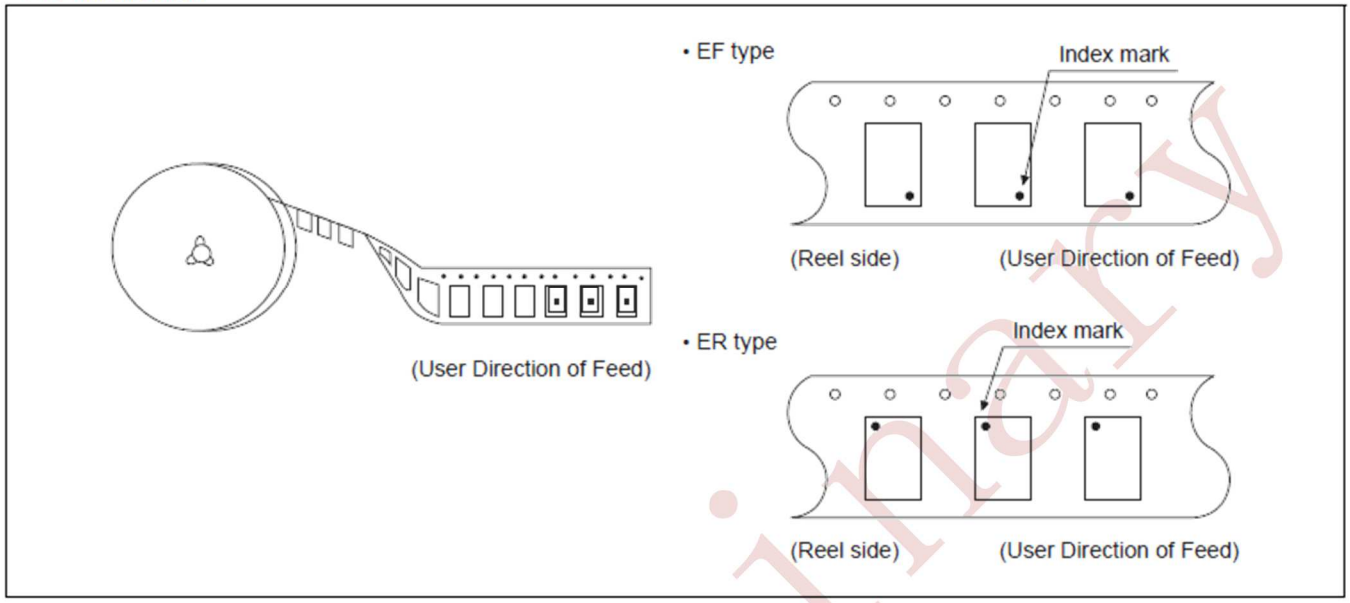


Figure 7.4.3.2 Power sequence (without VDD off control)

8 Ordering Information

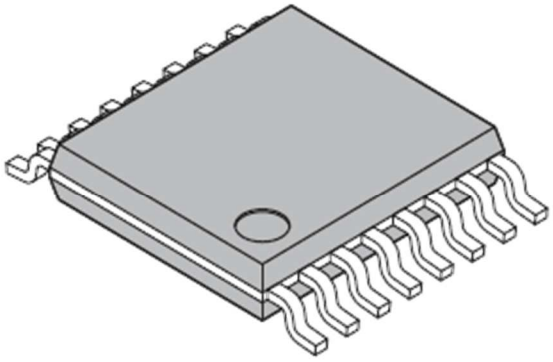
Part Number	Interface	Shipping form	Wafer thickness	Remarks
MB97R8120-DIAB15	RF	Sawn wafer	150µm±22.54µm	
MB97R8130PFT-G-JNERE1	RF+SPI	TSSOP16 (Tape & Reel)	-	EF type*
MB97R8130PFT-G-JNEFE1	RF+SPI		-	ER type*

* : IC orientation



Package Dimension

16-pin plastic TSSOP

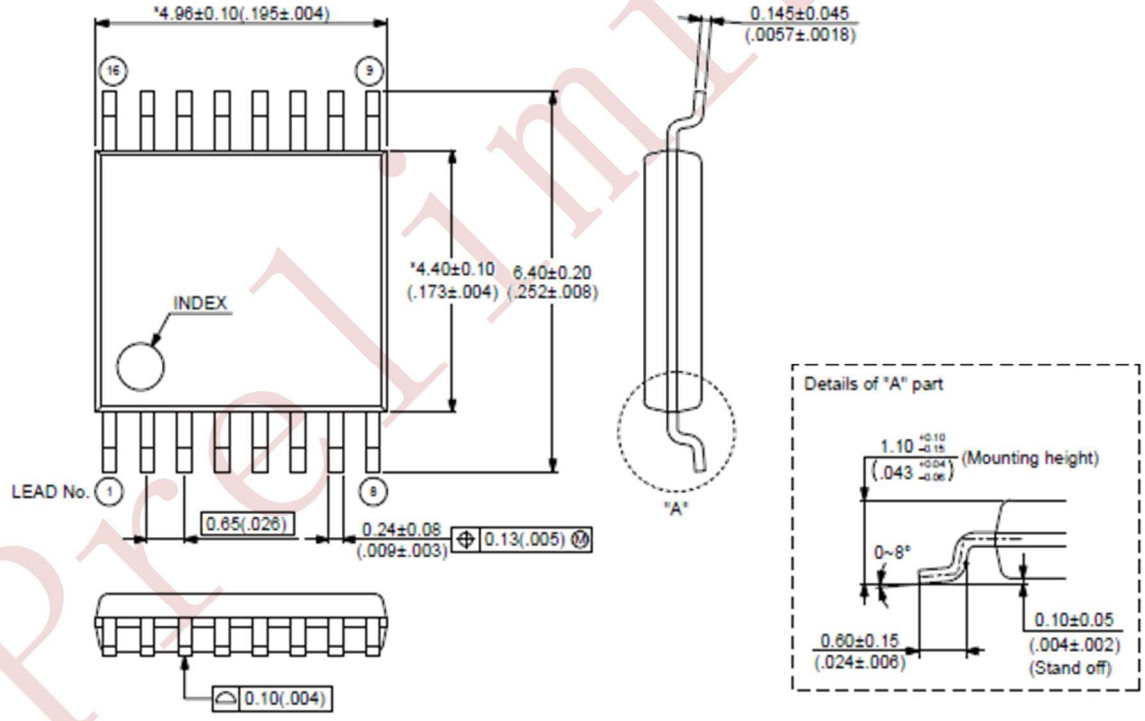


(FPT-16P-M08)

Lead pitch	0.65 mm
Package width × package length	4.40 mm × 4.96 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.20 mm Max
Weight	0.06 g

16-pin plastic TSSOP
(FPT-16P-M08)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) * : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

9 Others

9.1 Note items

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