

Memory FRAM

8 M (512 K × 16) Bit

MB85R8M2T

■ DESCRIPTIONS

The MB85R8M2T is an FRAM (Ferroelectric Random Access Memory) chip consisting of 524,288 words × 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

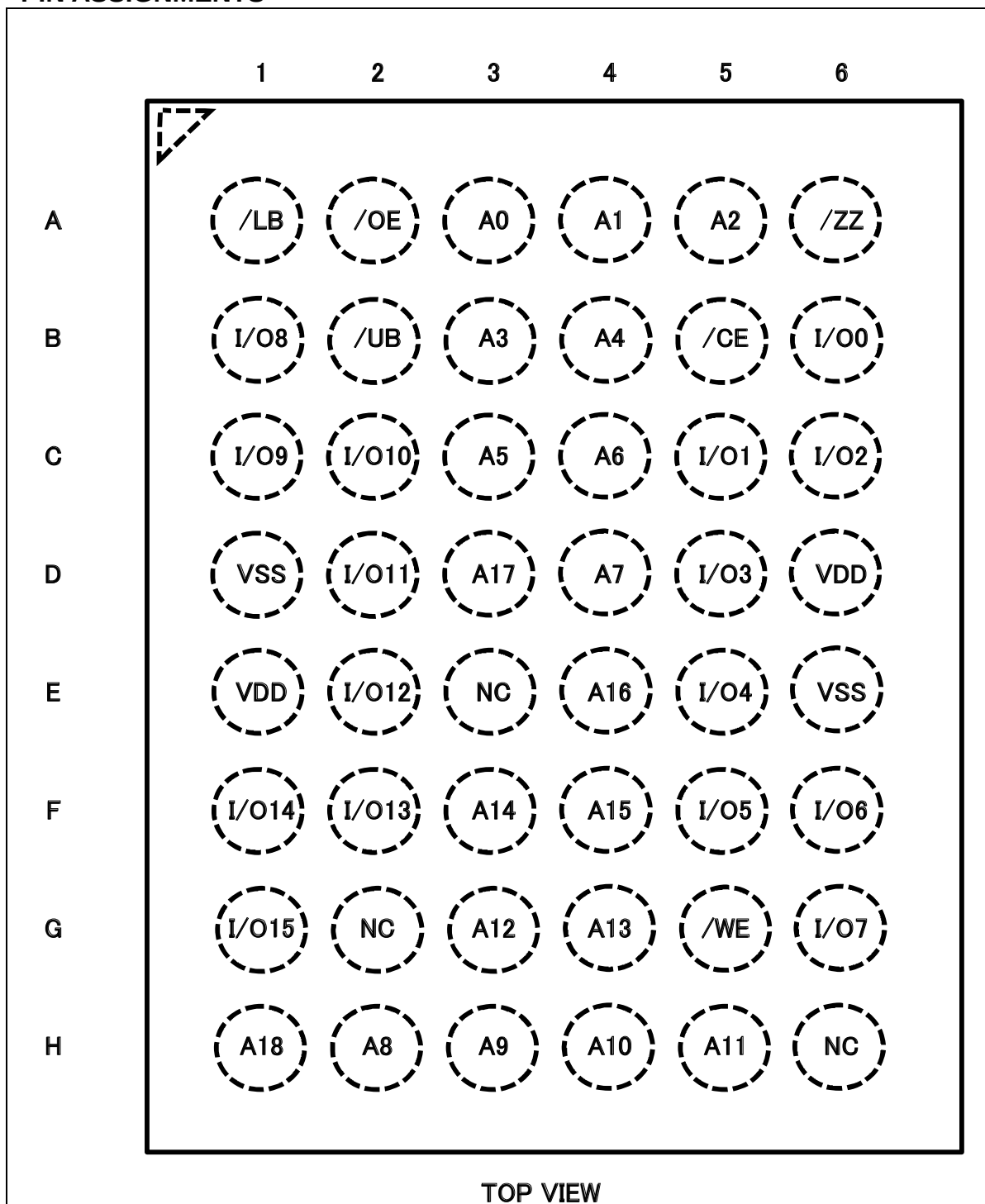
The MB85R8M2T is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85R8M2T can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E2PROM. The MB85R8M2T uses a pseudo-SRAM interface.

■ FEATURES

- Bit configuration : 524,288 words × 16 bits
- Read/write endurance : 10^{13} times / 16 bits
- Data retention : 10 years (+ 85 °C), 95 years (+ 55 °C), over 200 years (+ 35 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power operation : Operating power supply current 20 mA (Max)
Standby current 300 μA (Max)
Sleep current 40 μA (Max)
- Operation ambient temperature range : - 40 °C to + 85 °C
- Package : 48-pin plastic FBGA (BGA-48P-M24)
RoHS compliant

■ PIN ASSIGNMENTS



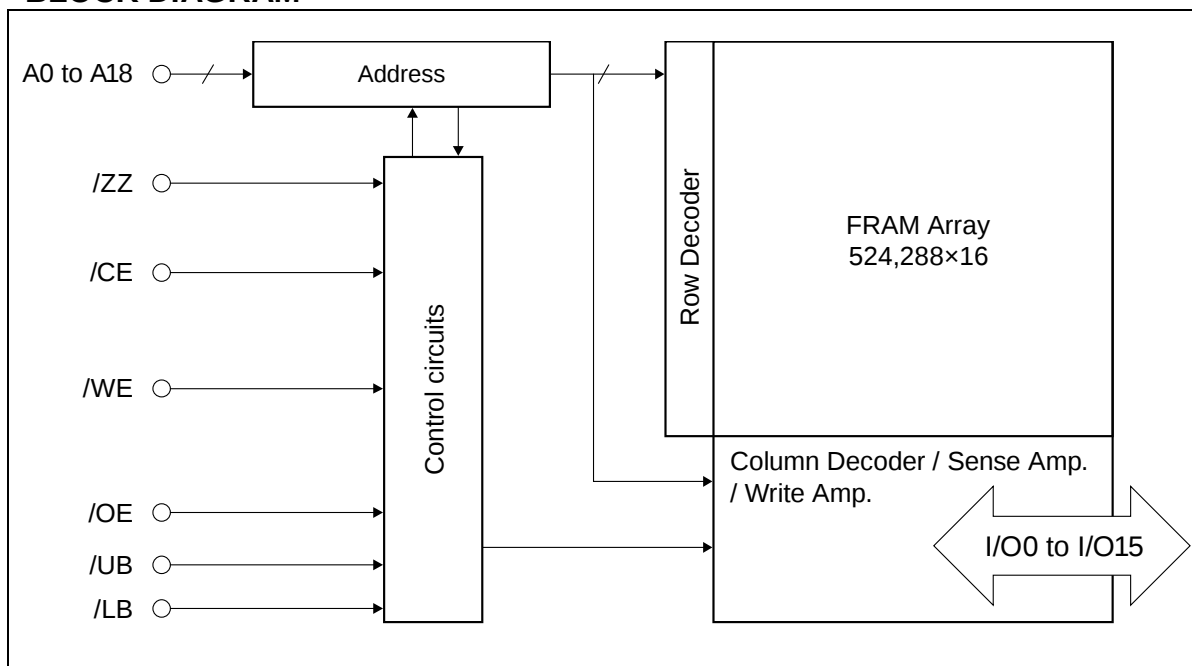
■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
A3,A4,A5,B3,B4,C3, C4,D4,H2,H3,H4,H5, G3,G4,F3,F4,E4,D3, H1	A0 to A18	Address Input pins Select 524,288 words in FRAM memory array by 19 Address Input pins. When these address inputs are changed during /CE equals to “L” level, reading operation of data selected in the address after transition will start.
B6,C5,C6,D5,E5,F5, F6,G6,B1,C1,C2,D2 E2,F2,F1,G1	I/O0 to I/O15	Data Input/Output pins These are 16 bits bidirectional pins for reading and writing.
B5	/CE	Chip Enable Input pin In case the /CE equals to “L” level and /ZZ equals to “H” level, device is activated and enables to start memory access. In writing operation, input data from I/O pins are latched at the rising edge of /CE and written to FRAM memory array.
G5	/WE	Write Enable Input pin Writing operation starts at the falling edge of /WE. Input data from I/O pins are latched at the rising edge of /WE and written to FRAM memory array.
A2	/OE	Output Enable Input pin When the /OE is “L” level, valid data are output to data bus. When the /OE is “H” level, all I/O pins become high impedance (High-Z) state.
A6	/ZZ	Sleep Mode Input pin When the /ZZ becomes to “L” level, device transits to the Sleep Mode. During reading and writing operation, /ZZ pin shall be hold “H” level.
A1,B2	/LB, /UB	Lower/Upper byte Control Input pins In case /LB or /UB equals to “L” level, it enables reading/writing operation of I/O0 to I/O7 or I/O8 to I/O15 respectively. In case /LB and /UB equal to “H” level, all I/O pins become High-Z state.
D6,E1	VDD	Supply Voltage pins Connect all two pins to the power supply.
D1,E6	VSS	Ground pins Connect all two pins to ground.

Note: Please refer to the timing diagram for functional description of each pin.

MB85R8M2T

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Operation Mode	/CE	/WE	/OE	A0 to A17	/ZZ
Sleep	×	×	×	×	L
Standby	H	×	×	×	H
Read	↓	H	L	H or L	H
Address Access Read	L	H	L	↑ or ↓	H
Write(/CE Control)*1	↓	L	×	H or L	H
Write(/WE Control)*1*2	L	↓	×	H or L	H
Address Access Write*1*3	L	↓	×	↑ or ↓	H
Pre-charge	↑	×	×	×	H

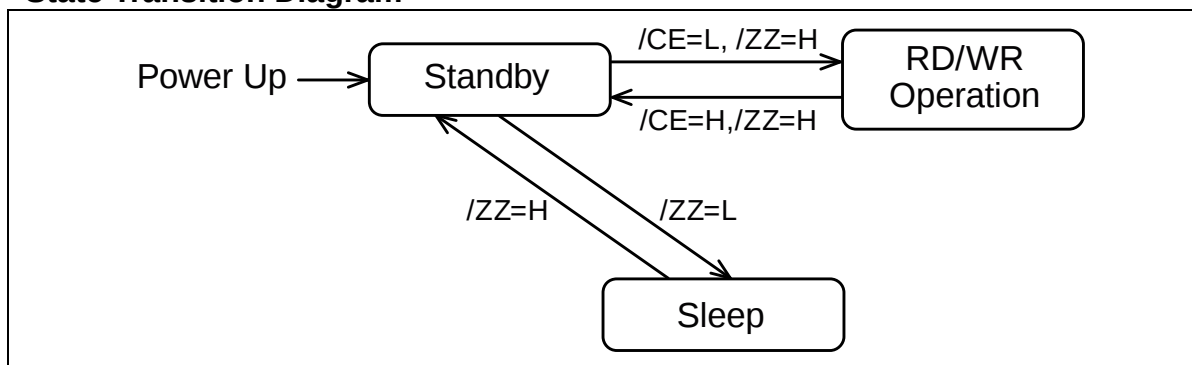
Note: H= "H" level, L= "L" level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑

*1: In writing cycle, input data is latched at early rising edge of /CE or /WE.

*2: In writing sequence of /WE control, there exists time with data output of reading cycle at the falling edge of /CE.

*3: In writing sequence of Address Access Write, there exists time with data output of reading cycle at the address transition.

■ State Transition Diagram



■ FUNCTIONAL TRUTH TABLE OF BYTE CONTROL

Operation Mode	/WE	/OE	/LB	/UB	I/O0 to I/O7	I/O8 to I/O15
Read(Without Output)	H	H	×	×	Hi-Z	Hi-Z
	H	×	H	H	Hi-Z	Hi-Z
Read(I/O8 to I/O15)	H	L	H	L	Hi-Z	Output
Read(I/O0 to I/O7)			L	H	Output	Hi-Z
Read(I/O0 to I/O15)			L	L	Output	Output
Write(I/O8 to I/O15)	↑	×	H	L	×	Input
Write(I/O0 to I/O7)			L	H	Input	×
Write(I/O0 to I/O15)			L	L	Input	Input

Note: H= "H" level, L= "L" level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑
Hi-Z= High Impedance

In case the byte reading or writing are not selected, /LB and /UB pins shall be connected to GND pin.
In case the byte writing, while /CE=L, please don't switch /LB and /UB.

■ ABABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V _{DD}	− 0.5	+ 4.0	V
Input Pin Voltage*	V _{IN}	− 0.5	V _{DD} + 0.5 (≤ 4.0)	V
Output Pin Voltage*	V _{OUT}	− 0.5	V _{DD} + 0.5 (≤ 4.0)	V
Operation Ambient Temperature	T _A	− 40	+ 85	°C
Storage Temperature	T _{stg}	− 55	+ 125	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage* ¹	V _{DD}	1.8	3.3	3.6	V
Operation Ambient Temperature* ²	T _A	− 40	—	+ 85	°C

*1: All voltages are referenced to VSS (ground 0 V).

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$ I_{LI} $	$V_{IN} = 0V \text{ to } V_{DD}$	—	—	5	μA
Output Leakage Current	$ I_{LO} $	$V_{OUT} = 0V \text{ to } V_{DD}$ $/CE = V_{IH} \text{ or } /OE = V_{IH}$	—	—	5	μA
Operating Power Supply Current*1	I_{DD}	$/CE = 0.2V, I_{out} = 0mA$	—	15	20	mA
Standby Current	I_{SB}	$/ZZ \geq V_{DD} - 0.2V$ $/CE, /WE, /OE \geq V_{DD} - 0.2V$ $/LB, /UB \geq V_{DD} - 0.2V$ Others $\geq V_{DD} - 0.2V \text{ or } \leq 0.2V$	—	60	300	μA
Sleep Current	I_{ZZ}	$/ZZ = V_{SS}$ $/CE, /WE, /OE \geq V_{DD} - 0.2V$ $/LB, /UB \geq V_{DD} - 0.2V$ Others $\geq V_{DD} - 0.2V \text{ or } \leq 0.2V$	—	10	40	μA
High Level Input Voltage	V_{IH}	$V_{DD} = 1.8V \text{ to } 3.6V$	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
Low Level Input Voltage	V_{IL}	$V_{DD} = 1.8V \text{ to } 3.6V$	-0.3	—	$V_{DD} \times 0.17$	V
High Level Output Voltage	V_{OH1}	$V_{DD} = 2.7V \text{ to } 3.6V$ $I_{OH} = -1.0mA$	$V_{DD} \times 0.8$	—	—	V
	V_{OH2}	$V_{DD} = 1.8V \text{ to } 2.7V$ $I_{OH} = -100\mu A$	$V_{DD} - 0.2$	—	—	
Low Level Output Voltage	V_{OL1}	$V_{DD} = 2.7V \text{ to } 3.6V$ $I_{OL} = 2.0mA$	—	—	0.4	V
	V_{OL2}	$V_{DD} = 1.8V \text{ to } 2.7V$ $I_{OL} = 150\mu A$	—	—	0.2	

*1: During the measurement of I_{DD} , all Address and I/O were taken to only change once per active cycle.

I_{out} : output current

MB85R8M2T

2. AC Characteristics

▪ AC Test Conditions

Power Supply Voltage	: 1.8 V to 3.6 V
Operation Ambient Temperature	: - 40 °C to + 85 °C
Input Voltage Amplitude	: 0 V / V_{DD}
Input Rising Time	: 3 ns
Input Falling Time	: 3 ns
Input Evaluation Level	: $V_{DD}/2$
Output Evaluation Level	: $V_{DD}/2$
Output Load Capacitance	: 30 pF

(1) Read Cycle

Parameter	Symbol	Value ($V_{DD}=1.8V$ to $2.7V$)		Value ($V_{DD}=2.7V$ to $3.6V$)		Unit
		Min	Max	Min	Max	
Read Cycle time	t_{RC}	185	—	150	—	ns
/CE Access Time	t_{CE}	—	95	—	75	ns
Address Access Time	t_{AA}	—	185	—	150	ns
/CE Output Data Hold time	t_{OH}	0	—	0	—	ns
Address Access Output Data Hold time	t_{OAH}	20	—	20	—	ns
/CE Active Time	t_{CA}	95	—	75	—	ns
Pre-charge Time	t_{PC}	90	—	75	—	ns
/LB, /UB Access Time	t_{BA}	—	35	—	20	ns
Address Setup Time	t_{AS}	5	—	5	—	ns
Address Hold Time	t_{AH}	95	—	75	—	ns
/CE↑ to Address Transition time* ¹	t_{CAH}	5	—	5	—	ns
/OE Access Time	t_{OE}	—	35	—	20	ns
/CE Output Floating Time* ¹	t_{HZ}	—	10	—	10	ns
/OE Output Floating Time	t_{OHZ}	—	10	—	10	ns
/LB, /UB Output Floating Time	t_{BHZ}	—	10	—	10	ns
Address Transition Time* ¹	t_{AX}	—	15	—	15	ns

*1: Same parameters with the Write cycle.

MB85R8M2T

(2) Write Cycle

Parameter	Symbol	Value (V _{DD} =1.8V to 2.7V)		Value (V _{DD} =2.7V to 3.6V)		Unit
		Min	Max	Min	Max	
Write Cycle Time	t _{WC}	185	—	150	—	ns
/CE Active Time	t _{CA}	95	—	75	—	ns
/CE↓ to /WE↑ Time	t _{CW}	95	—	75	—	ns
Pre-charge Time	t _{PC}	90	—	75	—	ns
Write Pulse Width	t _{WP}	20	—	20	—	ns
Address Setup Time	t _{AS}	5	—	5	—	ns
Address Hold Time	t _{AH}	95	—	75	—	ns
/CE↑ to Address Transition time	t _{CAH}	5	—	5	—	ns
/WE↓ to /CE↑ Time	t _{WLC}	20	—	20	—	ns
Address Transition to /WE↑ Time	t _{AWH}	185	—	150	—	ns
/WE↑ to Address Transition Time	t _{WHA}	0	—	0	—	ns
/LB, /UB Setup Time	t _{BS}	2	—	2	—	ns
/LB, /UB Hold Time	t _{BH}	0	—	0	—	ns
Data Setup Time	t _{DS}	10	—	10	—	ns
Data Hold Time	t _{DH}	0	—	0	—	ns
/WE Output Floating Time	t _{WZ}	—	10	—	10	ns
/WE Output Access Time*1	t _{WX}	10	—	10	—	ns
Write Setup Time*1	t _{WS}	0	—	0	—	ns
Write Hold Time*1	t _{WH}	0	—	0	—	ns

*1: Writing operation applies “Write Cycle Timing 1” or “Write Cycle Timing 2” by the relation of /CE and /WE timing. The values of t_{WX}, t_{WS} and t_{WH} are defined by these operations. The conditions of t_{WS} and t_{WH} are not checked at shipping test.

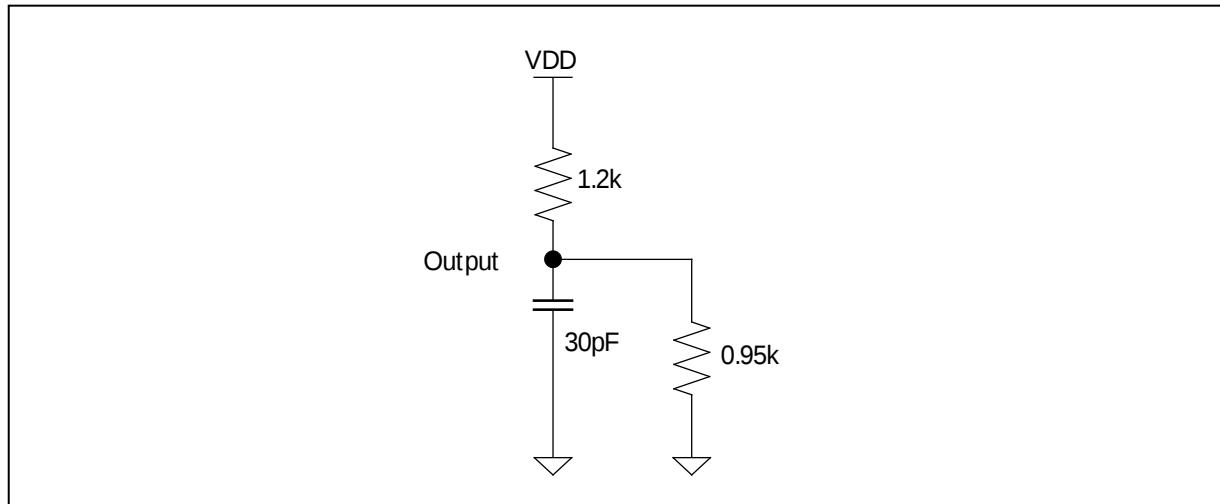
(3) Power ON/OFF Sequence and Sleep Mode Cycle

Parameter	Symbol	Value		Unit
		Min	Max	
/CE level hold time for Power ON	t _{PU}	450	—	μs
/CE level hold time for Power OFF	t _{PD}	85	—	ns
Power supply rising time	t _{VR}	50	—	μs/V
Power supply falling time	t _{VF}	100	—	μs/V
/ZZ active time	t _{ZZL}	1	—	μs
Sleep mode enable time	t _{ZZEN}	—	0	μs
/CE level hold time for Sleep mode release	t _{ZZEX}	450	—	μs

3. Pin Capacitance

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	$V_{DD} = 3.3\text{ V}$, $f = 1\text{ MHz}$, $T_A = +25\text{ }^{\circ}\text{C}$	—	—	9	pF
Input/Output Capacitance (I/O pin)	$C_{I/O}$		—	—	9	pF
/ZZ Pin Input Capacitance	C_{ZZ}		—	—	9	pF

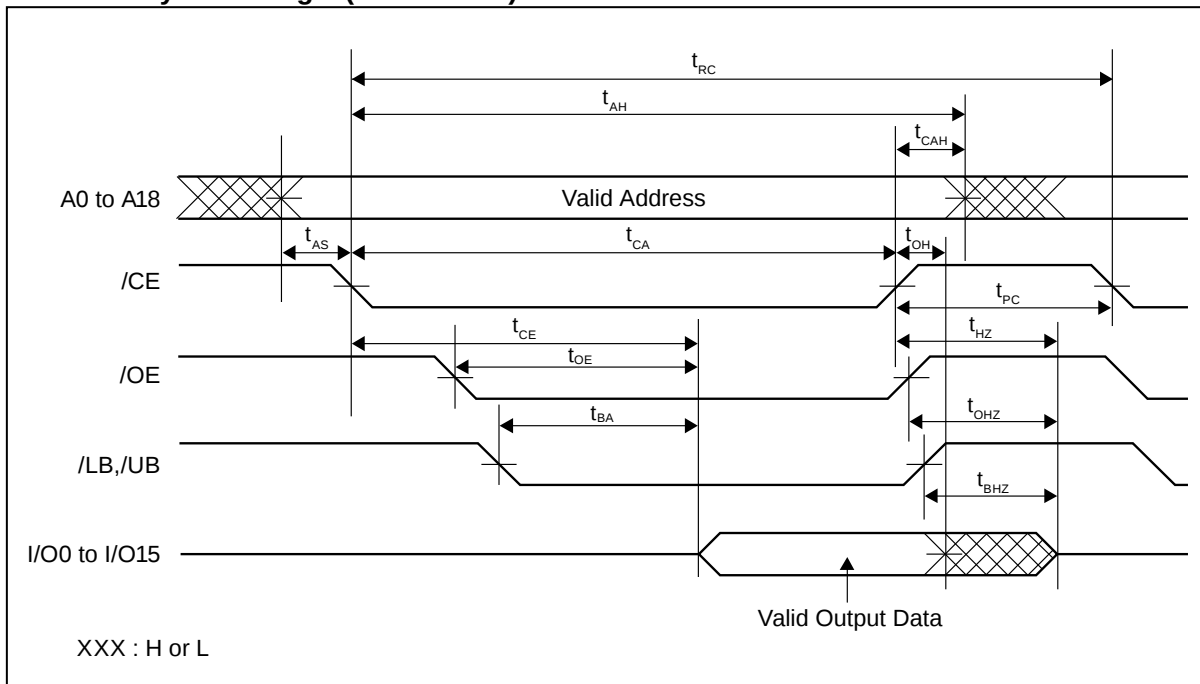
■ AC Test Load Circuit



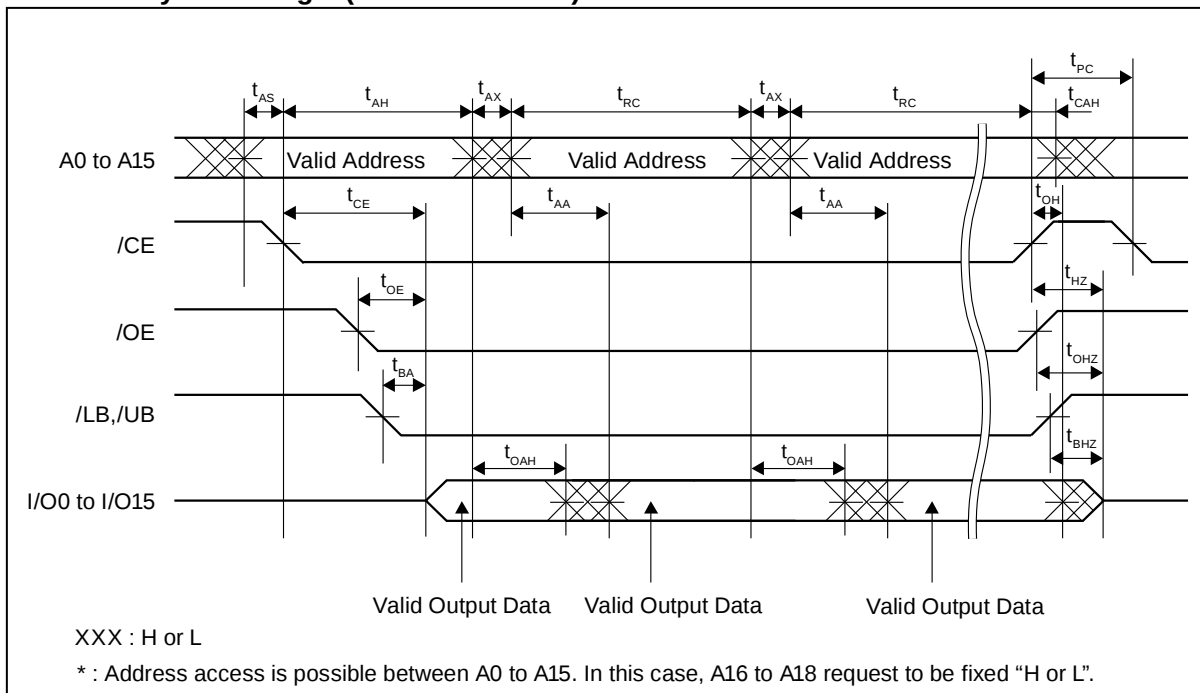
MB85R8M2T

■ TIMING DIAGRAMS

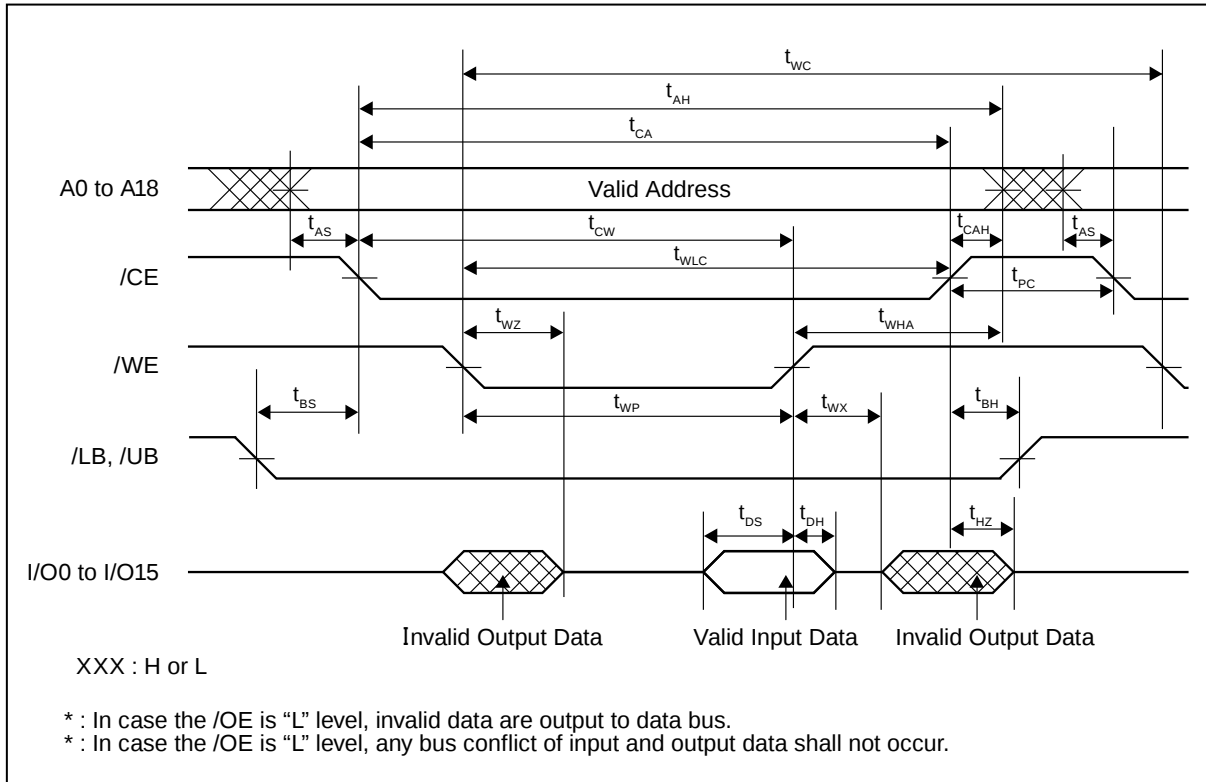
1. Read Cycle Timing 1 (/CE Control)



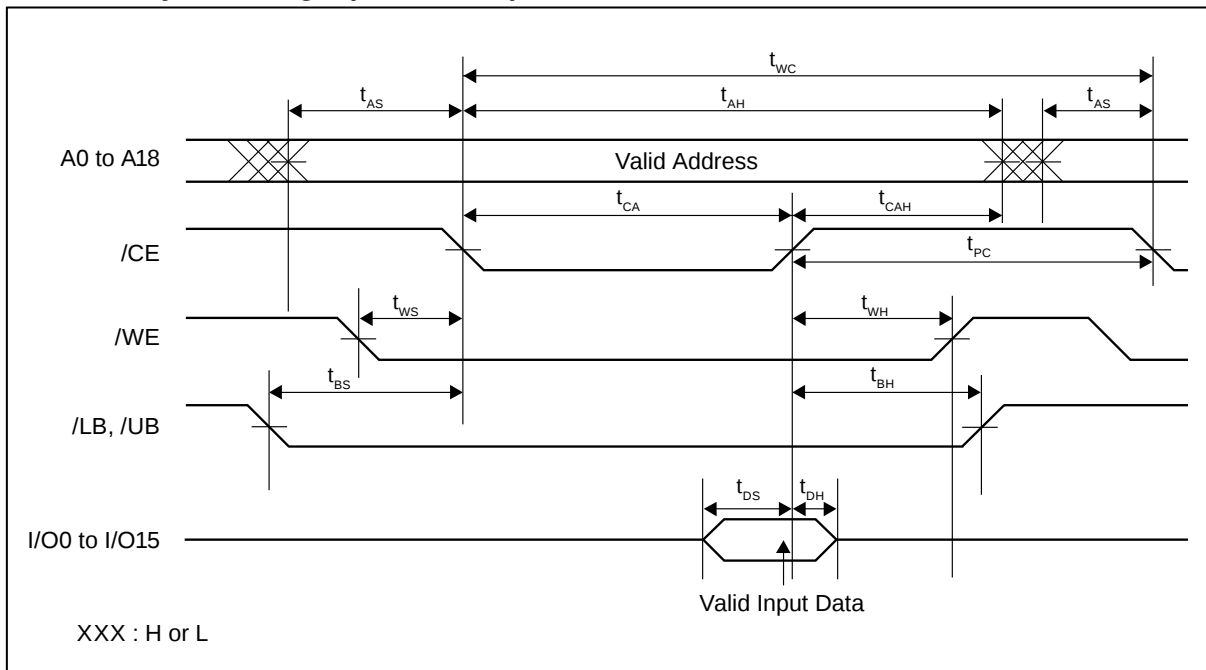
2. Read Cycle Timing 2 (Address Access)



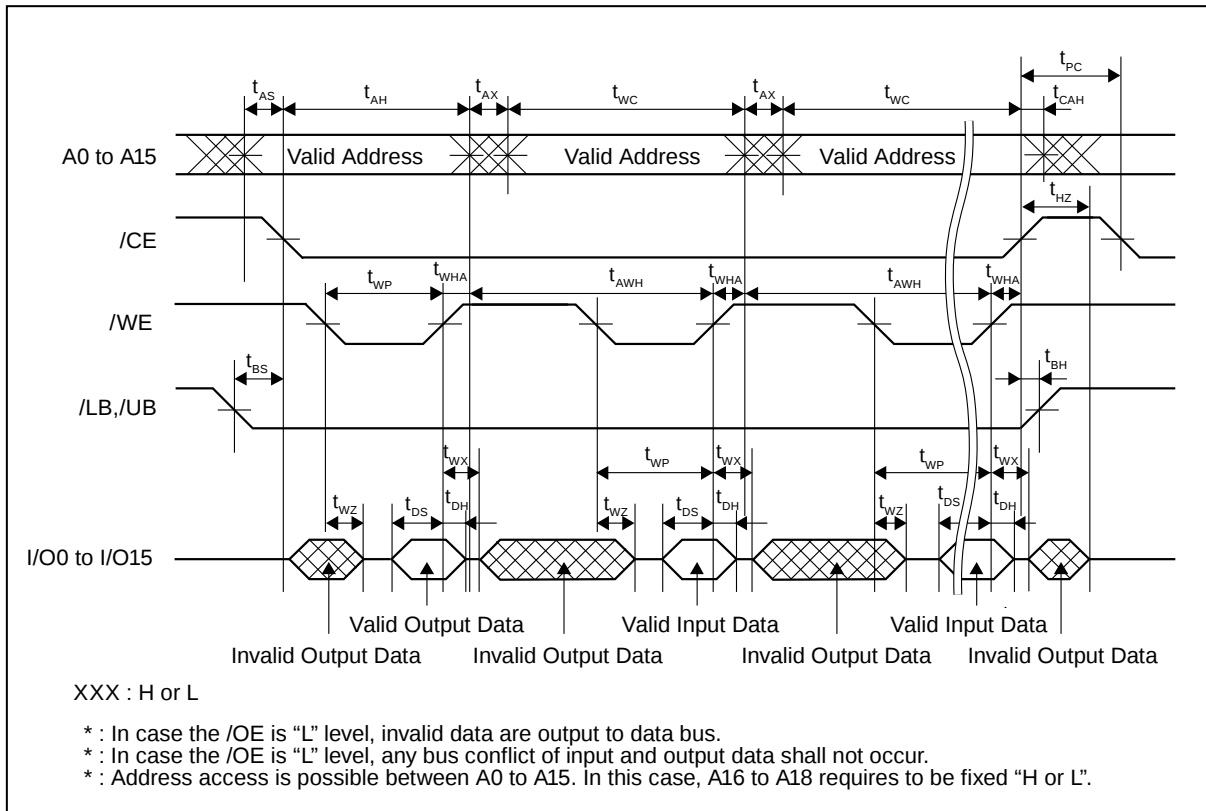
3. Write Cycle Timing 1 (/WE Control)



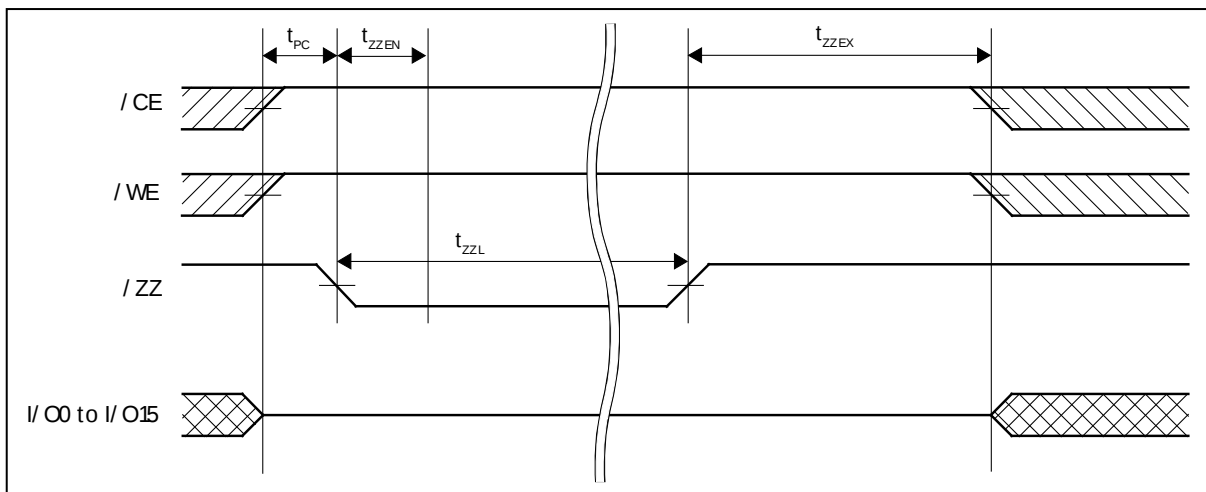
4. Write Cycle Timing 2 (/CE Control)



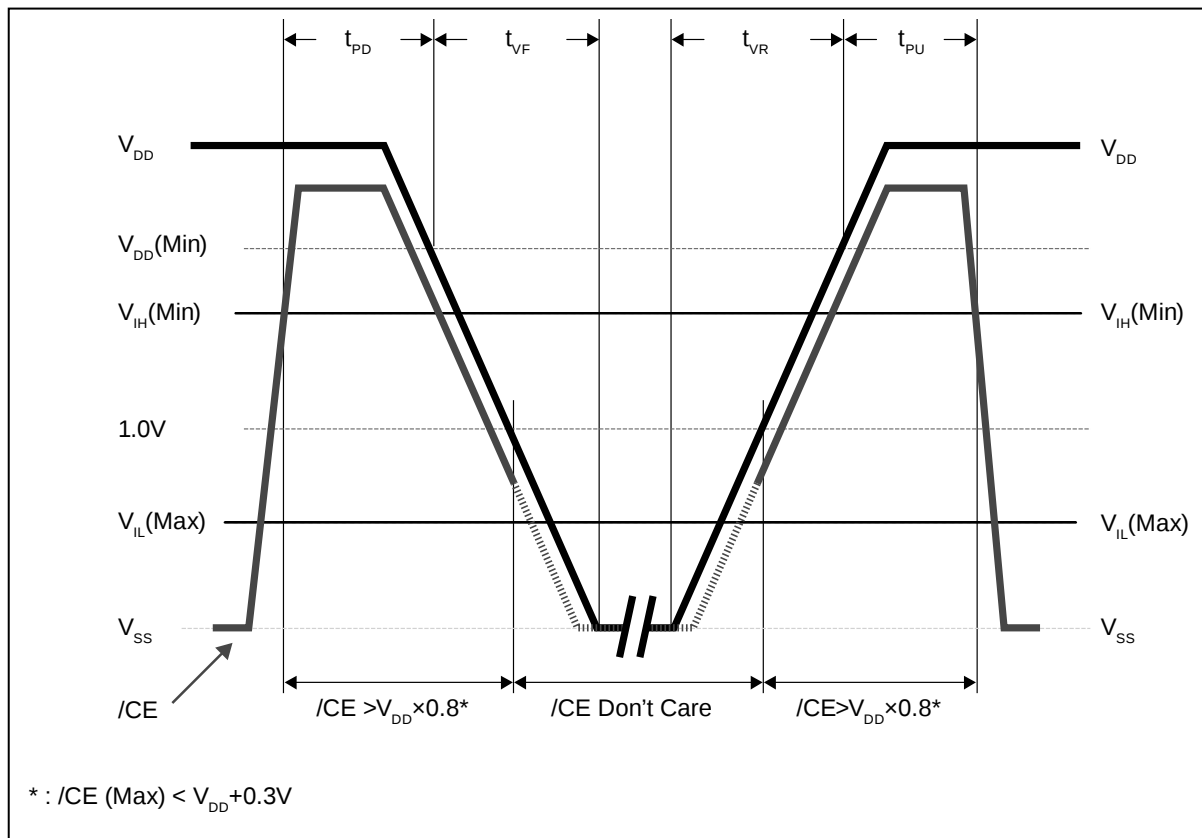
5. Write Cycle Timing 3 (Address Access and /WE Control)



6. Sleep Mode Timing



■ POWER ON/OFF SEQUENCE



■ FRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance* ¹	10^{13}	—	Times/16 bits	Operation Ambient Temperature $T_A = +85\text{ }^{\circ}\text{C}$
Data Retention* ²	10	—	Years	Operation Ambient Temperature $T_A = +85\text{ }^{\circ}\text{C}$
	95	—		Operation Ambient Temperature $T_A = +55\text{ }^{\circ}\text{C}$
	≥ 200	—		Operation Ambient Temperature $T_A = +35\text{ }^{\circ}\text{C}$

*1: Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

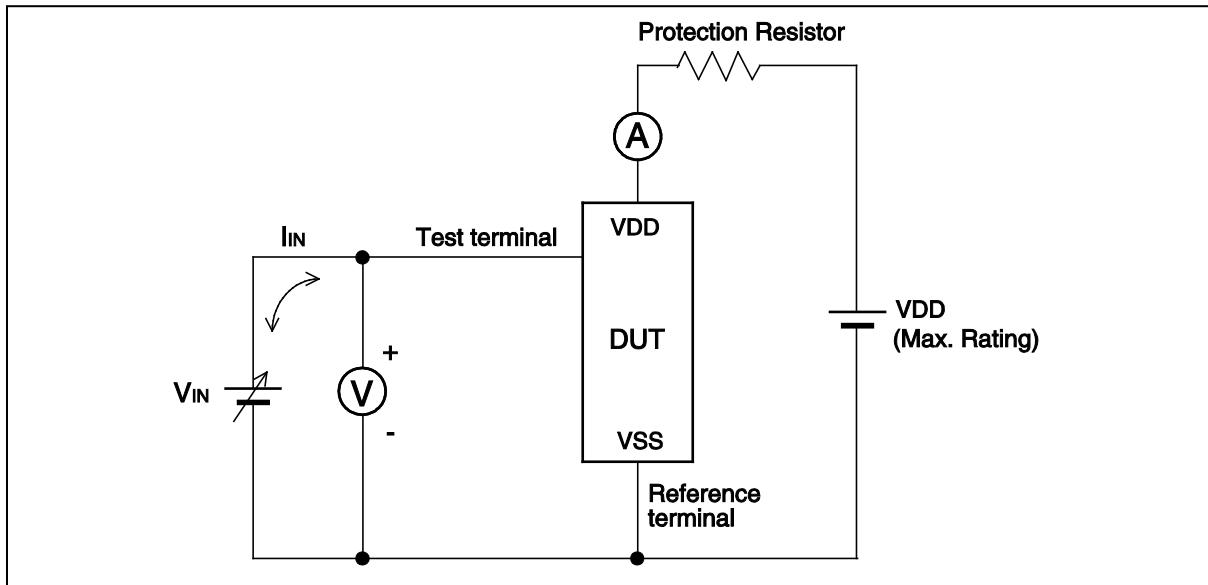
■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

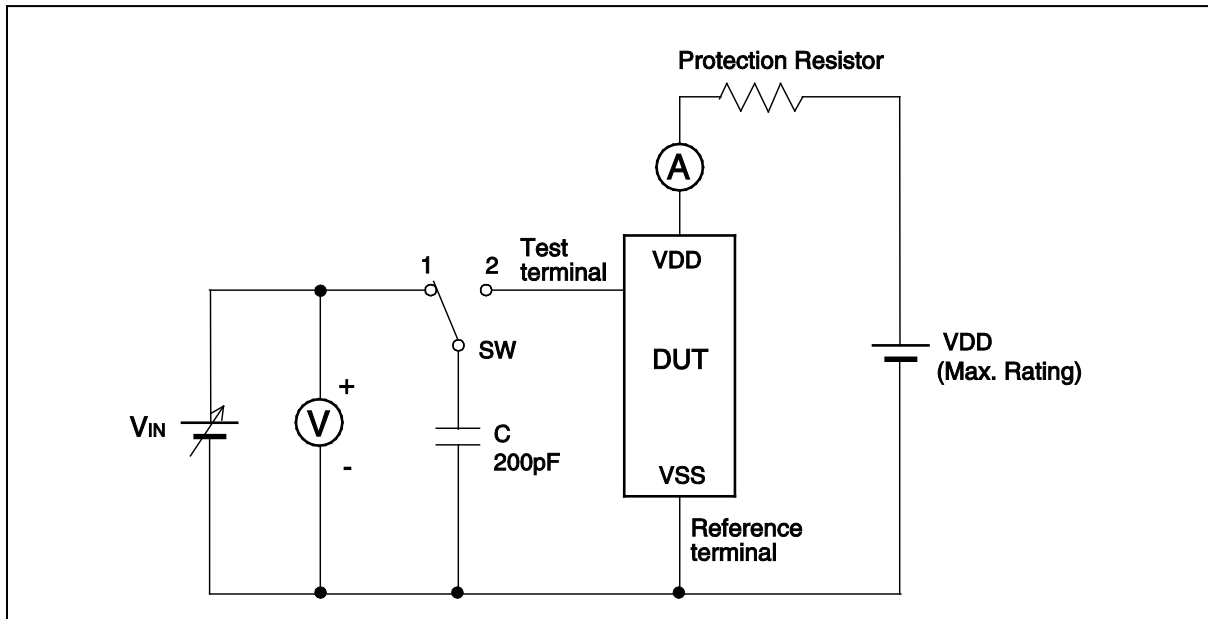
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85R8M2TPBS-M-JAE1	$\geq 2000 \text{ V} $
ESD MM (Machine Model) JESD22-A115 compliant		$\geq 200 \text{ V} $
ESD CDM (Charged Device Model) JESD22-C101 compliant		—
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		—
Latch-Up (C-V Method) Proprietary method		$\geq 200 \text{ V} $

▪ Current method of Latch-Up Resistance Test



Note: The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow.
 Confirm the latch up does not occur under $I_{\text{IN}} = \pm 300 \text{ mA}$.
 In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

▪ C-V method of Latch-Up Resistance Test



Note: Charge voltage alternately switching 1 and 2 approximately 2 sec intervals. This switching process is considered as one cycle.

Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

MB85R8M2T

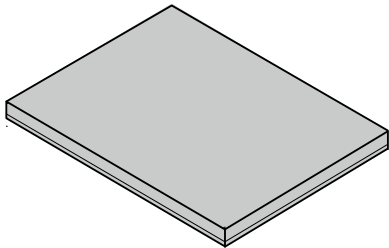
■ ORDERING INFORMATION

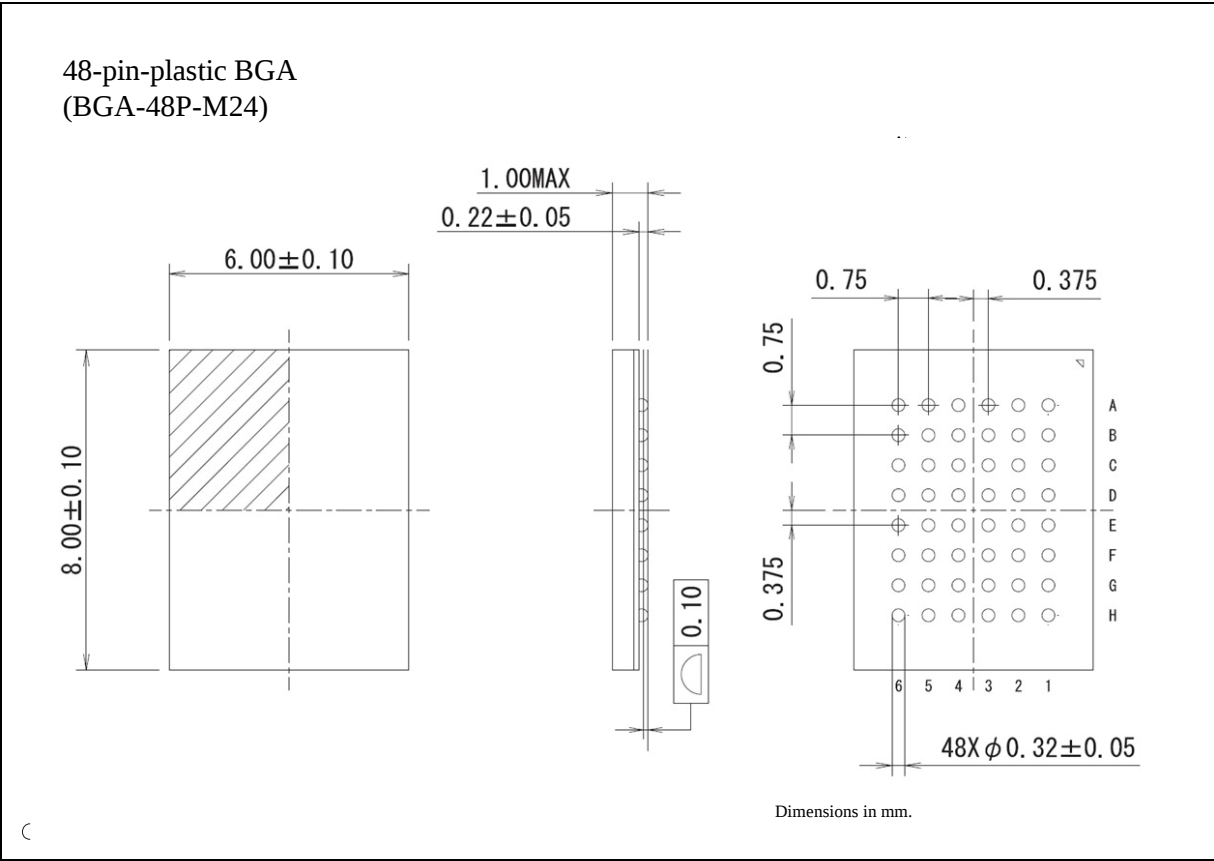
Part Number	Package	Shipping form	Minimum shipping quantity
MB85R8M2TPBS-M-JAE1	48-pin plastic FBGA (BGA-48P-M24)	Tray	—*

*: Please contact our sales office about minimum shipping quantity.

MB85R8M2T

■ PACKAGE DIMENSIONS

48-pin plastic BGA  (BGA- 48P-M24)	Lead pitch	0.75 mm
	Package width × package length	8.00mm × 6.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic Mold
	Mounting height	1.22mm Max.
	Weight	0.08g



■ MARKING

[MB85R8M2TPBS-M-JAE1]



MB85R8M2T
E1 1700 E00



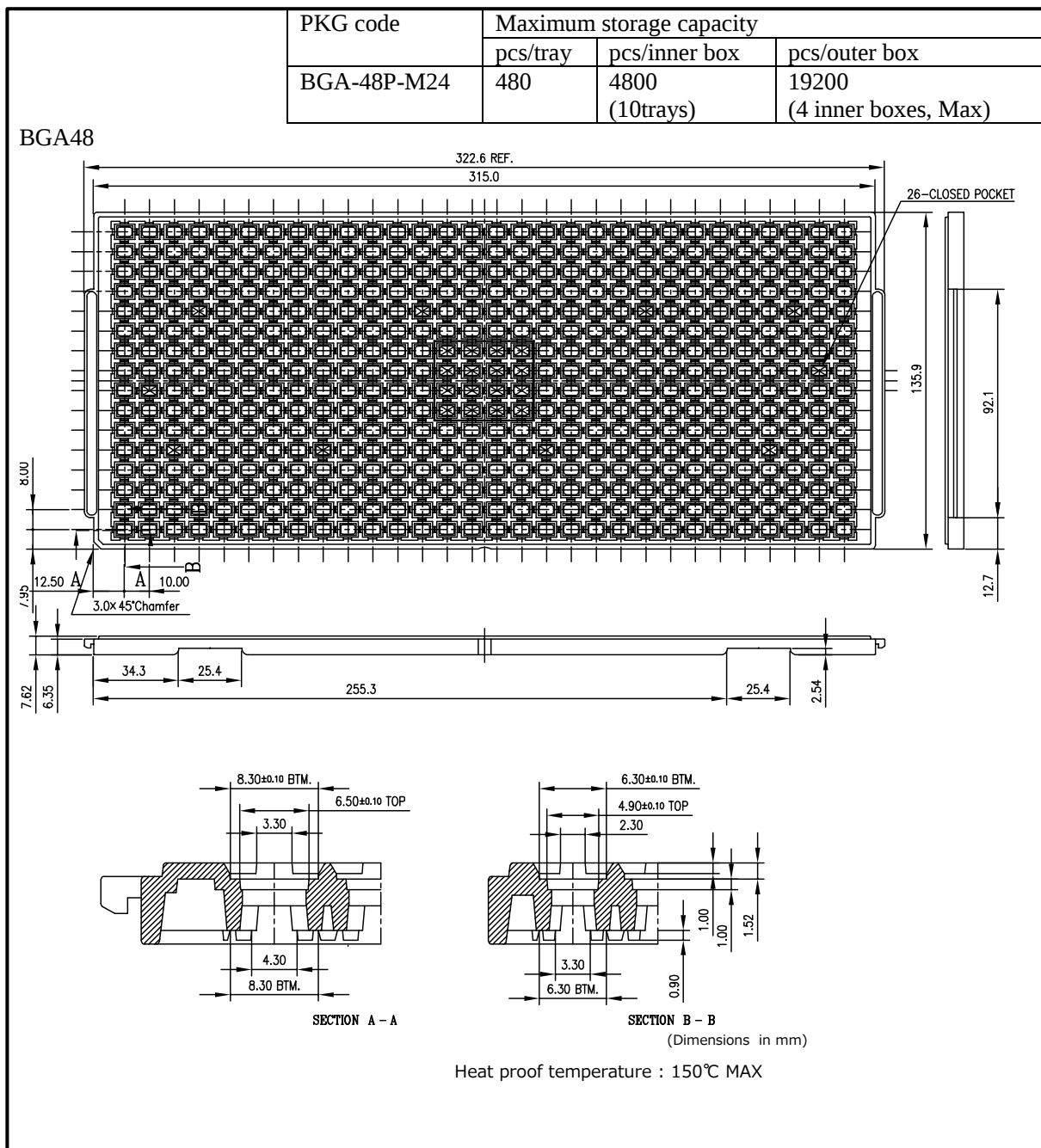
[BGA-48P-M24]

MB85R8M2T

■ PACKING

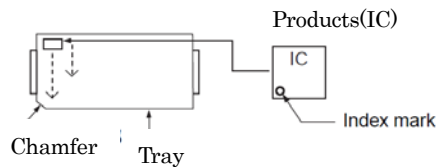
1. Tray

1.1 Tray dimensions



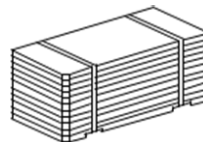
1.2 TRAY Dry Packing Specifications

(1) Pack ICs in the tray

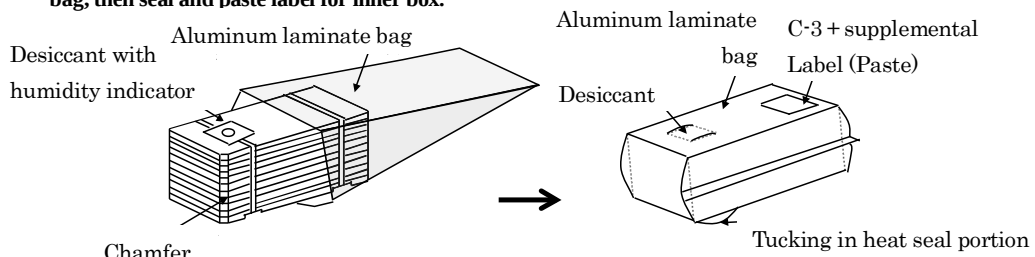


(2) Stack trays in designated number, put the lid(empty tray), bundle with bands.

- * Gaps between trays are uniform.
- * Chamfers direction are the same.
- * Bands are around cut-out portion of trays.

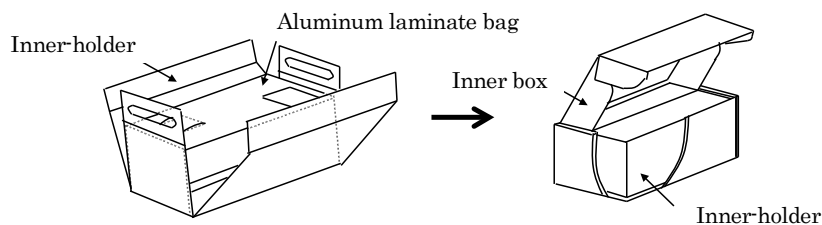


(3) Put desiccant(with humidity indicator:20g) on the bundled trays, vacuum pack in aluminum laminate bag, then seal and paste label for inner box.



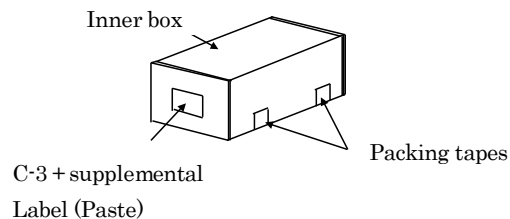
(4) Put the aluminum laminate in inner-holder, store in inner box.

- * It is allowed to put inner-holder in inner box then put aluminum laminate in the inner-holder.



(5) Close the lids of the inner box, paste one label for inner box.

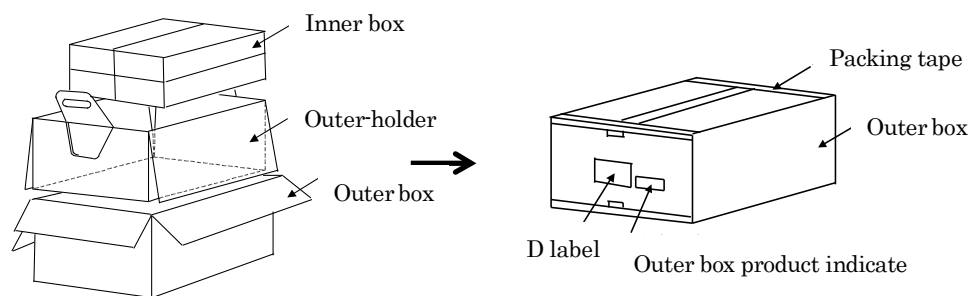
Close the inner box with packing tapes on two portions,



(6) Store in outer box

Put outer-holder in outer box, store inner box(es) maximum four.

Outer box is sealed with packing tape (H-paste), paste outer box product indicate on the designated portion.



MB85R8M2T

1.3 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]

XXXXXXXXXXXXX (Customer part number or FJ part number)		← C3-Label
(3N)1 XXXXXXXXXXXXX	XXX (LEAD FREE mark) (Part number and quantity)	
XXXXXXXXXXXXX (FJ control number)		← Perforated line
(3N)2 XXXXXXXXXXXXX	XXXXX (Quantity)	
XXXXXXXXXXXXX (Customer part number or FJ part number)		← Supplemental Label
(3N)3 XXXXXXXXXXXXX	XXXXX (Customer part number or FJ part number)	
XXXXXXXXXXXXX (Customer part number or FJ part number)		
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx		
XXXXXXXXXXXXX (Customer part number or FJ part number)		
XXXX-XXX XXX (Package count)		
XXXX-XXX XXX (Lot Number and quantity)		
XXXXXXXXXXXXX (FJ control number)		
XXXXXXXXXXXXX (Comment)		

Label II-A: Label on Outer box [D Label] (100mm x 100mm)

発注者 XXXXXXXXXXXX (Customer Name) (CUST.)		受注者 (VENDOR) 富士通		← D Label
受渡場所名 XXXXXXXXXXXX (Delivery Address) (DELIVERY POINT)		セミコンダクター株式会社		
納品キー番号 XXXXXXXXXXXX (TRANS.NO.) (FJ control number)		XXX (FJ control number)		
品名コード XXXXXXXXXXXX (PART NO.) (Customer part number or FJ part number)		XXX (FJ control number)		
品名 (PART NAME) XXXXXXXXXXXX (Part number)		XXXXXXXXXXXXX (Part number)		
入数 / 納入数量 XXX/XXX (Q'TY/TOTAL Q'TY)		単位 XX (UNIT)		
発注者用備考 (CUSTOMER'S REMARKS) XXXXXXXXXXXXXXXXXXXX		梱包個数 (PACKAGE COUNT) XXX/XXX		
(3N)3 XXXXXXXXXXXX XXX (FJ control number + Product quantity)		(FJ control number + Product quantity bar code)		
(3N)4 XXXXXXXXXXXX XXX (Part number + Product quantity)		(Part number + Product quantity bar code)		
(3N)5 XXXXXXXXXXXX (FJ control number)		(FJ control number bar code)		

Label II-B: Outer boxes product indicate

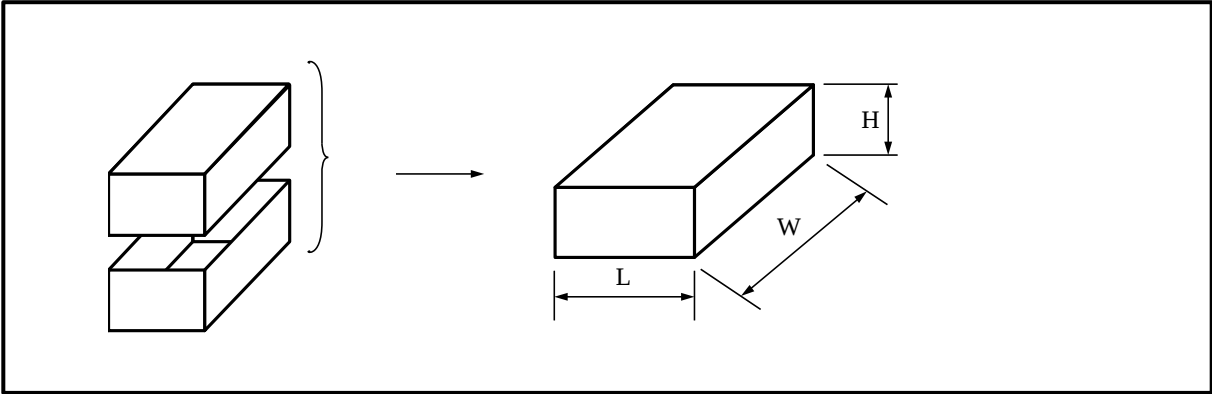
XXXXXXXXXXXXX (Part number)		
(Lot Number)	(Count)	(Quantity)
XXXX-XXX	X 箱	XXX 個
XXXX-XXX	X 箱	XXX 個
	計	XXX 個

Note: Depending on shipment state, "Label II-A" and "Label II-B" on the external boxes might not be printed.

MB85R8M2T

1.4 Dimensions for container

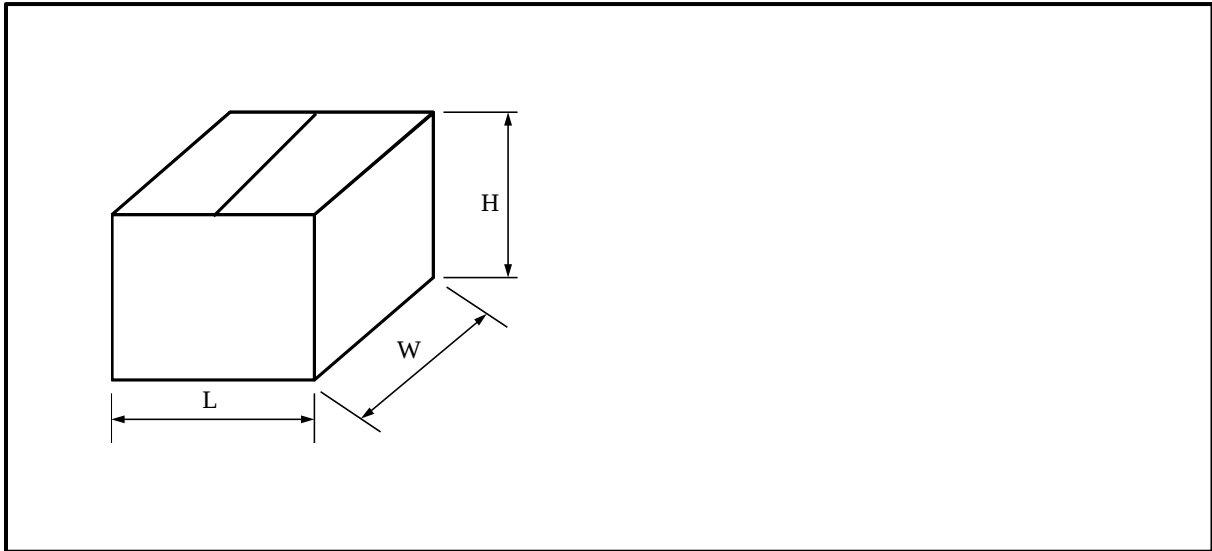
(1) Dimensions for inner box



L	W	H
162	360	90

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
375	410	225

(Dimensions in mm)

FUJITSU SEMICONDUCTOR LIMITED

Shin-Yokohama Chuo Building, 2-100-45 Shin-Yokohama,
Kohoku-ku, Yokohama, Kanagawa 222-0033, Japan
<http://jp.fujitsu.com/fsl/en/>

All Rights Reserved.

FUJITSU SEMICONDUCTOR LIMITED, its subsidiaries and affiliates (collectively, "FUJITSU SEMICONDUCTOR") reserves the right to make changes to the information contained in this document without notice. Please contact your FUJITSU SEMICONDUCTOR sales representatives before order of FUJITSU SEMICONDUCTOR device.

Information contained in this document, such as descriptions of function and application circuit examples is presented solely for reference to examples of operations and uses of FUJITSU SEMICONDUCTOR device. FUJITSU SEMICONDUCTOR disclaims any and all warranties of any kind, whether express or implied, related to such information, including, without limitation, quality, accuracy, performance, proper operation of the device or non-infringement. If you develop equipment or product incorporating the FUJITSU SEMICONDUCTOR device based on such information, you must assume any responsibility or liability arising out of or in connection with such information or any use thereof. FUJITSU SEMICONDUCTOR assumes no responsibility or liability for any damages whatsoever arising out of or in connection with such information or any use thereof.

Nothing contained in this document shall be construed as granting or conferring any right under any patents, copyrights, or any other intellectual property rights of FUJITSU SEMICONDUCTOR or any third party by license or otherwise, express or implied. FUJITSU SEMICONDUCTOR assumes no responsibility or liability for any infringement of any intellectual property rights or other rights of third parties resulting from or in connection with the information contained herein or use thereof.

The products described in this document are designed, developed and manufactured as contemplated for general use including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high levels of safety is secured, could lead directly to death, personal injury, severe physical damage or other loss (including, without limitation, use in nuclear facility, aircraft flight control system, air traffic control system, mass transport control system, medical life support system and military application), or (2) for use requiring extremely high level of reliability (including, without limitation, submersible repeater and artificial satellite). FUJITSU SEMICONDUCTOR shall not be liable for you and/or any third party for any claims or damages arising out of or in connection with above-mentioned uses of the products.

Any semiconductor devices fail or malfunction with some probability. You are responsible for providing adequate designs and safeguards against injury, damage or loss from such failures or malfunctions, by incorporating safety design measures into your facility, equipments and products such as redundancy, fire protection, and prevention of overcurrent levels and other abnormal operating conditions.

The products and technical information described in this document are subject to the Foreign Exchange and Foreign Trade Control Law of Japan, and may be subject to export or import laws or regulations in U.S. or other countries. You are responsible for ensuring compliance with such laws and regulations relating to export or re-export of the products and technical information described herein.

All company names, brand names and trademarks herein are property of their respective owners.