Apollo2 Blue Datasheet

Doc. ID: DS-A2B-0p8

Revision 0.8

November 2017

©2017 Ambiq Micro, Inc.
All rights reserved.

Features

Ultra-low supply current:

- < 10 µA/MHz executing from flash at 3.3 V
- < 10 µA/MHz executing from RAM at 3.3 V
- < 3 µA deep sleep mode with RTC at 3.3 V (Bluetooth in shutdown)

High-performance ARM Cortex-M4 Processor

- Up to 48 MHz clock frequency
- Floating point unit
- Memory protection unit
- Wake-up interrupt controller with 32 interrupts

Integrated Bluetooth®[1] wireless technology V5 low-energy sub-system

- RF sensitivity: -95 dBm
- TX: 5mA @0dBm, RX: 3.5 mA
- Tx output power: -40 dBm to +5 dBm
- AES 128-bit encryption
- Over-The-Air updates (OTA)
- Coexistence with other 2.4 GHz wireless

Ultra-low power memory:

- Up to 1 MB of flash memory for code/data
- Up to 256 KB of low leakage RAM for code/data
- 16kB 2-way Associative Cache

Ultra-low power interface for off-chip sensors:

- 14 bit ADC at up to 1.2 MS/s, 7 simultaneous input channels available
- Voltage Comparator
- Temperature sensor with +/-3ºC accuracy

Flexible serial peripherals:

- 4x I^2C/SPI masters with 128-byte bidirectional FIFO for communication with sensors, radios, and other peripherals
- 1x I^2C/SPI slave for host communications with 256-byte LRAM area for FIFO/host support
- 2x UART modules with 32-location transmit and receive FIFOs
- PDM for mono and stereo audio microphone (256-word FIFO)
- 1x I^2S slave for PDM audio pass-through

Rich set of clock sources:

- 32.768 kHz XTAL oscillator
- Low frequency RC oscillator – 1.024 kHz
- High frequency RC oscillator – 48 MHz
- RTC based on Ambiq's AM08X5/18X5 families

Wide operating range: 1.755-3.60 V, –40 to 85°C

Compact package option:

- 4 x 4 x 0.9 mm 64-pin LGA with up to 31 GPIO

Applications

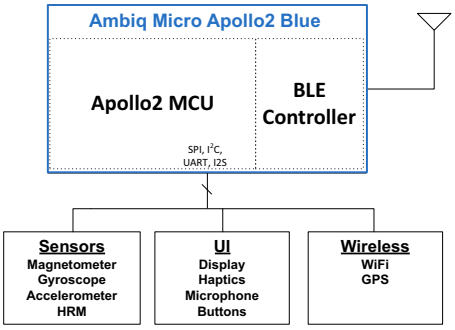
- Wearable electronics including smart watches
- Wireless sensors
- Activity and fitness monitors
- Beacons
- Remote sensing
- Motion and tracking devices
- Home automation
- Light control applications
- Wireless mice and keyboards
- Alarms and security system
- Toys
- Consumer electronics
- Medical devices

Description

The Apollo2 MCU is an ultra-low power, highly integrated microcontroller designed for battery-powered devices including wearable electronics,

1. The *Bluetooth*® word mark and logos are registered trademarks owned by the Bluetooth SIG, Inc. and any use of such marks is under license. Other trademarks and trade names are those of their respective owners.

Typical System Configuration for Apollo2 Blue System-In-Package



©2017 Ambiq Micro, Inc.
All rights reserved.

activity & fitness monitors, and wireless sensors. By combining ultra-low power sensor conversion electronics with the powerful ARM Cortex-M4 processor with Floating Point Unit, the Apollo2 MCU enables complex sensor processing tasks to be completed with unprecedented battery life. Weeks, months, and years of battery life are achievable while doing voice keyword detect, context detection, gesture recognition, and activity monitoring. The second generation Apollo2 MCU takes full advantage of Ambiq Micro's patented Subthreshold Power Optimized Technology (SPOT) Platform, setting a new industry benchmark in low power design.

The Apollo2 Blue builds upon the industry's best power management efficiency of the Apollo2 MCU Family with a System-In-Package comprised of the Apollo2 MCU and a Bluetooth low energy sub-system (BLE) to deliver a totally integrated Bluetooth low energy connectivity solution. The device offers Bluetooth 5 ready radio and integrates 1 MB of flash memory and 256 KB of RAM to accommodate radio and sensor overhead while leaving space for application code. This microcontroller also includes several masters and one slave SPI and I2C ports and two UART ports for communicating with sensors including accelerometers, gyroscopes, and magnetometers. Apollo2 Blue adds top rated Bluetooth low energy radio capability to an already-existing array of relevant functionality built around the Cortex-M4 processor expressly designed for use in IoT and wearables applications.

This datasheet provides details on the Apollo2 Blue. Internal to the Apollo2 Blue, the Apollo2 MCU and BLE are connected via a SPI interface. It is assumed throughout the document that the BLE host stack is run on the Apollo2 MCU, whereas the BLE controller stack is run on the BLE controller. The communication between host and controller is using an HCI interface as described in the Bluetooth low energy standard.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table of Content

1. Apollo2 Blue Package Pins 31
1.1 Pin Configuration 31
1.2 Pin Connections 32
2. System Core 47
2.1 MCU Sub-system 48
2.2 Apollo2 Blue Bluetooth Controller 49
3. MCU Core Details 50
3.1 Interrupts 50
3.2 Memory Map 53
3.3 Memory Protection Unit (MPU) 55
3.4 System Busses 55
3.5 Power Management 55
3.5.1 Cortex-M4 Power Modes 56
3.5.2 System Power Modes 57
3.5.3 Power Control 59
3.6 Debug Interfaces 70
3.6.1 Debugger Attachment 70
3.6.2 Instrumentation Trace Macrocell (ITM) 70
3.6.3 Trace Port Interface Unit (TPIU) 70
3.6.4 Faulting Address Trapping Hardware 70
3.7 ITM Registers 70
3.7.1 Register Memory Map 71
3.7.2 ITM Registers 73
3.8 MCUCTRL Registers 98
3.8.1 Register Memory Map 99
3.8.2 MCUCTRL Registers 100
3.9 Memory Subsystem 118
3.9.1 Features 118
3.9.2 Functional Overview 119
3.9.3 Flash Cache 120
3.9.4 SRAM Interface 134
4. Bluetooth Low Energy Sub-system 135
4.1 Functional Overview 135
4.1.1 Introduction 135
4.1.2 Main Features 136
4.1.3 Typical Applications 136
4.2 Functional Description 136
4.3 BLE Hardware Architecture 137
4.4 BLE Software Architecture 138
4.5 RF Description 138
4.6 Power Management 139
4.6.1 Power Management Configurations 139
4.7 BLE Operating Modes 140
4.7.1 Mode Descriptions 140

©2017 Ambiq Micro, Inc.
All rights reserved.

4.7.2 Mode Transitions 141
4.8 BLE Connections 141
4.8.1 External Pin Connections 141
4.8.2 Internal Die-to-Die Connections 142
5. I2C/SPI Master Module 144
5.1 Functional Overview 144
5.2 Interface Clock Generation 144
5.3 Command Operation 145
5.4 FIFO 147
5.5 I2C Interface 147
5.5.1 Bus Not Busy 148
5.5.2 Start Data Transfer 148
5.5.3 Stop Data Transfer 148
5.5.4 Data Valid 148
5.5.5 Acknowledge 148
5.5.6 I2C Slave Addressing 149
5.5.7 I2C Offset Address Transmission 149
5.5.8 I2C Normal Write Operation 150
5.5.9 I2C Normal Read Operation 150
5.5.10 I2C Raw Write Operation 151
5.5.11 I2C Raw Read Operation 151
5.5.12 Holding the Interface with CONT 151
5.5.13 I2C Multi-master Arbitration 151
5.6 SPI Operations 152
5.6.1 SPI Configuration 152
5.6.2 SPI Slave Addressing 152
5.6.3 SPI Normal Write 152
5.6.4 SPI Normal Read 153
5.6.5 SPI Raw Write 153
5.6.6 SPI Raw Read 154
5.6.7 SPI 3-wire Mode 154
5.6.8 Complex SPI Operations 154
5.6.9 SPI Polarity and Phase 155
5.7 Repeating a Command 155
5.8 Bit Orientation 156
5.9 Full Duplex Operations 156
5.10 SPI Flow Control 156
5.11 Pre-read Control 158
5.12 Minimizing Power 159
5.13 IOMSTR Registers 159
5.13.1 Register Memory Map 160
5.13.2 IOMSTR Registers 162
6. I2C/SPI Slave Module 176
6.1 Functional Overview 176
6.2 Local RAM Allocation 176
6.3 Direct Area Functions 177

©2017 Ambiq Micro, Inc.
All rights reserved.

6.4 FIFO Area Functions 180
6.5 Rearranging the FIFO 181
6.6 Interface Interrupts 181
6.7 Command Completion Interrupts 182
6.8 Host Address Space and Registers 183
6.9 I2C Interface 183
6.9.1 Bus Not Busy 183
6.9.2 Start Data Transfer 184
6.9.3 Stop Data Transfer 184
6.9.4 Data Valid 184
6.9.5 Acknowledge 184
6.9.6 Address Operation 184
6.9.7 Offset Address Transmission 185
6.9.8 Write Operation 185
6.9.9 Read Operation 186
6.9.10 General Address Detection 186
6.10 SPI Interface 186
6.10.1 Write Operation 187
6.10.2 Read Operation 187
6.10.3 Configuring 3-wire vs. 4-wire SPI Mode 187
6.10.4 SPI Polarity and Phase 188
6.11 Bit Orientation 188
6.12 Wakeup Using the I2C/SPI Slave 188
6.13 IOSLAVE Registers 189
6.13.1 Register Memory Map 190
6.13.2 IOSLAVE Registers 191
6.14 Host Side Address Space and Register 203
6.14.1 Host Address Space and Registers 203
7. PDM/I2S Module 208
7.1 Features 208
7.2 Functional Overview 209
7.2.1 PDM-to-PCM Conversion 209
7.2.2 Clock Generation 209
7.2.3 Clock Switching 210
7.2.4 Operating Modes 211
7.2.5 FIFO Control and Interrupts 212
7.2.6 Digital Volume Gain 212
7.2.7 Low Pass Filter (LPF) 213
7.2.8 High Pass Filter 213
7.3 I2S Slave Interface 213
7.4 PDM Registers 214
7.4.1 Register Memory Map 215
7.4.2 PDM Registers 216
8. GPIO and Pad Configuration Module 225
8.1 Functional Overview 225
8.2 Pad Configuration Functions 225

©2017 Ambiq Micro, Inc.
All rights reserved.

8.3 General Purpose I/O (GPIO) Functions 229
8.3.1 Configuring the GPIO Functions 229
8.3.2 Reading from a GPIO Pad 229
8.3.3 Writing to a GPIO Pad 230
8.3.4 GPIO Interrupts 230
8.4 Pad Connection Summary 230
8.4.1 Output Selection 230
8.4.2 Output Control 230
8.4.3 Input Control 232
8.4.4 Pull-up Control 232
8.4.5 Analog Pad Configuration 232
8.5 Module-specific Pad Configuration 232
8.5.1 Implementing IO Master Connections 232
8.5.2 Implementing IO Slave Connections 241
8.5.3 Implementing Counter/Timer Connections 244
8.5.4 Implementing UART Connections 245
8.5.5 Implementing Audio Connections 249
8.5.6 Implementing GPIO Connections 250
8.5.7 Implementing CLKOUT Connections 251
8.5.8 Implementing 32kHz CLKOUT Connections 251
8.5.9 Implementing ADC Connections 251
8.5.10 Implementing Voltage Comparator Connections 253
8.5.11 Implementing the Software Debug Port Connections 253
8.6 GPIO Registers 254
8.6.1 Register Memory Map 255
8.6.2 GPIO Registers 257
9. Clock Generator and Real Time Clock Module 337
9.1 Clock Generator 337
9.1.1 Functional Overview 337
9.1.2 Low Frequency RC Oscillator (LFRC) 338
9.1.3 High Precision XT Oscillator (XT) 338
9.1.4 High Frequency RC Oscillator (HFRC) 340
9.1.5 HFRC Autoadjustment 340
9.1.6 Frequency Measurement 340
9.1.7 Generating 100 Hz 341
9.2 CLKGEN Registers 341
9.2.1 Register Memory Map 342
9.2.2 CLKGEN Registers 343
9.3 Real Time Clock 356
9.3.1 RTC Functional Overview 356
9.3.2 Calendar Counters 356
9.3.3 Calendar Counter Reads 356
9.3.4 Alarms 357
9.3.5 12/24 Hour Mode 357
9.3.6 Century Control and Leap Year Management 357
9.3.7 Weekday Function 358

©2017 Ambiq Micro, Inc.
All rights reserved.

9.4 RTC Registers 358
9.4.1 Register Memory Map 358
9.4.2 RTC Registers 359
10. Counter/Timer Module 366
10.1 Functional Overview 366
10.2 Counter/Timer Functions 366
10.2.1 Single Count (FN = 0) 367
10.2.2 Repeated Count (FN = 1) 367
10.2.3 Single Pulse (FN = 2) 368
10.2.4 Repeated Pulse (FN = 3) 368
10.2.5 Continuous (FN = 4) 369
10.3 Creating 32-bit Counters 370
10.4 Power Optimization by Measuring HCLK 370
10.5 Generating the Sample Rate for the ADC 370
10.6 Measuring Buck Converter Charge Insertion 370
10.7 CTIMER Registers 371
10.7.1 Register Memory Map 371
10.7.2 CTIMER Registers 372
11. System Timer Module 396
11.1 Functional Overview 396
11.2 STIMER Registers 397
11.2.1 Register Memory Map 398
11.2.2 STIMER Registers 399
12. Watchdog Timer Module 417
12.1 Functional Overview 417
12.2 WDT Registers 417
12.2.1 Register Memory Map 418
12.2.2 WDT Registers 419
13. Reset Generator Module 424
13.1 Functional Overview 424
13.2 External Reset Pin 424
13.3 Power-on Event 425
13.4 Brown-out Event 425
13.5 Software Reset 425
13.6 Software Power On Initialization 426
13.7 Watchdog Expiration 426
13.8 RSTGEN Registers 426
13.8.1 Register Memory Map 426
13.8.2 RSTGEN Registers 427
14. UART Module 433
14.1 Features 433
14.2 Functional Overview 433
14.3 Enabling and Selecting the UART Clock 434
14.4 Configuration 434
14.5 Transmit FIFO and Receive FIFO 435
14.6 UART Registers 435

©2017 Ambiq Micro, Inc.
All rights reserved.

14.6.1 Register Memory Map 435
14.6.2 UART Registers 436
15. ADC and Temperature Sensor Module 448
15.1 Features 448
15.2 Functional Overview 449
15.2.1 Clock Source and Dividers 449
15.2.2 15 Channel Analog Mux 449
15.2.3 Triggering and Trigger Sources 450
15.2.4 Voltage Reference Sources 450
15.2.5 Eight Automatically Managed Conversion Slots 450
15.2.6 Automatic Sample Accumulation and Scaling 451
15.2.7 Sixteen Entry Result FIFO 452
15.2.8 Window Comparator 455
15.3 Operating Modes and the Mode Controller 456
15.3.1 Single Mode 457
15.3.2 Repeat Mode 458
15.3.3 Low Power Modes 458
15.4 Interrupts 459
15.5 Voltage Divider and Switchable Battery Load 460
15.6 ADC Registers 461
15.6.1 Register Memory Map 462
15.6.2 ADC Registers 463
16. Voltage Comparator Module 484
16.1 Functional Overview 484
16.2 VCOMP Registers 484
16.2.1 Register Memory Map 485
16.2.2 VCOMP Registers 486
17. Voltage Regulator Module 491
17.1 Functional Overview 491
18. Electrical Characteristics 492
18.1 Absolute Maximum Ratings 492
18.2 Recommended Operating Conditions 494
18.3 Current Consumption 494
18.4 Power Mode Transitions 496
18.5 Clocks/Oscillators 496
18.6 Analog-to-Digital Converter (ADC) 498
18.7 Buck Converter 500
18.8 Power-On RESET (POR) and Brown-Out Detector (BOD) 500
18.9 Resets 501
18.10 Voltage Comparator (VCOMP) 501
18.11 Inter-Integrated Circuit (I2C) Interface 502
18.12 Serial Peripheral Interface (SPI) Master Interface (IOM1, 2) 503
18.13 High Speed Serial Peripheral Interface (SPI) Master Interface (IOM 0, 4) 505
18.14 Serial Peripheral Interface (SPI) Slave Interface 507
18.15 PDM Interface 509
18.16 I2S Interface 509

©2017 Ambiq Micro, Inc.
All rights reserved.

18.17 Universal Asynchronous Receiver/Transmitter (UART) 510
18.18 Counter/Timer (CTIMER) 510
18.19 System Timer (STIMER) 510
18.20 Watchdog Timer (WDT) 510
18.21 Flash Memory 511
18.22 General Purpose Input/Output (GPIO) 511
18.23 Serial Wire Debug (SWD) 514
19. Package Mechanical Information 515
19.1 LGA Package 515
19.2 SMT Assembly Considerations for LGA Package 516
19.2.1 Solder Paste 516
19.2.2 Solder Stencils 516
19.2.3 Package-to-board Assembly 517
20. Ordering Information 531
21. Document Revision History 532

©2017 Ambiq Micro, Inc.
All rights reserved.

List of Figures

Figure 1. Apollo2 Blue LGA Pin Configuration Diagram 31
Figure 2. Block Diagram for the Ultra-Low Power Apollo2 Blue 47
Figure 3. Hardware Architecture 49
Figure 4. ARM Cortex-M4 Vector Table for Apollo2 Blue 51
Figure 5. Block Diagram for Flash and OTP Memory Subsystem 118
Figure 6. Block Diagram for Apollo2 with Flash Cache 120
Figure 7. Block diagram for the Flash Memory Controller 133
Figure 8. Block diagram for the SRAM Interface 134
Figure 9. Block Diagram for the Bluetooth Low Energy Sub-system 135
Figure 10. RF Transceiver Block Diagram 139
Figure 11. Mode Transitions 141
Figure 12. Die-to-Die Interconnection Diagram 142
Figure 13. Block Diagram for the I2C/SPI Master Module 144
Figure 14. I2C/SPI Master Clock Generation 145
Figure 15. Basic I2C Conditions 148
Figure 16. I2C Acknowledge 149
Figure 17. I2C 7-bit Address Operation 149
Figure 18. I2C 10-bit Address Operation 149
Figure 19. I2C Offset Address Transmission 150
Figure 20. I2C Normal Write Operation 150
Figure 21. I2C Normal Read Operation 150
Figure 22. I2C Raw Write Operation 151
Figure 23. I2C Raw Read Operation 151
Figure 24. SPI Normal Write Operation 153
Figure 25. SPI Normal Read Operation 153
Figure 26. SPI Raw Write Operation 154
Figure 27. SPI Raw Read Operation 154
Figure 28. SPI Combined Operation 154
Figure 29. SPI CPOL and CPHA 155
Figure 30. Flow Control at Beginning of a Write Transfer 157
Figure 31. Flow Control at Beginning of a Raw Read Transfer 157
Figure 32. Flow Control in the Middle of a Write Transfer 158
Figure 33. Flow Control in the Middle of a Read Transfer 158
Figure 34. Block diagram for the I2C/SPI Slave Module 176
Figure 35. I2C/SPI Slave Module LRAM Addressing 177
Figure 36. I2C/SPI Slave Module FIFO 181
Figure 37. Basic I2C Conditions 183
Figure 38. I2C Acknowledge 184
Figure 39. I2C 7-bit Address Operation 185
Figure 40. I2C 10-bit Address Operation 185
Figure 41. I2C Offset Address Transmission 185
Figure 42. I2C Write Operation 185
Figure 43. I2C Read Operation 186
Figure 44. SPI Write Operation 187

©2017 Ambiq Micro, Inc.
All rights reserved.

Figure 45. SPI Read Operation 187
Figure 46. SPI CPOL and CPHA 188
Figure 47. Block Diagram for PDM Module 208
Figure 48. Stereo PDM to PCM Conversion Path 209
Figure 49. PDM Clock Timing Diagram 209
Figure 50. PDM Clock Source Switching Flow 211
Figure 51. I2S Interface Data Format Timing 214
Figure 52. I2S Interface Setup and Hold Timing Diagram 214
Figure 53. Block diagram for the General Purpose I/O (GPIO) Module 225
Figure 54. Pad Connection Details 231
Figure 55. Block diagram for the Clock Generator and Real Time Clock Module 337
Figure 56. Block diagram for the Real Time Clock Module 356
Figure 57. Block Diagram for One General Purpose Counter/Timer Pair 366
Figure 58. Counter/Timer Operation, FN = 0 367
Figure 59. Counter/Timer Operation, FN = 1 368
Figure 60. Counter/Timer Operation, FN = 2 368
Figure 61. Counter/Timer Operation, FN = 3 369
Figure 62. Counter/Timer Operation, FN = 4 370
Figure 63. Block Diagram for the System Timer 396
Figure 64. Block diagram for the Watchdog Timer Module 417
Figure 65. Block diagram for the Reset Generator Module 424
Figure 66. Block diagram of circuitry for Reset pin 425
Figure 67. Block Diagram for the UART Module 433
Figure 68. Block Diagram for ADC and Temperature Sensor 448
Figure 69. Scan Flowchart 457
Figure 70. ADC State Diagram 460
Figure 71. Switchable Battery Load 461
Figure 72. Block diagram for the Voltage Comparator Module 484
Figure 73. Block Diagram for the Voltage Regulator Module 491
Figure 74. I2C Timing 502
Figure 75. SPI Master Mode, Phase = 0 503
Figure 76. SPI Master Mode, Phase = 1 504
Figure 77. SPI Master Mode, Phase = 0 505
Figure 78. SPI Master Mode, Phase = 1 506
Figure 79. SPI Slave Mode, Phase = 0 507
Figure 80. SPI Slave Mode, Phase = 1 508
Figure 81. Serial Wire Debug Timing 514
Figure 82. 4 x 4 x 0.9 mm, 0.4 mm Pitch, 64-lead LGA Package 515
Figure 83. Recommended Reflow Profile for 63/37 Solder Paste or Cu lead frame 518
Figure 84. Recommended Reflow Profile for Lead-free Solder Paste or PPF lead frame 519

©2017 Ambiq Micro, Inc.
All rights reserved.

List of Tables

Table 1: Pin List and Function Table 32
Table 2: MCU Interrupt Assignments 52
Table 3: ARM Cortex-M4 Memory Map 53
Table 4: MCU System Memory Map 53
Table 5: MCU Peripheral Device Memory Map 54
Table 6: PWRCTRL Register Map 59
Table 7: SUPPLYSRC Register 60
Table 8: SUPPLYSRC Register Bits 60
Table 9: POWERSTATUS Register 61
Table 10: POWERSTATUS Register Bits 61
Table 11: DEVICEEN Register 61
Table 12: DEVICEEN Register Bits 62
Table 13: SRAMPWDINSLEEP Register 63
Table 14: SRAMPWDINSLEEP Register Bits 63
Table 15: MEMEN Register 64
Table 16: MEMEN Register Bits 65
Table 17: PWRONSTATUS Register 66
Table 18: PWRONSTATUS Register Bits 66
Table 19: SRAMCTRL Register 67
Table 20: SRAMCTRL Register Bits 67
Table 21: ADCSTATUS Register 68
Table 22: ADCSTATUS Register Bits 68
Table 23: MISCOPT Register 69
Table 24: MISCOPT Register Bits 69
Table 25: ITM Register Map 71
Table 26: STIM0 Register 73
Table 27: STIM0 Register Bits 73
Table 28: STIM1 Register 73
Table 29: STIM1 Register Bits 73
Table 30: STIM2 Register 74
Table 31: STIM2 Register Bits 74
Table 32: STIM3 Register 74
Table 33: STIM3 Register Bits 74
Table 34: STIM4 Register 75
Table 35: STIM4 Register Bits 75
Table 36: STIM5 Register 75
Table 37: STIM5 Register Bits 75
Table 38: STIM6 Register 76
Table 39: STIM6 Register Bits 76
Table 40: STIM7 Register 76
Table 41: STIM7 Register Bits 76
Table 42: STIM8 Register 77
Table 43: STIM8 Register Bits 77
Table 44: STIM9 Register 77

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 45: STIM9 Register Bits 77
Table 46: STIM10 Register 78
Table 47: STIM10 Register Bits 78
Table 48: STIM11 Register 78
Table 49: STIM11 Register Bits 78
Table 50: STIM12 Register 79
Table 51: STIM12 Register Bits 79
Table 52: STIM13 Register 79
Table 53: STIM13 Register Bits 79
Table 54: STIM14 Register 80
Table 55: STIM14 Register Bits 80
Table 56: STIM15 Register 80
Table 57: STIM15 Register Bits 80
Table 58: STIM16 Register 81
Table 59: STIM16 Register Bits 81
Table 60: STIM17 Register 81
Table 61: STIM17 Register Bits 81
Table 62: STIM18 Register 82
Table 63: STIM18 Register Bits 82
Table 64: STIM19 Register 82
Table 65: STIM19 Register Bits 82
Table 66: STIM20 Register 83
Table 67: STIM20 Register Bits 83
Table 68: STIM21 Register 83
Table 69: STIM21 Register Bits 83
Table 70: STIM22 Register 84
Table 71: STIM22 Register Bits 84
Table 72: STIM23 Register 84
Table 73: STIM23 Register Bits 84
Table 74: STIM24 Register 85
Table 75: STIM24 Register Bits 85
Table 76: STIM25 Register 85
Table 77: STIM25 Register Bits 85
Table 78: STIM26 Register 86
Table 79: STIM26 Register Bits 86
Table 80: STIM27 Register 86
Table 81: STIM27 Register Bits 86
Table 82: STIM28 Register 87
Table 83: STIM28 Register Bits 87
Table 84: STIM29 Register 87
Table 85: STIM29 Register Bits 87
Table 86: STIM30 Register 88
Table 87: STIM30 Register Bits 88
Table 88: STIM31 Register 88
Table 89: STIM31 Register Bits 88
Table 90: TER Register 89

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 91: TER Register Bits 89
Table 92: TPR Register 89
Table 93: TPR Register Bits 89
Table 94: TCR Register 90
Table 95: TCR Register Bits 90
Table 96: LOCKAREG Register 91
Table 97: LOCKAREG Register Bits 91
Table 98: LOCKSREG Register 91
Table 99: LOCKSREG Register Bits 91
Table 100: PID4 Register 92
Table 101: PID4 Register Bits 92
Table 102: PID5 Register 92
Table 103: PID5 Register Bits 93
Table 104: PID6 Register 93
Table 105: PID6 Register Bits 93
Table 106: PID7 Register 93
Table 107: PID7 Register Bits 94
Table 108: PID0 Register 94
Table 109: PID0 Register Bits 94
Table 110: PID1 Register 94
Table 111: PID1 Register Bits 95
Table 112: PID2 Register 95
Table 113: PID2 Register Bits 95
Table 114: PID3 Register 95
Table 115: PID3 Register Bits 96
Table 116: CID0 Register 96
Table 117: CID0 Register Bits 96
Table 118: CID1 Register 96
Table 119: CID1 Register Bits 97
Table 120: CID2 Register 97
Table 121: CID2 Register Bits 97
Table 122: CID3 Register 97
Table 123: CID3 Register Bits 98
Table 124: MCUCTRL Register Map 99
Table 125: CHIP_INFO Register 100
Table 126: CHIP_INFO Register Bits 100
Table 127: CHIPID0 Register 100
Table 128: CHIPID0 Register Bits 100
Table 129: CHIPID1 Register 101
Table 130: CHIPID1 Register Bits 101
Table 131: CHIPREV Register 101
Table 132: CHIPREV Register Bits 101
Table 133: VENDORID Register 102
Table 134: VENDORID Register Bits 102
Table 135: DEBUGGER Register 102
Table 136: DEBUGGER Register Bits 103

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 137: BUCK Register 103
Table 138: BUCK Register Bits 103
Table 139: BUCK2 Register 104
Table 140: BUCK2 Register Bits 104
Table 141: BUCK3 Register 105
Table 142: BUCK3 Register Bits 105
Table 143: LDOREG2 Register 106
Table 144: LDOREG2 Register Bits 106
Table 145: BODPORCTRL Register 108
Table 146: BODPORCTRL Register Bits 108
Table 147: ADCCAL Register 108
Table 148: ADCCAL Register Bits 109
Table 149: ADCBATTLOAD Register 109
Table 150: ADCBATTLOAD Register Bits 109
Table 151: ADCREFCOMP Register 110
Table 152: ADCREFCOMP Register Bits 110
Table 153: XTALGENCTRL Register 110
Table 154: XTALGENCTRL Register Bits 111
Table 155: BOOTLOADERLOW Register 111
Table 156: BOOTLOADERLOW Register Bits 111
Table 157: SHADOWVALID Register 112
Table 158: SHADOWVALID Register Bits 112
Table 159: ICODEFAULTADDR Register 112
Table 160: ICODEFAULTADDR Register Bits 113
Table 161: DCODEFAULTADDR Register 113
Table 162: DCODEFAULTADDR Register Bits 113
Table 163: SYSFAULTADDR Register 113
Table 164: SYSFAULTADDR Register Bits 114
Table 165: FAULTSTATUS Register 114
Table 166: FAULTSTATUS Register Bits 114
Table 167: FAULTCAPTUREEN Register 115
Table 168: FAULTCAPTUREEN Register Bits 115
Table 169: DBGR1 Register 115
Table 170: DBGR1 Register Bits 116
Table 171: DBGR2 Register 116
Table 172: DBGR2 Register Bits 116
Table 173: PMUENABLE Register 116
Table 174: PMUENABLE Register Bits 117
Table 175: TPIUCTRL Register 117
Table 176: TPIUCTRL Register Bits 117
Table 177: CACHECTRL Register Map 122
Table 178: CACHECFG Register 123
Table 179: CACHECFG Register Bits 123
Table 180: FLASHCFG Register 124
Table 181: FLASHCFG Register Bits 124
Table 182: CACHECTRL Register 125

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 183: CACHECTRL Register Bits 125
Table 184: NCR0START Register 126
Table 185: NCR0START Register Bits 126
Table 186: NCR0END Register 127
Table 187: NCR0END Register Bits 127
Table 188: NCR1START Register 127
Table 189: NCR1START Register Bits 127
Table 190: NCR1END Register 128
Table 191: NCR1END Register Bits 128
Table 192: DMON0 Register 128
Table 193: DMON0 Register Bits 129
Table 194: DMON1 Register 129
Table 195: DMON1 Register Bits 129
Table 196: DMON2 Register 129
Table 197: DMON2 Register Bits 130
Table 198: DMON3 Register 130
Table 199: DMON3 Register Bits 130
Table 200: IMON0 Register 130
Table 201: IMON0 Register Bits 131
Table 202: IMON1 Register 131
Table 203: IMON1 Register Bits 131
Table 204: IMON2 Register 131
Table 205: IMON2 Register Bits 132
Table 206: IMON3 Register 132
Table 207: IMON3 Register Bits 132
Table 208: Operating Modes 140
Table 209: Die-to-Die Interconnection Table 143
Table 210: CMD Register for I2C Operations 145
Table 211: CMD Register for SPI Operations 145
Table 212: CMD Register Field Description 146
Table 213: IOMSTR Register Map 160
Table 214: FIFO Register 162
Table 215: FIFO Register Bits 162
Table 216: FIFOPTR Register 163
Table 217: FIFOPTR Register Bits 163
Table 218: TLNGTH Register 163
Table 219: TLNGTH Register Bits 164
Table 220: FIFOTHR Register 164
Table 221: FIFOTHR Register Bits 164
Table 222: CLKCFG Register 165
Table 223: CLKCFG Register Bits 165
Table 224: CMD Register 166
Table 225: CMD Register Bits 166
Table 226: CMDRPT Register 167
Table 227: CMDRPT Register Bits 167
Table 228: STATUS Register 167

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 229: STATUS Register Bits 167
Table 230: CFG Register 168
Table 231: CFG Register Bits 168
Table 232: INTEN Register 170
Table 233: INTEN Register Bits 170
Table 234: INTSTAT Register 171
Table 235: INTSTAT Register Bits 171
Table 236: INTCLR Register 172
Table 237: INTCLR Register Bits 173
Table 238: INTSET Register 174
Table 239: INTSET Register Bits 174
Table 240: Mapping of Direct Area Access Interrupts and Corresponding REGACCINTSTAT Bits 179
Table 241: I/O Interface Interrupt Control 182
Table 242: IOSLAVE Register Map 190
Table 243: FIFOPTR Register 191
Table 244: FIFOPTR Register Bits 191
Table 245: FIFOCFG Register 191
Table 246: FIFOCFG Register Bits 192
Table 247: FIFOTHR Register 192
Table 248: FIFOTHR Register Bits 192
Table 249: FUPD Register 193
Table 250: FUPD Register Bits 193
Table 251: FIFOCTR Register 193
Table 252: FIFOCTR Register Bits 193
Table 253: FIFOINC Register 194
Table 254: FIFOINC Register Bits 194
Table 255: CFG Register 194
Table 256: CFG Register Bits 195
Table 257: PRENC Register 195
Table 258: PRENC Register Bits 196
Table 259: IOINTCTL Register 196
Table 260: IOINTCTL Register Bits 196
Table 261: GENADD Register 197
Table 262: GENADD Register Bits 197
Table 263: INTEN Register 197
Table 264: INTEN Register Bits 197
Table 265: INTSTAT Register 198
Table 266: INTSTAT Register Bits 198
Table 267: INTCLR Register 199
Table 268: INTCLR Register Bits 199
Table 269: INTSET Register 200
Table 270: INTSET Register Bits 200
Table 271: REGACCINTEN Register 201
Table 272: REGACCINTEN Register Bits 201
Table 273: REGACCINTSTAT Register 201

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 274: REGACCINTSTAT Register Bits 202
Table 275: REGACCINTCLR Register 202
Table 276: REGACCINTCLR Register Bits 202
Table 277: REGACCINTSET Register 202
Table 278: REGACCINTSET Register Bits 203
Table 279: HOST_IER Register 203
Table 280: HOST_IER Register Bits 203
Table 281: HOST_ISR Register 204
Table 282: HOST_ISR Register Bits 204
Table 283: HOST_WCR Register 204
Table 284: HOST_WCR Register Bits 205
Table 285: HOST_WCS Register 205
Table 286: HOST_WCS Register Bits 205
Table 287: FIFOCTRLO Register 206
Table 288: FIFOCTRLO Register Bits 206
Table 289: FIFOCTRUP Register 206
Table 290: FIFOCTRUP Register Bits 206
Table 291: FIFO Register 207
Table 292: FIFO Register Bits 207
Table 293: PDM Clock Output Reference Table 210
Table 294: PDM Operating Modes and Data Formats 211
Table 295: Digital Volume Control 212
Table 296: LPF Digital Filter Parameters 213
Table 297: PDM Register Map 215
Table 298: PCFG Register 216
Table 299: PCFG Register Bits 216
Table 300: VCFG Register 218
Table 301: VCFG Register Bits 218
Table 302: FR Register 219
Table 303: FR Register Bits 219
Table 304: FRD Register 220
Table 305: FRD Register Bits 220
Table 306: FLUSH Register 220
Table 307: FLUSH Register Bits 220
Table 308: FTHR Register 221
Table 309: FTHR Register Bits 221
Table 310: INTEN Register 221
Table 311: INTEN Register Bits 221
Table 312: INTSTAT Register 222
Table 313: INTSTAT Register Bits 222
Table 314: INTCLR Register 223
Table 315: INTCLR Register Bits 223
Table 316: INTSET Register 223
Table 317: INTSET Register Bits 223
Table 318: Drive Strength Control Bits 225
Table 319: Apollo2 Blue Pad Function Mapping 227

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 320: Pad Function Color and Symbol Code 228
Table 321: Special Pad Types 228
Table 322: I2C Pullup Resistor Selection 229
Table 323: IO Master 0 I2C Configuration 232
Table 324: IO Master 1 I2C Configuration 233
Table 325: IO Master 2 I2C Configuration 233
Table 326: IO Master 3 I2C Configuration 234
Table 327: IO Master 4 I2C Configuration 234
Table 328: IO Master 5 I2C Configuration 234
Table 329: IO Master 0 4-wire SPI Configuration 234
Table 331: IO Master 1 4-wire SPI Configuration 236
Table 332: IO Master 1 4-wire SPI nCE Configuration 236
Table 330: IO Master 0 4-wire SPI nCE Configuration 236
Table 333: IO Master 2 4-wire SPI Configuration 237
Table 334: IO Master 2 4-wire SPI nCE Configuration 237
Table 335: IO Master 4 4-wire SPI Configuration 238
Table 336: IO Master 4 4-wire SPI nCE Configuration 238
Table 337: IO Master 5 4-wire SPI Configuration 239
Table 338: IO Master 5 4-wire SPI nCE Configuration 239
Table 339: IO Master 0 3-wire SPI Configuration 239
Table 340: IO Master 1 3-wire SPI Configuration 239
Table 341: IO Master 2 3-wire SPI Configuration 240
Table 342: IO Master 3 3-wire SPI Configuration 240
Table 343: IO Master 4 3-wire SPI Configuration 241
Table 344: IO Master 5 3-wire SPI Configuration 241
Table 345: IO Slave I2C Configuration 241
Table 346: IO Slave 4-wire SPI Configuration 242
Table 347: IO Slave 3-wire SPI Configuration 242
Table 348: I2C Loopback 242
Table 349: 3-wire SPI Loopback 243
Table 350: 4-wire SPI Loopback 243
Table 351: Counter/Timer Pad Configuration 245
Table 353: UART0 RX Configuration 246
Table 354: UART0 RTS Configuration 246
Table 355: UART0 CTS Configuration 246
Table 352: UART0 TX Configuration 246
Table 358: UART1 RTS Configuration 248
Table 359: UART1 CTS Configuration 248
Table 356: UART1 TX Configuration 248
Table 357: UART1 RX Configuration 248
Table 361: PDM DATA Configuration 250
Table 362: I2S BCLK Configuration 250
Table 363: I2S WCLK Configuration 250
Table 364: I2S DAT Configuration 250
Table 360: PDM CLK Configuration 250
Table 365: CLKOUT Configuration 251

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 366: 32kHz CLKOUT Configuration 251
Table 367: ADC Analog Input Configuration 251
Table 369: Voltage Comparator Reference Configuration 253
Table 370: Voltage Comparator Input Configuration 253
Table 368: ADC Trigger Input Configuration 253
Table 371: SWO Configuration 254
Table 372: GPIO Register Map 255
Table 373: PADREGA Register 257
Table 374: PADREGA Register Bits 257
Table 375: PADREGB Register 259
Table 376: PADREGB Register Bits 260
Table 377: PADREGC Register 262
Table 378: PADREGC Register Bits 262
Table 379: PADREGD Register 265
Table 380: PADREGD Register Bits 265
Table 381: PADREGE Register 267
Table 382: PADREGE Register Bits 267
Table 383: PADREGF Register 270
Table 384: PADREGF Register Bits 270
Table 385: PADREGG Register 272
Table 386: PADREGG Register Bits 272
Table 387: PADREGH Register 273
Table 388: PADREGH Register Bits 273
Table 389: PADREGJ Register 275
Table 390: PADREGJ Register Bits 275
Table 391: PADREGK Register 277
Table 392: PADREGK Register Bits 277
Table 393: PADREGL Register 279
Table 394: PADREGL Register Bits 279
Table 395: PADREGM Register 281
Table 396: PADREGM Register Bits 281
Table 397: CFGA Register 282
Table 398: CFGA Register Bits 283
Table 399: CFGB Register 285
Table 400: CFGB Register Bits 285
Table 401: CFGC Register 288
Table 402: CFGC Register Bits 288
Table 403: CFGD Register 290
Table 404: CFGD Register Bits 290
Table 405: CFGE Register 292
Table 406: CFGE Register Bits 292
Table 407: CFGF Register 294
Table 408: CFGF Register Bits 294
Table 409: PADKEY Register 296
Table 410: PADKEY Register Bits 296
Table 411: RDA Register 296

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 412: RDA Register Bits 296
Table 413: RDB Register 297
Table 414: RDB Register Bits 297
Table 415: WTA Register 297
Table 416: WTA Register Bits 297
Table 417: WTB Register 298
Table 418: WTB Register Bits 298
Table 419: WTSA Register 298
Table 420: WTSA Register Bits 298
Table 421: WTSB Register 299
Table 422: WTSB Register Bits 299
Table 423: WTCA Register 299
Table 424: WTCA Register Bits 299
Table 425: WTCB Register 300
Table 426: WTCB Register Bits 300
Table 427: ENA Register 300
Table 428: ENA Register Bits 300
Table 429: ENB Register 301
Table 430: ENB Register Bits 301
Table 431: ENSA Register 301
Table 432: ENSA Register Bits 301
Table 433: ENSB Register 302
Table 434: ENSB Register Bits 302
Table 435: ENCA Register 302
Table 436: ENCA Register Bits 302
Table 437: ENCB Register 303
Table 438: ENCB Register Bits 303
Table 439: STMRCAP Register 303
Table 440: STMRCAP Register Bits 303
Table 441: IOM0IRQ Register 304
Table 442: IOM0IRQ Register Bits 304
Table 443: IOM1IRQ Register 305
Table 444: IOM1IRQ Register Bits 305
Table 445: IOM2IRQ Register 305
Table 446: IOM2IRQ Register Bits 305
Table 447: IOM3IRQ Register 306
Table 448: IOM3IRQ Register Bits 306
Table 449: IOM4IRQ Register 306
Table 450: IOM4IRQ Register Bits 306
Table 451: IOM5IRQ Register 307
Table 452: IOM5IRQ Register Bits 307
Table 453: LOOPBACK Register 307
Table 454: LOOPBACK Register Bits 307
Table 455: GPIOOBS Register 308
Table 456: GPIOOBS Register Bits 308
Table 457: ALTPADCFGA Register 309

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 458: ALTPADCFGA Register Bits 309
Table 459: ALTPADCFGB Register 310
Table 460: ALTPADCFGB Register Bits 310
Table 461: ALTPADCFGC Register 311
Table 462: ALTPADCFGC Register Bits 311
Table 463: ALTPADCFGD Register 313
Table 464: ALTPADCFGD Register Bits 313
Table 465: ALTPADCFGE Register 314
Table 466: ALTPADCFGE Register Bits 314
Table 467: ALTPADCFGF Register 315
Table 468: ALTPADCFGF Register Bits 315
Table 469: ALTPADCFGG Register 317
Table 470: ALTPADCFGG Register Bits 317
Table 471: ALTPADCFGH Register 318
Table 472: ALTPADCFGH Register Bits 318
Table 473: ALTPADCFGI Register 319
Table 474: ALTPADCFGI Register Bits 319
Table 475: ALTPADCFGJ Register 320
Table 476: ALTPADCFGJ Register Bits 320
Table 477: ALTPADCFGK Register 321
Table 478: ALTPADCFGK Register Bits 321
Table 479: ALTPADCFGL Register 322
Table 480: ALTPADCFGL Register Bits 322
Table 481: ALTPADCFGM Register 324
Table 482: ALTPADCFGM Register Bits 324
Table 483: INT0EN Register 325
Table 484: INT0EN Register Bits 325
Table 485: INT0STAT Register 326
Table 486: INT0STAT Register Bits 326
Table 487: INT0CLR Register 328
Table 488: INT0CLR Register Bits 328
Table 489: INT0SET Register 330
Table 490: INT0SET Register Bits 330
Table 491: INT1EN Register 332
Table 492: INT1EN Register Bits 332
Table 493: INT1STAT Register 333
Table 494: INT1STAT Register Bits 333
Table 495: INT1CLR Register 334
Table 496: INT1CLR Register Bits 334
Table 497: INT1SET Register 335
Table 498: INT1SET Register Bits 335
Table 499: CLKGEN Register Map 342
Table 500: CALXT Register 343
Table 501: CALXT Register Bits 343
Table 502: CALRC Register 343
Table 503: CALRC Register Bits 343

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 504: ACALCTR Register 344
Table 505: ACALCTR Register Bits 344
Table 506: OCTRL Register 344
Table 507: OCTRL Register Bits 344
Table 508: CLKOUT Register 345
Table 509: CLKOUT Register Bits 345
Table 510: CCTRL Register 347
Table 511: CCTRL Register Bits 347
Table 512: STATUS Register 347
Table 513: STATUS Register Bits 347
Table 514: HFADJ Register 348
Table 515: HFADJ Register Bits 348
Table 516: HFVAL Register 349
Table 517: HFVAL Register Bits 349
Table 518: CLOCKEN Register 350
Table 519: CLOCKEN Register Bits 350
Table 520: CLOCKEN2 Register 351
Table 521: CLOCKEN2 Register Bits 351
Table 522: CLOCKEN3 Register 351
Table 523: CLOCKEN3 Register Bits 351
Table 524: UARTEN Register 352
Table 525: UARTEN Register Bits 352
Table 526: INTEN Register 353
Table 527: INTEN Register Bits 353
Table 528: INTSTAT Register 353
Table 529: INTSTAT Register Bits 353
Table 530: INTCLR Register 354
Table 531: INTCLR Register Bits 354
Table 532: INTSET Register 355
Table 533: INTSET Register Bits 355
Table 534: Alarm RPT Function 357
Table 535: INTSET Register Bits 358
Table 536: RTC Register Map 358
Table 537: CTRLOW Register 359
Table 538: CTRLOW Register Bits 359
Table 539: CTRUP Register 360
Table 540: CTRUP Register Bits 360
Table 541: ALMLOW Register 361
Table 542: ALMLOW Register Bits 361
Table 543: ALMUP Register 361
Table 544: ALMUP Register Bits 362
Table 545: RTCCTL Register 362
Table 546: RTCCTL Register Bits 362
Table 547: INTEN Register 363
Table 548: INTEN Register Bits 363
Table 549: INTSTAT Register 364

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 550: INTSTAT Register Bits 364
Table 551: INTCLR Register 364
Table 552: INTCLR Register Bits 365
Table 553: INTSET Register 365
Table 554: INTSET Register Bits 365
Table 555: CTIMER Register Map 371
Table 556: TMR0 Register 372
Table 557: TMR0 Register Bits 372
Table 558: CMPRA0 Register 372
Table 559: CMPRA0 Register Bits 372
Table 560: CMPRB0 Register 373
Table 561: CMPRB0 Register Bits 373
Table 562: CTRL0 Register 373
Table 563: CTRL0 Register Bits 374
Table 564: TMR1 Register 376
Table 565: TMR1 Register Bits 377
Table 566: CMPRA1 Register 377
Table 567: CMPRA1 Register Bits 377
Table 568: CMPRB1 Register 377
Table 569: CMPRB1 Register Bits 378
Table 570: CTRL1 Register 378
Table 571: CTRL1 Register Bits 378
Table 572: TMR2 Register 381
Table 573: TMR2 Register Bits 381
Table 574: CMPRA2 Register 381
Table 575: CMPRA2 Register Bits 382
Table 576: CMPRB2 Register 382
Table 577: CMPRB2 Register Bits 382
Table 578: CTRL2 Register 383
Table 579: CTRL2 Register Bits 383
Table 580: TMR3 Register 386
Table 581: TMR3 Register Bits 386
Table 582: CMPRA3 Register 386
Table 583: CMPRA3 Register Bits 386
Table 584: CMPRB3 Register 387
Table 585: CMPRB3 Register Bits 387
Table 586: CTRL3 Register 387
Table 587: CTRL3 Register Bits 387
Table 588: INTEN Register 390
Table 589: INTEN Register Bits 390
Table 590: INTSTAT Register 392
Table 591: INTSTAT Register Bits 392
Table 592: INTCLR Register 393
Table 593: INTCLR Register Bits 393
Table 594: INTSET Register 394
Table 595: INTSET Register Bits 394

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 596: STIMER Register Map 398
Table 597: STCFG Register 399
Table 598: STCFG Register Bits 399
Table 599: STTMR Register 401
Table 600: STTMR Register Bits 401
Table 601: CAPTURE_CONTROL Register 401
Table 602: CAPTURE_CONTROL Register Bits 401
Table 603: SCMPR0 Register 402
Table 604: SCMPR0 Register Bits 402
Table 605: SCMPR1 Register 403
Table 606: SCMPR1 Register Bits 403
Table 607: SCMPR2 Register 403
Table 608: SCMPR2 Register Bits 404
Table 609: SCMPR3 Register 404
Table 610: SCMPR3 Register Bits 404
Table 611: SCMPR4 Register 405
Table 612: SCMPR4 Register Bits 405
Table 613: SCMPR5 Register 405
Table 614: SCMPR5 Register Bits 405
Table 615: SCMPR6 Register 406
Table 616: SCMPR6 Register Bits 406
Table 617: SCMPR7 Register 406
Table 618: SCMPR7 Register Bits 407
Table 619: SCAPT0 Register 407
Table 620: SCAPT0 Register Bits 407
Table 621: SCAPT1 Register 407
Table 622: SCAPT1 Register Bits 408
Table 623: SCAPT2 Register 408
Table 624: SCAPT2 Register Bits 408
Table 625: SCAPT3 Register 408
Table 626: SCAPT3 Register Bits 409
Table 627: SNVR0 Register 409
Table 628: SNVR0 Register Bits 409
Table 629: SNVR1 Register 409
Table 630: SNVR1 Register Bits 410
Table 631: SNVR2 Register 410
Table 632: SNVR2 Register Bits 410
Table 633: STMINTEN Register 410
Table 634: STMINTEN Register Bits 411
Table 635: STMINTSTAT Register 412
Table 636: STMINTSTAT Register Bits 412
Table 637: STMINTCLR Register 413
Table 638: STMINTCLR Register Bits 413
Table 639: STMINTSET Register 415
Table 640: STMINTSET Register Bits 415
Table 641: WDT Register Map 418

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 642: CFG Register 419
Table 643: CFG Register Bits 419
Table 644: RSTRT Register 420
Table 645: RSTRT Register Bits 420
Table 646: LOCK Register 420
Table 647: LOCK Register Bits 420
Table 648: COUNT Register 421
Table 649: COUNT Register Bits 421
Table 650: INTEN Register 421
Table 651: INTEN Register Bits 422
Table 652: INTSTAT Register 422
Table 653: INTSTAT Register Bits 422
Table 654: INTCLR Register 422
Table 655: INTCLR Register Bits 423
Table 656: INTSET Register 423
Table 657: INTSET Register Bits 423
Table 658: RSTGEN Register Map 426
Table 659: CFG Register 427
Table 660: CFG Register Bits 427
Table 661: SWPOI Register 427
Table 662: SWPOI Register Bits 428
Table 663: SWPOR Register 428
Table 664: SWPOR Register Bits 428
Table 665: STAT Register 429
Table 666: STAT Register Bits 429
Table 667: CLRSTAT Register 429
Table 668: CLRSTAT Register Bits 430
Table 669: TPIU_RST Register 430
Table 670: TPIU_RST Register Bits 430
Table 671: INTEN Register 431
Table 672: INTEN Register Bits 431
Table 673: INTSTAT Register 431
Table 674: INTSTAT Register Bits 431
Table 675: INTCLR Register 432
Table 676: INTCLR Register Bits 432
Table 677: INTSET Register 432
Table 678: INTSET Register Bits 432
Table 679: UART Register Map 435
Table 680: DR Register 436
Table 681: DR Register Bits 436
Table 682: RSR Register 437
Table 683: RSR Register Bits 437
Table 684: FR Register 438
Table 685: FR Register Bits 438
Table 686: ILPR Register 439
Table 687: ILPR Register Bits 439

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 688: IBRD Register 439
Table 689: IBRD Register Bits 439
Table 690: FBRD Register 440
Table 691: FBRD Register Bits 440
Table 692: LCRH Register 440
Table 693: LCRH Register Bits 440
Table 694: CR Register 441
Table 695: CR Register Bits 441
Table 696: IFLS Register 442
Table 697: IFLS Register Bits 443
Table 698: IER Register 443
Table 699: IER Register Bits 443
Table 700: IES Register 444
Table 701: IES Register Bits 444
Table 702: MIS Register 445
Table 703: MIS Register Bits 445
Table 704: IEC Register 446
Table 705: IEC Register Bits 446
Table 706: One SLOT Configuration Register 451
Table 707: 10.6 ADC Sample Format 451
Table 708: Per Slot Sample Accumulator 452
Table 709: Accumulator Scaling 452
Table 710: FIFO Register 453
Table 711: 14-bit FIFO Data Format 453
Table 712: 12-bit FIFO Data Format 453
Table 713: 10-bit FIFO Data Format 453
Table 714: 8-bit FIFO Data Format 454
Table 715: Window Comparator Lower Limit Register 455
Table 716: Window Comparator Upper Limit Register 455
Table 717: ADC Power Modes 458
Table 718: ADC Register Map 462
Table 719: CFG Register 463
Table 720: CFG Register Bits 463
Table 721: STAT Register 465
Table 722: STAT Register Bits 465
Table 723: SWT Register 465
Table 724: SWT Register Bits 465
Table 725: SL0CFG Register 466
Table 726: SL0CFG Register Bits 466
Table 727: SL1CFG Register 467
Table 728: SL1CFG Register Bits 467
Table 729: SL2CFG Register 469
Table 730: SL2CFG Register Bits 469
Table 731: SL3CFG Register 470
Table 732: SL3CFG Register Bits 470
Table 733: SL4CFG Register 472

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 734: SL4CFG Register Bits 472
Table 735: SL5CFG Register 473
Table 736: SL5CFG Register Bits 473
Table 737: SL6CFG Register 475
Table 738: SL6CFG Register Bits 475
Table 739: SL7CFG Register 476
Table 740: SL7CFG Register Bits 476
Table 741: WULIM Register 478
Table 742: WULIM Register Bits 478
Table 743: WLLIM Register 478
Table 744: WLLIM Register Bits 478
Table 745: FIFO Register 479
Table 746: FIFO Register Bits 479
Table 747: INTEN Register 479
Table 748: INTEN Register Bits 480
Table 749: INTSTAT Register 480
Table 750: INTSTAT Register Bits 480
Table 751: INTCLR Register 481
Table 752: INTCLR Register Bits 481
Table 753: INTSET Register 482
Table 754: INTSET Register Bits 482
Table 755: VCOMP Register Map 485
Table 756: CFG Register 486
Table 757: CFG Register Bits 486
Table 758: STAT Register 487
Table 759: STAT Register Bits 487
Table 760: PWDKEY Register 488
Table 761: PWDKEY Register Bits 488
Table 762: INTEN Register 488
Table 763: INTEN Register Bits 488
Table 764: INTSTAT Register 489
Table 765: INTSTAT Register Bits 489
Table 766: INTCLR Register 489
Table 767: INTCLR Register Bits 489
Table 768: INTSET Register 490
Table 769: INTSET Register Bits 490
Table 770: VREG Status 491
Table 771: Absolute Maximum Ratings 492
Table 772: Recommended Operating Conditions 494
Table 773: Current Consumption 494
Table 774: Power Mode Transitions 496
Table 775: Clocks/Oscillators 496
Table 776: Analog to Digital Converter (ADC) 498
Table 777: Buck Converter 500
Table 778: Power-On Reset (POR) and Brown-Out Detector (BOD) 500
Table 779: Resets 501

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 780: Voltage Comparator (VCOMP) 501
Table 781: Inter-Integrated Circuit (I2C) Interface 502
Table 782: Serial Peripheral Interface (SPI) Master Interface 503
Table 783: High Speed Serial Peripheral Interface (SPI) Master Interface 505
Table 784: Serial Peripheral Interface (SPI) Slave Interface 507
Table 785: Pulse Density Modulation (PDM) Interface 509
Table 786: Inter-Integrated Serial (I2S) Interface 509
Table 787: Universal Asynchronous Receiver/Transmitter (UART) 510
Table 788: Counter/Timer (CTIMER) 510
Table 789: System Timer (WDT) 510
Table 790: Watchdog Timer (WDT) 510
Table 791: Flash Memory 511
Table 792: General Purpose Input/Output (GPIO) 511
Table 793: Serial Wire Debug (SWD) 514
Table 794: Reflow Soldering Requirements (Pb-free assembly) 515
Table 795: 531
Table 796: Ordering Information 531
Table 797: Document Revision List 532

©2017 Ambiq Micro, Inc.
All rights reserved.

1. Apollo2 Blue Package Pins

1.1 Pin Configuration

Notes:

- Pads outlined in red are internally connected and should be NO CONNECTS on the PCB.
- Pads outlined in orange are connected internally to the BLE module for testing and status information. These connections are brought out to the pins when the pad is configured as GPIO. The pads can be configured as other functions as specified in the Pin List and Function Table. These pins should be connected and configured carefully.

Figure 1. Apollo2 Blue LGA Pin Configuration Diagram

©2017 Ambiq Micro, Inc.
All rights reserved.

1.2 Pin Connections

The following table lists the external pins of the Apollo2 Blue and their available functions.

Note that several internal connections to the BLE sub-system are brought out to external pins for debugging purposes. These are the pins outlined in red in Figure 1 above. They are not listed in the below table, but are described in “Internal Die-to-Die Connections” on page 142 in the BLE chapter.

GPIO pad numbers listed in orange in Table 1 are connected internally to the BLE module for testing and status information. These connections are brought out to the pins when the pad is configured as GPIO or another listed function.

NOTE: The VIO supply for the BLE subsystem and the Apollo2 VDDH supply must be at the same voltage, ideally tied to the same supply, for operational internal communication.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
POWER					
C2	-	-	VDDP	VDD Supply for Buck converters	Power
B2	-	-	GNDP	Ground Connection for I/O Pads	Ground
B4	-	-	VDDA	Analog Voltage Supply	Power
B3	-	-	GNDA	Ground for Analog Supply	Ground
H4	-	-	GNDD	Ground for Digital Supply	Ground
H3	-	-	VDDH	VDD Supply for I/O pads	Power
C6			ADC_VREF	Dedicated ADC voltage reference	Power
BUCK					
C1	-	-	VDDF	Memory Buck Converter Voltage Output Supply	Power
A1	-	-	COREBUCK_SW	Core Buck Converter Inductor Switch	Power
B1	-	-	MEM_BUCK_SW	Memory Buck Converter Inductor Switch	Power
A2	-	-	VDDC	Core Buck Converter Voltage Output Supply	Power

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
OSCILLATOR					
A4	-	-	XO	32.768 kHz Crystal Output	XT
A3	-	-	XI	32.768 kHz Crystal Input	XT
RESET					
G6	-	-	nRST	External Reset Input	Input/ Output
BLE SUB-SYSTEM					
H6			XIN	48MHz XTAL input	XT
H5			XOUT	48MHz XTAL output	XT
C8			VCC	Analog Supply Voltage	Power
A8			VBAT1	DCDC Supply input	Power
D8			VBAT2	Supply for Power management	Power
B8			VIO	Supply for GPIOs / ESD rails	Power
H8			ANT	Antenna Port	Input/Output
A7			SW_DCDC	DCDC Switch output	Output
G8			AVSS_PA	AVSS_PA (GND for PA)	Ground
H7			AVSS	AVSS_RF, AVSS_PR, AVSS_PLL connected together on substrate	Ground
A5			VSS	Logic and System Ground	Ground
A6			VSS_DCDC	DCDC Ground	Ground
GPIO					

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
H1	0	0	SLSCL	I^2C Slave Clock	Input
		1	SLSCK	SPI Slave Clock	Input
		2	CLKOUT	Oscillator output clock	Output
		3	GPIO0	General Purpose I/O	Input/ Output
		4	MxSCKLB	SPI MX CLKI-OUT->CLKIN Loopback	Output
		5	M2SCK	SPI Master 2 Clock	Output
		6	MxSCLLB	I^2C MX CLKIOUT->CLKIN Loopback	Input
		7	M2SCL	I^2C Master 2 Clock	Open Drain Output
G1	1	0	SLSDA	I^2C Slave I/O Data	Bidirectional Open Drain
		1	SLMISO	SPI Slave Output Data	Output
		2	UART0TX	UART0 Transmit	Output
		3	GPIO1	General Purpose I/O	Input/ Output
		4	MxMISOLB	SPI M0 Data Loopback (int to IOM)	Input
		5	M2MIS0	SPI Master 2 Input Data	Input
		6	MxSDALB	Loopback I^2C Master 0 I/O Data	Bidirectional Open Drain
		7	M2SDA	I^2C Master 2 I/O Data	Bidirectional Open Drain

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
E1	2	0	SLWIR3	SPI Slave I/O Pin for 3-Wire Mode	Bidirectional 3-state
		1	SLMOSI	SPI Slave Input Data	Input
		2	UART0RX	UART0 Receive	Input
		3	GPIO2	General Purpose I/O	Input/ Output
		4	MxMOSILB	SPI Master 0 Output Data (loopback)	Input
		5	M2MOSI	SPI Master 2 Output Data	Output
		6	MxWIR3LB	SPI Master 0 I/O Pin for 3-Wire Mode (loopback)	Bidirectional 3-state
		7	M2WIR3	SPI Master 1 I/O Pin for 3-Wire Mode (loopback)	Bidirectional 3-state
F2	3	0	UA0RTS	UART0 Request to Send (RTS)	Output
		1	SLnCE	SPI Slave Chip Enable	Input
		2	M1nCE4	SPI Master 1 Chip Enable 4	Output
		3	GPIO3	General Purpose I/O	Input/ Output
		4	MxnCELB	SPI Master 0 Chip Enable (loopback)	Input
		5	M2nCE0	SPI Master 2 Chip Enable 0	Output
		6	TRIG1	ADC Trigger input	Input
		7	I2S_WCLK	I2S L/R Clock	Input

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
F8	4	0	UA0CTS	UART0 Clear to Send (CTS)	Input
		1	SLINT	Configurable Slave Interrupt	Output
		2	M0nCE5	SPI Master 0 Chip Enable 5	Output
		3	GPIO4	General Purpose I/O	Input/ Output
		4	SLINTGP	Loopback Slave Interrupt	Input
		5	M2nCE5	SPI Master 2 Chip Enable 5	Output
		6	CLKOUT	Oscillator Output Clock	Output
		7	32KHz_XT	32 kHz Clock	Output
F1	5	0	M0SCL	I^2C Master 0 Clock	Open Drain Output
		1	M0SCK	SPI Master 0 Clock	Output
		2	UA0RTS	UART0 Request To Send (RTS)	Output
		3	GPIO5	General Purpose I/O	Input/ Output
		4	M0SCKLB	SPI Master 0 Clock (loopback)	Output
		5	RSVD	Reserved for future use	
		6	M0SCLLB	I^2C Master 0 Clock (loopback)	Open Drain Output
		7	M1nCE2	SPI Master 1 Chip Enable 2	Output

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
E2	6	0	M0SDA	I^2C Master 0 Data	Bidirectional Open Drain
		1	M0MISO	SPI Master 0 Input Data	Input
		2	UA0CTS	UART0 Clear To Send (CTS)	Input
		3	GPIO6	General Purpose I/O	Input/ Output
		4	SLMISOLB	Loopback SPI Slave Output Data (loopback)	Output
		5	M1nCE0	SPI Master 1 Chip Enable 0	Output
		6	SLSDALB	Loopback I^2C Slave I/O Data (loopback)	Bidirectional Open Drain
		7	I2S_DAT	I2S Data output	Output
D1	7	0	M0WIR3	SPI Master 0 I/O Pin for 3-Wire Mode	Bidirectional 3-state
		1	M0MOSI	SPI Master 0 Out-put Data	Output
		2	CLKOUT	Oscillator Output Clock	Output
		3	GPIO7	General Purpose I/O	Input/ Output
		4	TRIG0	ADC Trigger Input	Input
		5	UART0TX	UART0 Transmit	Output
		6	SLWIR3LB	Loopback SPI Slave I/O Pin for 3-Wire Mode	Bidirectional 3-state
		7	M1nCE1	SPI Master 1 Chip Enable 1	Output

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
F5	8	0	M1SCL	I^2C Master 1 Clock	Open Drain Output
		1	M1SCK	SPI Master 1 Clock	Output
		2	M0nCE4	SPI Master 0 Chip Enable 4	Output
		3	GPIO8	General Purpose I/O	Input/ Output
		4	M2nCE4	SPI Master 2 Chip Enable 4	Output
		5	M1SCKLB	SPI Master 1 Clock (loopback)	Output
		6	UART1TX	UART1 Transmit	Output
		7	M1SCLLB	I^2C Master 1 Clock (loopback)	Open Drain Output
F7	9	0	M1SDA	I^2C Master 1 Data	Bidirectional Open Drain
		1	M1MISO	SPI Master 1 Input Data	Input
		2	M0nCE5	SPI Master 0 Chip Enable 5	Output
		3	GPIO9	General Purpose I/O	Input/ Output
		4	M4nCE5	SPI Master 4 Chip Enable 5	Output
		5	SLMISOLB	SPI Slave Output Data (loopback)	Output
		6	UART1RX	UART1 Receive	Input
		7	SLSDALB	I^2C Slave Data (loopback)	Bidirectional Open Drain

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
F4	10	0	M1WIR3	SPI Master 1 I/O Pin for 3-Wire Mode	Bidirectional 3-state
		1	M1MOSI	SPI Master 1 Output Data	Output
		2	M0nCE6	SPI Master 0 Chip Enable 6	Output
		3	GPIO10	General Purpose I/O	Input/ Output
		4	M2nCE6	SPI Master 2 Chip Enable 6	Output
		5	UA1RTS	UART1 Request to Send (RTS)	Output
		6	M4nCE4	SPI Master 4 Chip Enable 4	Output
		7	SLWIR3LB	Loopback SPI Slave I/O Pin for 3-Wire Mode (loopback)	Bidirectional 3-state
B6	11	0	ADCSE2	Analog to Digital Converter SE In2	Analog Input
		1	M0nCE0	SPI Master 0 Chip Enable 0	Output
		2	CLKOUT	Oscillator Output Clock	Output
		3	GPIO11	General Purpose I/O	Input/ Output
		4	M2nCE7	SPI Master 2 Chip Enable 7	Output
		5	UA1CTS	UART1 Clear to Send (CTS)	Input
		6	UART0RX	UART0 receive	Input
		7	PDM_DATA	PDM audio data input	Input

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
B7	12	0	ADCD0NSE9	Analog to Digital Converter Diff In0 Neg	Analog Input
		1	M1nCE0	SPI Master 1 Chip Enable 0	Output
		2	TCTA0	Timer/Counter A0	Output
		3	GPIO12	General Purpose I/O	Input/ Output
		4	CLKOUT	Oscillator output clock	Output
		5	PDM_CLK	PDM Clock output	Output
		6	UA0CTS	UART0 Clear to Send (CTS)	Input
		7	UART1TX	UART1 Transmit	Output
D6	13	0	ADCD0PSE8	Analog to Digital Converter Diff In0 Pos	Analog Input
		1	M1nCE1	SPI Master 1 Chip Enable 1	Output
		2	TCTB0	Timer/Counter B0	Output
		3	GPIO13	General Purpose I/O	Input/ Output
		4	M2nCE3	SPI Master 2 Chip Enable 3	Output
		5	RSVD	Reserved for future use	
		6	UA0RTS	UART0 RTS (Request to Send)	Output
		7	UART1RX	UART1 Receive	Input
E8	14	0	ADCD1P	Analog to Digital Converter Diff In1 Pos	Analog Input
		1	M1nCE2	SPI Master 1 Chip Enable 2	Output
		2	UART1TX	UART1 Transmit	Output
		3	GPIO14	General Purpose I/O	Input/ Output
		4	M2nCE1	SPI Master 1 Chip Enable 1	Output
		5	RSVD	Reserved for future use	
		6	SWDCK	Software debug clock	Input
		7	32KHz_XT	32 kHz clock	Output

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
D7	15	0	ADCD1N	Analog to Digital Converter Diff In1 Neg	Analog Input
		1	M1nCE3	SPI Master 1 Chip Enable 3	Output
		2	UART1RX	UART1 Receive	Input
		3	GPIO15	General Purpose I/O	Input/ Output
		4	M2nCE2	SPI Master 2 Chip Enable 2	Output
		5	RSVD	Reserved	
		6	SWDIO	Serial Wire Data I/ O	Bidirectional 3-state
		7	SWO	Serial Wire Debug	Output
C5	16	0	ADCSE0	Analog to Digital Converter SE In0	Input
		1	M0nCE4	SPI Master 0 Chip Enable 4	Output
		2	TRIG0	ADC Trigger Input 0	Input
		3	GPIO16	General Purpose I/O	Input/ Output
		4	M2nCE3	SPI Master 2 Chip Enable 3	Output
		5	CMPIN0	Voltage compara- tor input 0	Analog Input
		6	UART0TX	UART0 transmit	Output
		7	UA1RTS	UART1 Request to Send (RTS)	Output
C4	17	0	CMPRF1	Voltage Compara- tor Reference 1	Analog Input
		1	M0nCE1	SPI Master 0 Chip Enable 1	Output
		2	TRIG1	ADC Trigger Input 1	Input
		3	GPIO17	General Purpose I/O	Input/ Output
		4	M4nCE3	SPI Master 4 Chip Enable 3	Output
		5	RSVD	Reserved for future use	
		6	UART0RX	UART0 Receive	Input
		7	UA1CTS	UART1 Clear to Send (CTS)	Input

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
D3	18	0	CMPIN1	Voltage Comparator Input 1	Analog Input
		1	M0nCE2	SPI Master 0 Chip Enable 2	Output
		2	TCTA1	Timer/Counter A1	Output
		3	GPIO18	General Purpose I/O	Input/ Output
		4	M4nCE1	SPI Master 4 Chip Enable 1	Output
		5	RSVD	Reserved for future use	
		6	UART1TX	UART1 Transmit	Output
		7	32KHz_XT	32kHz clock	Output
C3	19	0	CMPRF0	Comparator Reference 0	Analog Input
		1	M0nCE3	SPI Master 0 Chip Enable 3	Output
		2	TCTB1	Timer/Counter B1	Output
		3	GPIO19	General Purpose I/O	Input/ Output
		4	TCTA1	Timer/counter A1	Output
		5	RSVD	Reserved for future use	
		6	UART1RX	UART1 receive	Input
		7	I2S_BCLK	I2S Bit Clock	Input
F6	20	0	SWDCK	Software Debug Clock	Input
		1	M1nCE5	SPI Master 1 Chip Enable 5	Output
		2	TCTA2	Timer/Counter A2	Output
		3	GPIO20	General Purpose I/O	Input/ Output
		4	UART0TX	UART0 Transmit	Output
		5	UART1TX	UART1 Transmit	Output
		6	RSVD	Reserved for future use	
		7	RSVD	Reserved for future use	

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
E3	21	0	SWDIO	Software Data I/O	Bidirectional 3-state
		1	M1nCE6	SPI Master 1 Chip Enable 6	Output
		2	TCTB2	Timer/Counter B2	Output
		3	GPIO21	General Purpose I/O	Input/ Output
		4	UART0RX	UART0 Receive	Input
		5	UART1RX	UART1 Receive	Input
		6	RSVD	Reserved for future use	
		7	RSVD	Reserved for future use	
G3	22	0	UART0TX	UART0 Transmit	Output
		1	M1nCE7	SPI Master 1 Chip Enable 7	Output
		2	TCTA3	Timer/Counter A3	Output
		3	GPIO22	General Purpose I/O	Input/ Output
		4	PDM_CLK	PDM Clock Out-put	Output
		5	RSVD	Reserved for future use	
		6	TCTB1	Timer/counter B1	Output
		7	SWO	Serial Wire Debug	Output
B5	29	0	ADCSE1	Analog to Digital Converter SE In1	Analog Input
		1	M1nCE6	SPI Master 1 Chip Enable 6	Output
		2	TCTA2	Timer/Counter A2	Output
		3	GPIO29	General Purpose I/O	Input/ Output
		4	UA0CTS	UART0 Clear to Send (CTS)	Input
		5	UA1CTS	UART1 Clear to Send (CTS)	Input
		6	M4nCE0	SPI Master 4 Chip Enable 0	Output
		7	PDM_DATA	PDM audio data input to chip	Input

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
D2	30	0	RSVD	Reserved for future use	
		1	M1nCE7	SPI Master 1 Chip Enable 7	Output
		2	TCTB2	Timer/Counter B2	Output
		3	GPIO30	General Purpose I/O	Input/ Output
		4	UART0TX	UART0 Transmit	Output
		5	UA1RTS	UART1 Request to Send (RTS)	Output
		6	RSVD	Reserved for future use	
		7	I2S_DAT	I2S Data output	Output
G4	35	0	ADCSE7	Analog to Digital Converter SE In7	Analog Input
		1	M1nCE0	SPI Master 1 Chip Enable 0	Output
		2	UART1TX	UART1 Transmit	Output
		3	GPIO35	General Purpose I/O	Input/ Output
		4	M4nCE6	SPI Master 4 Chip Enable 6	Output
		5	TCTA1	Timer/counter A1	Output
		6	UA0RTS	UART0 Request to Send (RTS)	Output
		7	M3nCE2	SPI Master 3 Chip Enable 2	Output
G5	36	0	TRIG1	ADC Trigger input	Input
		1	M1nCE1	SPI Master 1 Chip Enable 1	Output
		2	UART1RX	UART1 Receive	Input
		3	GPIO36	General Purpose I/O	Input/ Output
		4	32KHz_XT	32 kHz Clock	Output
		5	M2nCE0	SPI Master 2 Chip Enable 0	Output
		6	UA0CTS	UART0 Clear to Send (CTS)	Input
		7	M3nCE3	SPI Master 3 Chip Enable 3	Output

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
E6	39	0	UART0TX	UART0 transmit	Output
		1	UART1TX	UART1 Transmit	Output
		2	CLKOUT	Oscillator Output Clock	Output
		3	GPIO39	General Purpose I/O	Input/ Output
		4	M4SCL	I2C Master 4 Clock	Output
		5	M4SCK	SPI Master 4 Clock	Output
		6	M4SCKLB	SPI M4 CLKIOUT->CLKIN (loop-back)	Input
		7	M4SCLLB	I2C M4 CLKIOUT->CLKIN (loop-back)	Input
E7	40	0	UART0RX	UART0 receive	Input
		1	UART1RX	UART1 Receive	Input
		2	TRIG0	ADC trigger	Input
		3	GPIO40	General Purpose I/O	Input/ Output
		4	M4SDA	I2C Master 4 Data	Bidirectional Open Drain
		5	M4MISO	SPI Master 4 data in	Input
		6	SLMISOLB	SPI slave output data (loopback)	Output
		7	SLSDALB	I2C Slave I/O data	Bidirectional Open Drain
H2	41	0	M2nCE1	SPI Master 2 chip enable 1	Output
		1	CLKOUT	Oscillator Output Clock	Output
		2	SWO	Serial Wire Debug Output	Output
		3	GPIO41	General Purpose I/O	Input/ Output
		4	M3nCE5	IO Master 3 Chip Enable	Output
		5	M5nCE7	IO Master 5 Chip Enable	Output
		6	M4nCE2	IO Master 4 Chip Enable	Output
		7	UA0RTS	UART0 Request to Send (RTS)	Output

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 1: Pin List and Function Table

Apollo2 Blue LGA Number	GPIO Pad Number	Function Select Number	Pad Function Name	Description	Pin Type
F3	44	0	UA1RTS	UART1 Request to Send (RTS)	Output
		1	M0nCE2	SPI Master 0 Chip Enable 2	Output
		2	TCTA1	Timer/Counter A1	Output
		3	GPIO44	General Purpose I/O	Input/ Output
		4	M4WIR3	SPI Master 4 I/O pin for 3-wire mode	Bidirectional 3-state
		5	M4MOSI	SPI Master 4 Data Out	Output
		6	M5nCE6	SPI Master 5 Chip Enable 6	Output
		7	SLWIR3LB	SPI Slave I/O pin for 3-wire	Bidirectional 3-state

©2017 Ambiq Micro, Inc.
All rights reserved.

2. System Core

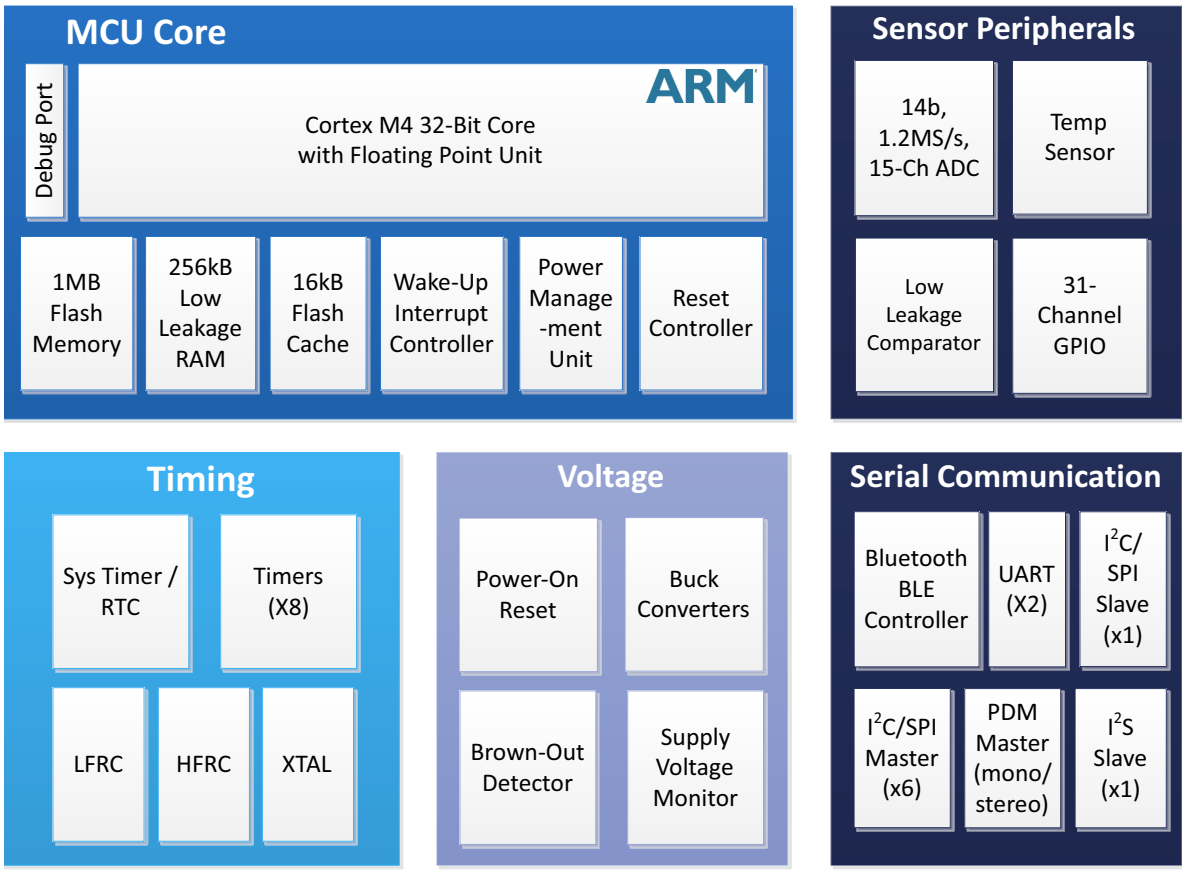


Figure 2. Block Diagram for the Ultra-Low Power Apollo2 Blue

The ultra-low power Apollo2 Blue, shown in Figure 2, is an ideal solution for battery-powered applications requiring sensor measurement and data analysis. In a typical system, the Apollo2 Blue serves as an applications processor for one or more sensors and has an integrated BLE radio. The Apollo2 Blue can measure analog sensor outputs using an integrated 14 bit ADC and digital sensor outputs using the integrated serial master ports. The Cortex-M4 core with Floating Point Unit (referred to throughout this document as “M4”, “M4 Core” or “Cortex-M4”) integrated in the Apollo2 Blue is capable of running complex data analysis and sensor fusion algorithms to process the sensor data. The Cortex-M4 core with FPU also enables accelerated time-to-market since application code may be efficiently executed in floating point form without the need to perform extensive fixed point optimizations.

With unprecedented energy efficiency for sensor conversion and data analysis, the Apollo2 Blue enables months and years of battery life for products only achieving days or months of battery life today. For example, a fitness monitoring device with days or weeks of life on a rechargeable battery could be redesigned to achieve a year or more of life on a non-rechargeable battery. Similarly the Apollo2 Blue enables the use of more complex sensor processing algorithms due to its extremely low active mode power of less than 10 µA/MHz. By using the Apollo2 Blue, the aforementioned fitness monitoring device

©2017 Ambiq Micro, Inc.
All rights reserved.

could achieve the current multi-day or multi-week battery life while adding new computation-intensive functions like context detection and gesture recognition.

2.1 MCU Sub-system

At the center of the Apollo2 Blue is a 32-bit ARM Cortex-M4 processor with Floating Point Unit with several tightly coupled peripherals. The Ambiq Micro implementation of the Cortex-M4 core delivers both greater performance and much lower power than 8-bit, 16-bit, and other comparable 32-bit cores. Code and data may be stored in the 1 MB Flash Memory and the 256 KB Low Leakage RAM. The Wake-Up Interrupt Controller (WIC) coupled with the Cortex-M4 supports sophisticated and configurable sleep state transitions with a variety of interrupt sources.

An integrated Bluetooth low energy controller provides support for Bluetooth 4.2 at 3mA Rx/Tx. Apollo2 Blue supports up to 7dBm transmit power with optional external power amplifier controls to enable even higher transmit range.

A rich set of sensor peripherals enable the monitoring of several sensors. An integrated temperature sensor enables the measurement of ambient temperature. A scalable ultra-low power Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) monitors the temperature sensor, several internal voltages, and up to eight external sensor signals. The ADC is uniquely tuned for minimum power with a configurable measurement mode that does not require MCU intervention. In addition to integrated analog sensor peripherals, I^2C/SPI/PDM master ports and/or UART ports enables the MCU to communicate with external sensors and radios (such as Bluetooth transceivers) that have digital outputs.

The Apollo2 Blue also includes a set of timing peripherals and an RTC which is based on Ambiq's AM08XX and AM18XX Real-Time Clock (RTC) families. The general purpose Timer/Counter Module (CTIMER), 32-bit System Timer (STIMER), and the RTC may be driven independently by one of three different clock sources: a low frequency RC oscillator, a high frequency RC oscillator, and a 32.768 kHz crystal (XTAL) oscillator. These clock sources use the proprietary advanced calibration techniques developed for the AM08XX and AM18XX products that achieve XTAL-like accuracy with RC-like power. Additionally, the Apollo2 Blue includes clock reliability functions first offered in the AM08XX and AM18XX products. For example, the RTC can automatically switch from an XTAL source to an RC source in the event of an XTAL failure.

As with any ARM-based MCU, the Apollo2 Blue is supported by a complete suite of standard software development tools. Ambiq Micro provides drivers for all peripherals along with basic application code to shorten development times. Software debug is facilitated by the addition of an Instrumentation Trace Macrocell (ITM), a Trace Port Interface Unit (TPIU) and through the use of a Serial Wire Debugger interface (SWD).

©2017 Ambiq Micro, Inc.
All rights reserved.

2.2 Apollo2 Blue Bluetooth Controller

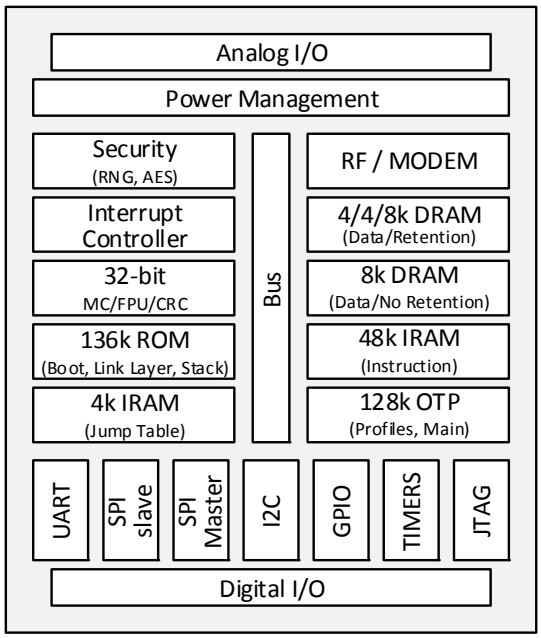


Figure 3. Hardware Architecture

In Figure 3, the hardware architecture of the BLE controller is shown. It has a 32-bit MCU which efficiently controls the movement of data between the RF modem, memory, and the digital interfaces. The 32-bit MCU includes a floating point unit (FPU) for efficient implementation of sensor algorithms. A CRC coprocessor is also included for efficient verification of program memory. Memories are included for the following functions (size shown in parentheses):

- ROM (136 kB) – used for the start-up sequence, Bluetooth low energy link layer and stack
- RAM (48 kB) – used for application development
- RAMs (4, 4, and 12 kB) – used for data with optional state retention
- dRAM (8 kB) – used for data without state retention
- iRAM (4 kB) – used for the sub-routine jump table
- OTP (128 kB) – used for configuration data, Bluetooth profiles, and applications

The memory architecture is divided into several different power domains for power consumption optimizations. When a memory is not being used, it can be switched off to reduce power consumption. During Bluetooth connected sleep mode the entire MCU subsystem can be shut off when only the power management system and required state retention memories (if any) need to be powered. The power management system will properly wake up the MCU subsystem when it is needed. The RF modem is also on a separate supply domain and is turned on and off as needed in order to minimize energy consumption. For detailed explanation of the BLE Controller, register at https://forums.emdeveloper.com/index.php to download the latest documents, SDK, configuration tools, etc.

©2017 Ambiq Micro, Inc.
All rights reserved.

3. MCU Core Details

At the center of the Apollo2 Blue is a 32-bit ARM Cortex-M4 core with the floating point option. This 3-stage pipeline implementation of the ARM v7-M architecture offers highly efficient processing in a very low power design. The ARM M DAP enables debugging access via a Serial Wire Interface from outside of the MCU which allows access to all of the memory and peripheral devices of the MCU. The M4 core offers some other advantages including:

- Single 4 GB memory architecture with all Peripherals being memory-mapped
- Low-Power Consumption Modes:
  - Active
  - Sleep
  - Deep-Sleep
  - Power-Off
- Interrupts and Events
  - NVIC – interrupt controller
  - WIC – Wake-Up Interrupt Controller
  - Sleep-on-Exit (reduces interrupt overhead, used in an ISR SW structure)
  - WFI (enter sleep modes, wait for interrupts)

The following sections provide behavioral and performance details about each of the peripherals controlled by the MCU core. Where multiple instances of a peripheral exist on Apollo2 Blue (e.g., the six I^2C/SPI master modules), base memory addresses for the registers are provided for each and noted as INSTANCE 0, INSTANCE 1, etc.

3.1 Interrupts

Within the MCU, multiple peripherals can generate interrupts. In some cases, a single peripheral may be able to generate multiple different interrupts. Each interrupt signal generated by a peripheral is connected back to the M4 core in two places. First, the interrupts are connected to the Nested Vectored Interrupt Controller, NVIC, in the core. This connection provides the standard changes to program flow associated with interrupt processing. Additionally, they are connected to the WIC outside of the core, allowing the interrupt sources to wake the M4 core when it is in a deep sleep (SRPG) mode.

The MCU supports the M4 NMI as well as the normal interrupt types. For details on the Interrupt model of the M4, please see the “**Cortex-M4 Devices Generic User Guide,**” document number DUI0553A.

Below is the M4 Vector Table for Apollo2 Blue:

©2017 Ambiq Micro, Inc.
All rights reserved.

Exception Number	IRQ Number	Offset	Vector	Peripheral/Description
255	239	0x03FC	IRQ239	
.		.	.	
.		0x00C4		
.		0x00C0	IRQ28-31	SW INT[0-3]
.		0x00AC	IRQ27	Reserved
.		0x008C	IRQ19-26	Stimer Compare[0:7]
.		0x0088	IRQ18	Stimer Capture/Overflow
.		0x0084	IRQ17	PDM
.		0x0080	IRQ16	ADC
.		0x007C	IRQ15	UART1
.		0x0078	IRQ14	UART0
.		0x0074	IRQ13	Counter/Timers
.		0x0070	IRQ12	GPIO
.		0x006C	IRQ11	I^2C/SPI Master 5
.		0x0068	IRQ10	I^2C/SPI Master 4
.		0x0064	IRQ9	I^2C/SPI Master 3
.		0x0060	IRQ8	I^2C/SPI Master 2
.		0x005C	IRQ7	I^2C/SPI Master 1
.		0x0058	IRQ6	I^2C/SPI Master 0
.		0x0054	IRQ5	I^2C/SPI Slave Register Access
.		0x0050	IRQ4	I^2C/SPI Slave
.		0x004C	IRQ3	Voltage Comparator
18	2	0x0048	IRQ2	Clock Control and RTC
17	1	0x0044	IRQ1	Watchdog Timer
16	0	0x0040	IRQ0	Brownout Detection
15	-1	0x003C	Systick	
14	-2	0x0038	PendSV	
13			Reserved	
12			Reserved for Debug	
11	-5	0x002C	SVCall	
10			Reserved	
9				
8				
7				
6	-10	0x0018	Usage Fault	
5	-11	0x0014	Bus Fault	
4	-12	0x0010	Memory management Fault	
3	-13	0x000C	Hard fault	
2	-14	0x0008	NMI	Unused
1		0x0004	Reset	
		0x0000	Initial SP value	

Figure 4. ARM Cortex-M4 Vector Table for Apollo2 Blue

©2017 Ambiq Micro, Inc.
All rights reserved.

The Cortex-M4 allows the user to assign various interrupts to different priority levels based on the requirements of the application. In this MCU implementation, 8 different priority levels are available.

One additional feature of the M4 interrupt architecture is the ability to relocate the Vector Table to a different address. This could be useful if the application requires a different set of interrupt service routines for a particular mode of an application. The software could move the Vector Table into SRAM and reassign the interrupt service routine entry addresses as needed.

Hardware interrupts are assigned in the MCU to the M4 NVIC as follows:

Table 2: MCU Interrupt Assignments

IRQ	Peripheral/Description
NMI	Unused
IRQ0	Brownout Detection
IRQ1	Watchdog Timer
IRQ2	Clock Control and RTC
IRQ3	Voltage Comparator
IRQ4	I^2C / SPI Slave
IRQ5	I^2C / SPI Slave Register Access
IRQ6	I^2C / SPI Master0
IRQ7	I^2C / SPI Master1
IRQ8	I^2C / SPI Master2
IRQ9	I^2C / SPI Master3
IRQ10	I^2C / SPI Master4
IRQ11	I^2C / SPI Master5
IRQ12	GPIO
IRQ13	Counter/Timers
IRQ14	UART0
IRQ15	UART1
IRQ16	ADC
IRQ17	PDM
IRQ18	STimer Capture/Overflow
IRQ19-26	STimer Compare[0:7]
IRQ27	Reserved
IRQ28-31	SW INT[0-3]

©2017 Ambiq Micro, Inc.
All rights reserved.

3.2 Memory Map

ARM has a well-defined memory map for devices based on the ARM v7-M Architecture. The M4 further refines this map in the area of the Peripheral and System address ranges. Below is the system memory map as defined by ARM:

Table 3: ARM Cortex-M4 Memory Map

Address	Name	Executable	Description
0x00000000 – 0x1FFFFFFF	Code	Y	ROM or Flash Memory
0x20000000 – 0x3FFFFFFF	Reserved	N	Reserved
0x40000000 – 0x5FFFFFFF	Peripheral	N	On-chip peripheral address space
0x60000000 – 0x9FFFFFFF	External RAM	Y	External / Off-chip Memory
0xA0000000 – 0xDFFFFFFF	External Device	N	External device memory
0xE0000000 – 0xE00FFFFF	Private Peripheral Bus	N	NVIC, System timers, System Control Block
0xE0100000 – 0xFFFFFFFF	Vendor	N	Vendor Defined

The MCU-specific implementation of this memory map is as follows:

Table 4: MCU System Memory Map

Address	Name	Executable	Description
0x00000000 – 0x000FFFFF	Flash	Y	Flash Memory
0x00100000 – 0x07FFFFFF	Reserved	X	No device at this address range
0x08000000 – 0x08000FFF	Boot Loader ROM	Y	Execute Only Boot Loader and Flash Helper Functions.
0x08001000 – 0x0FFFFFFF	Reserved	X	No device at this address range
0x10000000 – 0x1003FFFF	SRAM	Y	Low-power SRAM
0x10040000 – 0x3FFFFFFF	Reserved	X	No device at this address range
0x40000000 – 0x4FFFFFFF	Peripheral – APB	N	APB Peripheral devices
0x50000000 – 0x5FFFFFFF	Peripheral – AHB	N	AHB Peripheral devices
0x60000000 – 0xDFFFFFFF	Reserved	X	No device at this address range
0xE0000000 – 0xE00FFFFF	PPB	N	NVIC, System timers, System Control Block
0xE0100000 – 0xEFFFFFFF	Reserved	X	No device at this address range
0xF0000000 – 0xF0000FFF	Reserved	X	No device at this address range
0xF0001000 – 0xFFFFFFFF	Reserved	X	No device at this address range

Peripheral devices within the memory map are allocated on 4 KB boundaries, allowing each device up to 1024 32-bit control and status registers. Peripherals will return undefined read data when an attempt to access a register which does not exist occurs. Peripherals, whether accessed via the APB or the AHB, will always accept any write data sent to their registers without attempting to return an ERROR response. Specifically, a write to a read-only register would just become a don’t-care write.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 5 shows the address mapping for the peripheral devices of the Base Platform.

Table 5: MCU Peripheral Device Memory Map

Address	Device
0x40000000 – 0x400003FF	Reset / BoD Control
0x40000400 – 0x40003FFF	Reserved
0x40004000 – 0x400041FF	Clock Generator / RTC
0x40004200 – 0x40007FFF	Reserved
0x40008000 – 0x400083FF	Timers
0x40008400 – 0x4000BFFF	Reserved
0x4000C000 – 0x4000C3FF	Voltage Comparator
0x4000C400 – 0x4000FFFF	Reserved
0x40010000 – 0x400103FF	GPIO Control
0x40010400 – 0x40017FFF	Reserved
0x40018000 – 0x40018FFF	Flash Cache Control
0x40019000 – 0x4001BFFF	Reserved
0x4001C000 – 0x4001C3FF	UART0
0x4001C400 – 0x4001CFFF	Reserved
0x4001D000 – 0x4001D3FF	UART1
0x4001D400 – 0x4001FFFF	Reserved
0x40020000 – 0x400203FF	Miscellaneous Control
0x40020400 – 0x40020FFF	Reserved
0x40021000 – 0x400213FF	Power Control
0x40021400 – 0x40023FFF	Reserved
0x40024000 – 0x400243FF	Watchdog Timer
0x40024400 – 0x4FFFFFFF	Reserved
0x50000000 – 0x500003FF	I^2C / SPI Slave
0x50000400 – 0x50003FFF	Reserved
0x50004000 – 0x500043FF	I^2C / SPI Master0
0x50004400 – 0x50004FFF	Reserved
0x50005000 – 0x500053FF	I^2C / SPI Master1
0x50005400 – 0x50005FFF	Reserved
0x50006000 – 0x500063FF	I^2C / SPI Master2
0x50006400 – 0x50006FFF	Reserved
0x50007000 – 0x500073FF	I^2C / SPI Master3
0x50007400 – 0x50007FFF	Reserved
0x50008000 – 0x500083FF	I^2C / SPI Master4
0x50008400 – 0x50008FFF	Reserved
0x50009000 – 0x500093FF	I^2C / SPI Master5

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 5: MCU Peripheral Device Memory Map

Address	Device
0x50009400 – 0x5000FFFF	Reserved
0x50010000 – 0x500103FF	ADC
0x50010400 – 0x50010FFF	Reserved
0x50011000 – 0x500113FF	PDM
0x50011400 – 0x5001FFFF	Reserved
0x50020000 – 0x5002FFFF	Flash OTP
0x50030000 – 0x5FFFFFFF	Reserved

3.3 Memory Protection Unit (MPU)

The Apollo2 Blue includes an MPU which is a core component for memory protection. The M4 processor supports the standard ARMv7 *Protected Memory System Architecture* model. The MPU provides full support for:

- Protection regions.
- Overlapping protection regions, with ascending region priority:
  - 7 = highest priority
  - 0 = lowest priority.
- Access permissions
- Exporting memory attributes to the system.

MPU mismatches and permission violations invoke the programmable-priority MemManage fault handler. See the ARM®v7-M Architecture Reference Manual for more information.

You can use the MPU to:

- Enforce privilege rules.
- Separate processes.
- Enforce access rules.

3.4 System Busses

The ARM Cortex-M4 utilizes 3 instances of the AMBA AHB bus for communication with memory and peripherals. The ICode bus is designed for instruction fetches from the ‘Code’ memory space while the DCode bus is designed for data and debug accesses in that same region. The System bus is designed for fetches to the SRAM and other peripheral devices of the MCU.

The Apollo2 Blue maps the available SRAM memory onto an address space within the ‘Code’ memory space. This gives the user the opportunity to perform instruction and data fetches from the lower-power SRAM to effectively lower the power consumption of the MCU.

The peripherals of the Apollo2 Blue which are infrequently accessed are located on an AMBA APB bus. A bridge exists which translates the accesses from the System AHB to the APB. Accesses to these peripherals will inject a single wait-state on the AHB during any access cycle.

3.5 Power Management

The Power Management Unit (PMU) is a finite-state machine that controls the transitions of the MCU between power modes. When moving from Active Mode to Deep Sleep Mode, the PMU manages the

©2017 Ambiq Micro, Inc.
All rights reserved.

state-retention capability of the registers within the Cortex-M4 core and also controls the shutdown of the voltage regulators of the MCU. Once in the Deep Sleep Mode, the PMU, in conjunction with the Wake-Up Interrupt Controller, waits for a wakeup event. When the event is observed, the PMU begins the power restoration process by re-enabling the on-chip voltage regulators and restoring the CPU register state. The M4 is then returned to active mode once all state is ready.

The Apollo2 Blue power modes are described in the subsequent discussion along with the operation of the PMU.

3.5.1 Cortex-M4 Power Modes

The ARM Cortex-M4 defines the following 3 power modes:

- Active
- Sleep
- Deep Sleep

In addition to the above ARM-defined modes, the Apollo2 Blue will support a Shutdown mode in which the entire device is powered down except for the logic required to support a Power-On Reset.

Each mode is described below.

3.5.1.1 Active Mode

In the Active Mode, the M4 is powered up, clocks are active, and instructions are being executed. In this mode, the M4 expects all (enabled) devices attached to the AHB and APB to be powered and clocked for normal access. All of the non-debug ARM clocks (FCLK, HCLK) are active in this state.

To transition from the Active Mode to any of the lower-power modes, a specific sequence of instructions is executed on the M4 core. First, specific bits in the *ARMv7-M System Control Register* must be set to determine the mode to enter. See page B3-269 of the *ARMv7-M Architecture Reference Manual* for more details.

After the SCR is setup, code can enter the low-power states using one of the 2 following methods:

- Execute a Wait-For-Interrupt (WFI) instruction.
- Set the SLEEPONEXIT bit of the SCR such that the exit from an ISR will automatically return to a sleep state.

The M4 will enter a low-power mode after one of these are performed (assuming all conditions are met) and remain there until some event causes the core to return to Active Mode. The possible reasons to return to Active Mode are:

- A reset
- An enabled Interrupt is received by the NVIC
- A Debug Event is received from the DAP

3.5.1.2 Sleep Mode

In the Sleep Mode, the M4 is powered up, but the clocks (HCLK, FCLK) are not active. The power supply is still applied to the M4 logic such that it can immediately become active on a wakeup event and begin executing instructions.

3.5.1.3 Deep Sleep Mode

In the Deep Sleep Mode, the M4 enters SRPG mode where the main power is removed, but the flops retain their state. The clocks are not active, and the MCU clock sources for HCLK and FCLK can be deactivated. To facilitate the removal of the source supply and entry into SRPG mode, the M4 will

©2017 Ambiq Micro, Inc.
All rights reserved.

handshake with the Wake-up Interrupt Controller and Power Management Unit and set up the possible wakeup conditions.

3.5.2 System Power Modes

In addition to the CPU power states, there are system power states defined as follows.

3.5.2.1 SYS Active (S_{ACT})

CPU is in Active Mode and executing instructions. All peripheral devices are on and available.

3.5.2.2 SYS Sleep Mode 0 (S_{S0})

In SYS Sleep Mode 0, this is a low power state for the MCU. In this mode, all SRAM memory is retained (256KB), Flash memory is in standby, HFRC is on, main core clock domain is gated but peripheral clock domains can be on. CPU is in Sleep Mode.

This state can be entered if a peripheral device (SPI/UART/I2C) is actively transferring data and the time window is sufficient for CPU to enter Sleep Mode but is not long enough to go into a Deep Sleep Mode.

3.5.2.3 SYS Sleep Mode 1 (S_{S1})

In SYS Sleep Mode 1, this is a low power state for the MCU. In this mode, all SRAM memory is retained (256 KB), Flash memory is in standby, HFRC is on, all functional clocks are gated. CPU is in Sleep Mode.

This state can be entered if a no peripheral device (SPI/UART/I2C) is actively transferring data, however, communication may occur within a short time window which will prevent the CPU from entering Deep Sleep Mode (and subsequently the system from entering a lower power state).

This state is also referred to as “Active Idle”. In other words, all power domains are powered on, but all clocks are gated. This state is a good power baseline for the system as it represents the active mode DC power level. Typically the power in this state is dominated by leakage and always-on functional blocks.

3.5.2.4 SYS Deep Sleep Mode 0 (S_{DS0})

In SYS Deep Sleep Mode 0, this is a deep low power state for the MCU. In this mode, SRAM is in retention (capacity controlled by software), cache memory is in retention (16 KB), Flash memory is in power down, HFRC is on, main core power domain is off but peripheral power domains can be on. CPU is in Deep Sleep. Core logic state is retained.

This state can be entered if a peripheral device (SPI/UART/I2C) is actively (or intermittently) transferring data but the window of acquisition is long enough to allow the CPU to go into a deeper low power state.

Note: For easier notation, SRAM memory retention is defined as follows:

- 256KB: $S_{DS0\text{-}256RET}$
- 128KB: $S_{DS0\text{-}128RET}$
- 64KB: $S_{DS0\text{-}64RET}$
- 8KB: $S_{DS0\text{-}8RET}$
- 0KB: S_{DS0}

3.5.2.5 SYS Deep Sleep Mode 1 (S_{DS1})

In SYS Deep Sleep Mode 1, this is a deep low power state for the MCU. In this mode, SRAM is in retention (capacity controlled by software), cache memory is powered down, Flash memory is in power down, HFRC

©2017 Ambiq Micro, Inc.
All rights reserved.

is on, main core power domain is off but peripheral power domains can be on. CPU is in Deep Sleep. Core logic state is retained.

This state can be entered if the latency to warm up the cache can be tolerated. This could be an extended wait for peripheral communication event.

Note: For easier notation, SRAM memory retention is defined as follows:

- 256KB: $S_{DS1\text{-}256RET}$
- 128KB: $S_{DS1\text{-}128RET}$
- 64KB: $S_{DS1\text{-}64RET}$
- 8KB: $S_{DS1\text{-}8RET}$
- 0KB: S_{DS1}

3.5.2.6 SYS Deep Sleep Mode 2 (S_{DS2})

In SYS Deep Sleep Mode 2, this is the minimum power state that the MCU can resume normal operation. In this mode, minimal SRAM memory is retained as needed for software to resume (note that SRAM can have 0-256 KB in retention depending on the software/system functional and latency requirements), Cache is powered off (no retention), Flash memory is in power down, HFRC is off, XTAL is ON, all internal switched power domains are off/gated. CPU is in Deep Sleep. Core logic state is retained.

Note: For easier notation, SRAM memory retention is defined as follows:

- 256KB: $S_{DS2\text{-}256RET}$
- 128KB: $S_{DS2\text{-}128RET}$
- 64KB: $S_{DS2\text{-}64RET}$
- 8KB: $S_{DS2\text{-}8RET}$
- 0KB: S_{DS2}

This state can be entered when all activity has suspended for a duration of time sufficient to sustain the longer exit latencies to resume. This could be a state where periodic data samples are taken and the data is locally processed/accumulated/transferred at long time intervals. This state can only be entered (vs S_{DS1}) if the peripheral devices are either not enabled/active or if the application can afford to save/restore the state of the controller(s) on entry/exit of this mode.

3.5.2.7 SYS Deep Sleep Mode 3 (S_{DS3})

In SYS Deep Sleep Mode 3, this is a deep sleep power state for the MCU. In this mode, no memory is in retention, all memory is powered down, LFRC is on (HFRC and XTAL are off), all internal switched power domains are off/gated. CPU is in Deep Sleep. Core logic state is retained. Single timer is running.

This state can be entered on long inactivity periods. Also can be used for very low power ADC sampling without CPU interaction.

3.5.2.8 SYS OFF Mode (S_{OFF})

In SYS OFF Mode, MCU is completely powered down with no power supplied. CPU is in shutdown mode with no state retention. Only Flash memory is retained.

This mode is controlled external to the MCU by removing power to the device.

©2017 Ambiq Micro, Inc.
All rights reserved.

3.5.3 Power Control

The power control block provides control and status for the power state of all of the power domains in the SoC. Software can control these blocks via power control registers within this block.

3.5.3.1 PWRCTRL Registers

PWR Controller Register Bank

INSTANCE 0 BASE ADDRESS:0x40021000

Power Controller register Bank - this is the place SW writes to.

3.5.3.1.1 Register Memory Map

Table 6: PWRCTRL Register Map

Address(s)	Register Name	Description
0x40021000	SUPPLYSRC	Memory and Core Voltage Supply Source Select Register
0x40021004	POWERSTATUS	Power Status Register for MCU supplies and peripherals
0x40021008	DEVICEEN	DEVICE ENABLES for SHELBY
0x4002100C	SRAMPWDINSLEEP	Powerdown an SRAM Banks in Deep Sleep mode
0x40021010	MEMEN	Disables individual banks of the MEMORY array
0x40021014	PWRONSTATUS	POWER ON Status
0x40021018	SRAMCTRL	SRAM Control register
0x4002101C	ADCSTATUS	Power Status Register for ADC Block
0x40021020	MISCOPT	Power Optimization Control Bits

©2017 Ambiq Micro, Inc.
All rights reserved.

3.5.3.1.2 PWRCTRL Registers

3.5.3.1.2.1SUPPLYSRC Register

Memory and Core Voltage Supply Source Select Register

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x40021000

Memory and Core Voltage Supply Source Select Register

Table 7: SUPPLYSRC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													SWITCH_LDO_IN_SLEE	COREBUCKEN	MEMBUCKEN

Table 8: SUPPLYSRC Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	RESERVED.
2	SWITCH_LDO_IN_SLEEP	0x1	RW	Switches the CORE DOMAIN from BUCK mode (if enabled) to LDO when CPU is in DEEP SLEEP. If all the devices are off then this does not matter and LDO (low power mode) is used EN = 0x1 - Automatically switch from CORE BUCK to CORE LDO when CPU is in DEEP SLEEP
1	COREBUCKEN	0x0	RW	Enables and Selects the Core Buck as the supply for the low-voltage power domain. EN = 0x1 - Enable the Core Buck for the low-voltage power domain.
0	MEMBUCKEN	0x0	RW	Enables and select the Memory Buck as the supply for the Flash and SRAM power domain. EN = 0x1 - Enable the Memory Buck as the supply for flash and SRAM.

3.5.3.1.2.2POWERSTATUS Register

Power Status Register for MCU supplies and peripherals

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x40021004

Power Status Register for MCU supplies and peripherals

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 9: POWERSTATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														COREBUCKON	MEMBUCKON

Table 10: POWERSTATUS Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	RESERVED.
1	COREBUCKON	0x0	RO	Indicates whether the Core low-voltage domain is supplied from the LDO or the Buck. LDO = 0x0 - Indicates the the LDO is supplying the Core low-voltage. BUCK = 0x1 - Indicates the the Buck is supplying the Core low-voltage.
0	MEMBUCKON	0x0	RO	Indicate whether the Memory power domain is supplied from the LDO or the Buck. LDO = 0x0 - Indicates the LDO is supplying the memory power domain. BUCK = 0x1 - Indicates the Buck is supplying the memory power domain.

3.5.3.1.2.3DEVICEEN Register

DEVICE ENABLES for SHELBY

OFFSET: 0x00000008

INSTANCE 0 ADDRESS: 0x40021008

DEVICE ENABLES for SHELBY

Table 11: DEVICEEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					PDM	ADC	UART1	UART0	IO_MASTER5	IO_MASTER4	IO_MASTER3	IO_MASTER2	IO_MASTER1	IO_MASTER0	IO_SLAVE

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 12: DEVICEEN Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	RESERVED.
10	PDM	0x0	RW	Enable PDM Digital Block EN = 0x1 - Enable PDM DIS = 0x0 - Disables PDM
9	ADC	0x0	RW	Enable ADC Digital Block EN = 0x1 - Enable ADC DIS = 0x0 - Disables ADC
8	UART1	0x0	RW	Enable UART 1 EN = 0x1 - Enable UART 1 DIS = 0x0 - Disables UART 1
7	UART0	0x0	RW	Enable UART 0 EN = 0x1 - Enable UART 0 DIS = 0x0 - Disables UART 0
6	IO_MASTER5	0x0	RW	Enable IO MASTER 5 EN = 0x1 - Enable IO MASTER 5 DIS = 0x0 - Disables IO MASTER 5
5	IO_MASTER4	0x0	RW	Enable IO MASTER 4 EN = 0x1 - Enable IO MASTER 4 DIS = 0x0 - Disables IO MASTER 4
4	IO_MASTER3	0x0	RW	Enable IO MASTER 3 EN = 0x1 - Enable IO MASTER 3 DIS = 0x0 - Disables IO MASTER 3
3	IO_MASTER2	0x0	RW	Enable IO MASTER 2 EN = 0x1 - Enable IO MASTER 2 DIS = 0x0 - Disables IO MASTER 2
2	IO_MASTER1	0x0	RW	Enable IO MASTER 1 EN = 0x1 - Enable IO MASTER 1 DIS = 0x0 - Disables IO MASTER 1
1	IO_MASTER0	0x0	RW	Enable IO MASTER 0 EN = 0x1 - Enable IO MASTER 0 DIS = 0x0 - Disables IO MASTER 0
0	IO_SLAVE	0x0	RW	Enable IO SLAVE EN = 0x1 - Enable IO SLAVE DIS = 0x0 - Disables IO SLAVE

©2017 Ambiq Micro, Inc.
All rights reserved.

3.5.3.1.2.4SRAMPWDINSLEEP Register

Powerdown an SRAM Banks in Deep Sleep mode

OFFSET: 0x0000000C

INSTANCE 0 ADDRESS: 0x4002100C

Powerdown an SRAM Banks in Deep Sleep mode

Table 13: SRAMPWDINSLEEP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CACHE_PWD_SLP	RSVD																				SRAMSLEEPPOWERDOWN										

Table 14: SRAMPWDINSLEEP Register Bits

Bit	Name	Reset	RW	Description
31	CACHE_P-WD_SLP	0x0	RW	Enable CACHE BANKS to power down in deep sleep EN = 0x1 - CACHE BANKS POWER DOWN in CORE SLEEP DIS = 0x0 - CACHE BANKS STAYS in Retention in CORE SLEEP
30:11	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 14: SRAMPWDINSLEEP Register Bits

Bit	Name	Reset	RW	Description
10:0	SRAMSLEEP-POWERDOWN	0x0	RW	Selects which SRAM banks are powered down in deep sleep mode, causing the contents of the bank to be lost. NONE = 0x0 - All banks retained GROUP0_SRAM0 = 0x1 - 0KB-8KB SRAM GROUP0_SRAM1 = 0x2 - 8KB-16KB SRAM GROUP0_SRAM2 = 0x4 - 16KB-24KB SRAM GROUP0_SRAM3 = 0x8 - 24KB-32KB SRAM GROUP1 = 0x10 - 32KB-64KB SRAMs GROUP2 = 0x20 - 64KB-96KB SRAMs GROUP3 = 0x40 - 96KB-128KB SRAMs GROUP4 = 0x80 - 128KB-160KB SRAMs GROUP5 = 0x100 - 160KB-192KB SRAMs GROUP6 = 0x200 - 192KB-224KB SRAMs GROUP7 = 0x400 - 224KB-256KB SRAMs SRAM8K = 0x1 - Do not Retain lower 8KB SRAM16K = 0x3 - Do not Retain lower 16KB SRAM32K = 0xF - Do not Retain lower 32KB SRAM64K = 0x1F - Do not Retain lower 64KB SRAM128K = 0x7F - Do not Retain lower 128KB ALLBUTLOWER8K = 0x7FE - All banks but lower 8k powered down. ALLBUTLOWER16K = 0x7FC - All banks but lower 16k powered down. ALLBUTLOWER24K = 0x7F8 - All banks but lower 24k powered down. ALLBUTLOWER32K = 0x7F0 - All banks but lower 32k powered down. ALLBUTLOWER64K = 0x7E0 - All banks but lower 64k powered down. ALLBUTLOWER128K = 0x780 - All banks but lower 128k powered down. ALL = 0x7FF - All banks powered down.

3.5.3.1.2.5MEMEN Register

Disables individual banks of the MEMORY array

OFFSET: 0x00000010

INSTANCE 0 ADDRESS: 0x40021010

Disables individual banks of the MEMORY array

Table 15: MEMEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CACHEB2	RSVD	CACHEB0	RSVD																FLASH1	FLASH0	SRAMEN										

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 16: MEMEN Register Bits

Bit	Name	Reset	RW	Description
31	CACHEB2	0x1	RW	Enable CACHE BANK 2 EN = 0x1 - Enable CACHE BANK 2 DIS = 0x0 - Disable CACHE BANK 2
30	RSVD	0x0	RO	Reserved
29	CACHEB0	0x1	RW	Enable CACHE BANK 0 EN = 0x1 - Enable CACHE BANK 0 DIS = 0x0 - Disable CACHE BANK 0
28:13	RSVD	0x0	RO	RESERVED.
12	FLASH1	0x1	RW	Enable FLASH1 EN = 0x1 - Enable FLASH1 DIS = 0x0 - Disables FLASH1
11	FLASH0	0x1	RW	Enable FLASH 0 EN = 0x1 - Enable FLASH 0 DIS = 0x0 - Disables FLASH 0
10:0	SRAMEN	0x7ff	RW	Enables power for selected SRAM banks (else an access to its address space to generate a Hard Fault). NONE = 0x0 - All banks disabled GROUP0_SRAM0 = 0x1 - 0KB-8KB SRAM GROUP0_SRAM1 = 0x2 - 8KB-16KB SRAM GROUP0_SRAM2 = 0x4 - 16KB-24KB SRAM GROUP0_SRAM3 = 0x8 - 24KB-32KB SRAM GROUP1 = 0x10 - 32KB-64KB SRAMs GROUP2 = 0x20 - 64KB-96KB SRAMs GROUP3 = 0x40 - 96KB-128KB SRAMs GROUP4 = 0x80 - 128KB-160KB SRAMs GROUP5 = 0x100 - 160KB-192KB SRAMs GROUP6 = 0x200 - 192KB-224KB SRAMs GROUP7 = 0x400 - 224KB-256KB SRAMs SRAM8K = 0x1 - ENABLE lower 8KB SRAM16K = 0x3 - ENABLE lower 16KB SRAM32K = 0xF - ENABLE lower 32KB SRAM64K = 0x1F - ENABLE lower 64KB SRAM128K = 0x7F - ENABLE lower 128KB SRAM256K = 0x7FF - ENABLE lower 256KB ALL = 0x7FF - All banks ENABLED

3.5.3.1.2.6PWRONSTATUS Register

POWER ON Status

OFFSET: 0x00000014

INSTANCE 0 ADDRESS: 0x40021014

POWER ON Status

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 17: PWRONSTATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD										PD_CACHEB2	RSVD	PD_CACHEB0	PD_GRP7_SRAM	PD_GRP6_SRAM	PD_GRP5_SRAM	PD_GRP4_SRAM	PD_GRP3_SRAM	PD_GRP2_SRAM	PD_GRP1_SRAM	PD_GRP0_SRAM3	PD_GRP0_SRAM2	PD_GRP0_SRAM1	PD_GRP0_SRAM0	PDADC	PD_FLAM1	PD_FLAM0	PD_PDM	PDC	PDB	PDA	PD_MCUL

Table 18: PWRONSTATUS Register Bits

Bit	Name	Reset	RW	Description
31:22	RSVD	0x0	RO	This bitfield is reserved for future use.
21	PD_CACHEB2	0x0	RO	This bit is 1 if power is supplied to CACHE BANK 2
20	RSVD	0x0	RO	Reserved
19	PD_CACHEB0	0x0	RO	This bit is 1 if power is supplied to CACHE BANK 0
18	PD_GRP7_SRAM	0x0	RO	This bit is 1 if power is supplied to SRAM domain PD_GRP7
17	PD_GRP6_SRAM	0x0	RO	This bit is 1 if power is supplied to SRAM domain PD_GRP6
16	PD_GRP5_SRAM	0x0	RO	This bit is 1 if power is supplied to SRAM domain PD_GRP5
15	PD_GRP4_SRAM	0x0	RO	This bit is 1 if power is supplied to SRAM domain PD_GRP4
14	PD_GRP3_SRAM	0x0	RO	This bit is 1 if power is supplied to SRAM domain PD_GRP3
13	PD_GRP2_SRAM	0x0	RO	This bit is 1 if power is supplied to SRAM domain PD_GRP2
12	PD_GRP1_SRAM	0x0	RO	This bit is 1 if power is supplied to SRAM domain PD_GRP1
11	PD_GRP0_SRAM3	0x0	RO	This bit is 1 if power is supplied to SRAM domain PD_SRAM0_3
10	PD_GRP0_SRAM2	0x0	RO	This bit is 1 if power is supplied to SRAM domain PD_SRAM0_2
9	PD_GRP0_SRAM1	0x0	RO	This bit is 1 if power is supplied to SRAM domain SRAM0_1
8	PD_GRP0_SRAM0	0x0	RO	This bit is 1 if power is supplied to SRAM domain SRAM0_0
7	PDADC	0x0	RO	This bit is 1 if power is supplied to domain PD_ADC

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 18: PWRONSTATUS Register Bits

Bit	Name	Reset	RW	Description
6	PD_FLAM1	0x0	RO	This bit is 1 if power is supplied to domain PD_FLAM1
5	PD_FLAM0	0x0	RO	This bit is 1 if power is supplied to domain PD_FLAM0
4	PD_PDM	0x0	RO	This bit is 1 if power is supplied to domain PD_PDM
3	PDC	0x0	RO	This bit is 1 if power is supplied to power domain C, which supplies IOM3-5.
2	PDB	0x0	RO	This bit is 1 if power is supplied to power domain B, which supplies IOM0-2.
1	PDA	0x0	RO	This bit is 1 if power is supplied to power domain A, which supplies IOS and UART0,1.
0	PD_MCUL	0x0	RO	This bit is 1 if power is supplied to power domain PD_MCUL.

3.5.3.1.2.7SRAMCTRL Register

SRAM Control register

OFFSET: 0x00000018

INSTANCE 0 ADDRESS: 0x40021018

SRAM Control register

Table 19: SRAMCTRL Register

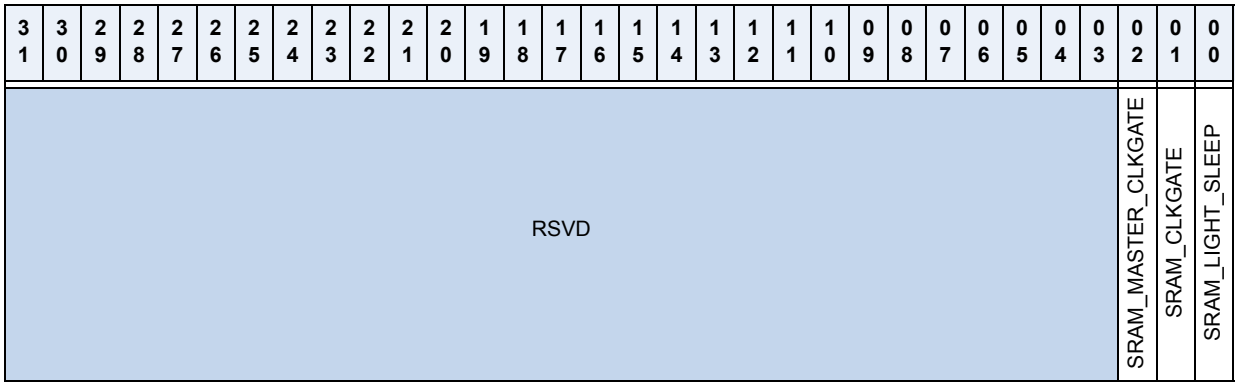


Table 20: SRAMCTRL Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	This bitfield is reserved for future use.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 20: SRAMCTRL Register Bits

Bit	Name	Reset	RW	Description
2	SRAM_MASTER_CLKGATE	0x0	RW	Enables top-level clock gating in the SRAM block. This bit should be enabled for lowest power operation. EN = 0x1 - Enable Master SRAM Clock Gate DIS = 0x0 - Disables Master SRAM Clock Gating
1	SRAM_CLKGATE	0x0	RW	Enables individual per-RAM clock gating in the SRAM block. This bit should be enabled for lowest power operation. EN = 0x1 - Enable Individual SRAM Clock Gating DIS = 0x0 - Disables Individual SRAM Clock Gating
0	SRAM_LIGHT_SLEEP	0x1	RW	Enable LS (light sleep) of cache RAMs. When this bit is set, the RAMS will be put into light sleep mode while inactive. NOTE: if the SRAM is actively used, this may have an adverse affect on power since entering/exiting LS mode may consume more power than would be saved. EN = 0x1 - Enable LIGHT SLEEP for SRAMs DIS = 0x0 - Disables LIGHT SLEEP for SRAMs

3.5.3.1.2.8ADCSTATUS Register

Power Status Register for ADC Block

OFFSET: 0x0000001C

INSTANCE 0 ADDRESS: 0x4002101C

Power Status Register for ADC Block

Table 21: ADCSTATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										ADC_REFBUF_PWD	ADC_REFKEEP_PWD	ADC_VBAT_PWD	ADC_VPTAT_PWD	ADC_BGT_PWD	ADC_PWD

Table 22: ADCSTATUS Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED.
5	ADC_REFBUF_PWD	0x0	RO	This bit indicates that the ADC REFBUF is powered down
4	ADC_REFKEEP_PWD	0x0	RO	This bit indicates that the ADC REFKEEP is powered down

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 22: ADCSTATUS Register Bits

Bit	Name	Reset	RW	Description
3	ADC_VBAT_PWD	0x0	RO	This bit indicates that the ADC VBAT resistor divider is powered down
2	ADC_VPTAT_PWD	0x0	RO	This bit indicates that the ADC temperature sensor input buffer is powered down
1	ADC_BGT_PWD	0x0	RO	This bit indicates that the ADC Band Gap is powered down
0	ADC_PWD	0x0	RO	This bit indicates that the ADC is powered down

3.5.3.1.2.9MISCOPT Register

Power Optimization Control Bits

OFFSET: 0x00000020

INSTANCE 0 ADDRESS: 0x40021020

Power Optimization Control Bits

Table 23: MISCOPT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													DIS_LDOLPMODE_TIMERS	DIS_LDOLPMODE_HFRC	ADC_EN_MASK

Table 24: MISCOPT Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	RESERVED.
2	DIS_LDOLPMODE_TIMERS	0x0	RW	Setting this bit will enable the MEM LDO to be in LPMODE during deep sleep even when the ctimers or stimers are running
1	DIS_LDOLPMODE_HFRC	0x0	RW	Setting this bit will enable the Core LDO to be in LPMODE during deep sleep even when HFRC is enabled.
0	ADC_EN_MASK	0x0	RW	Control Bit to mask the ADC_EN in the adc_pwr_down equation.

©2017 Ambiq Micro, Inc.
All rights reserved.

3.6 Debug Interfaces

A number of useful debug facilities are provided in the Apollo2 Blue.

3.6.1 Debugger Attachment

An external debugger can be connected to the MCU using ARM's Serial Wire Debug (SWD) interface. The SWD interface is a 2-wire interface that is supported by a variety of off-the-shelf commercial debuggers, enabling customers to utilize their development environment of choice.

3.6.2 Instrumentation Trace Macrocell (ITM)

For system trace the processor integrates an *Instrumentation Trace Macrocell* (ITM) alongside data watchpoints and a profiling unit. To enable simple and cost-effective profiling of the system events these generate, a *Serial Wire Viewer* (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin.

3.6.3 Trace Port Interface Unit (TPIU)

The Apollo2 Blue includes a Cortex-M4 Trace Port Interface Unit (TPIU). The Cortex-M4 TPIU is an ARM IP component that acts as a bridge between the on-chip trace data from the ITM and the single pin supporting the Serial Wire Viewer Protocol.

The TPIU includes a Trace Output Serializer that can format and send the SWV protocol in either a Manchester encoded form or as a standard UART stream.

3.6.4 Faulting Address Trapping Hardware

The Apollo2 Blue offers an optional facility for trapping the address associated with bus faults occurring on any of the three AMBA AHB buses on the chip. This facility must be specifically enabled so that energy is not wasted when one is not actively debugging.

3.7 ITM Registers

ARM ITM Registers.

INSTANCE 0 BASE ADDRESS:0x00000000

©2017 Ambiq Micro, Inc.
All rights reserved.

3.7.1 Register Memory Map

Table 25: ITM Register Map

Address(s)	Register Name	Description
0xE0000000	STIM0	Stimulus Port Register 0
0xE0000004	STIM1	Stimulus Port Register 1
0xE0000008	STIM2	Stimulus Port Register 2
0xE000000C	STIM3	Stimulus Port Register 3
0xE0000010	STIM4	Stimulus Port Register 4
0xE0000014	STIM5	Stimulus Port Register 5
0xE0000018	STIM6	Stimulus Port Register 6
0xE000001C	STIM7	Stimulus Port Register 7
0xE0000020	STIM8	Stimulus Port Register 8
0xE0000024	STIM9	Stimulus Port Register 9
0xE0000028	STIM10	Stimulus Port Register 10
0xE000002C	STIM11	Stimulus Port Register 11
0xE0000030	STIM12	Stimulus Port Register 12
0xE0000034	STIM13	Stimulus Port Register 13
0xE0000038	STIM14	Stimulus Port Register 14
0xE000003C	STIM15	Stimulus Port Register 15
0xE0000040	STIM16	Stimulus Port Register 16
0xE0000044	STIM17	Stimulus Port Register 17
0xE0000048	STIM18	Stimulus Port Register 18
0xE000004C	STIM19	Stimulus Port Register 19
0xE0000050	STIM20	Stimulus Port Register 20
0xE0000054	STIM21	Stimulus Port Register 21
0xE0000058	STIM22	Stimulus Port Register 22
0xE000005C	STIM23	Stimulus Port Register 23
0xE0000060	STIM24	Stimulus Port Register 24
0xE0000064	STIM25	Stimulus Port Register 25
0xE0000068	STIM26	Stimulus Port Register 26
0xE000006C	STIM27	Stimulus Port Register 27
0xE0000070	STIM28	Stimulus Port Register 28
0xE0000074	STIM29	Stimulus Port Register 29
0xE0000078	STIM30	Stimulus Port Register 30
0xE000007C	STIM31	Stimulus Port Register 31
0xE0000E00	TER	Trace Enable Register.
0xE0000E40	TPR	Trace Privilege Register.
0xE0000E80	TCR	Trace Control Register.
0xE0000FB0	LOCKAREG	Lock Access Register

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 25: ITM Register Map

Address(s)	Register Name	Description
0xE0000FB4	LOCKSREG	Lock Status Register
0xE0000FD0	PID4	Peripheral Identification Register 4
0xE0000FD4	PID5	Peripheral Identification Register 5
0xE0000FD8	PID6	Peripheral Identification Register 6
0xE0000FDC	PID7	Peripheral Identification Register 7
0xE0000FE0	PID0	Peripheral Identification Register 0
0xE0000FE4	PID1	Peripheral Identification Register 1
0xE0000FE8	PID2	Peripheral Identification Register 2
0xE0000FEC	PID3	Peripheral Identification Register 3
0xE0000FF0	CID0	Component Identification Register 1
0xE0000FF4	CID1	Component Identification Register 1
0xE0000FF8	CID2	Component Identification Register 2
0xE0000FFC	CID3	Component Identification Register 3

©2017 Ambiq Micro, Inc.
All rights reserved.

3.7.2 ITM Registers

3.7.2.1 STIM0 Register

Stimulus Port Register 0

OFFSET: 0xE0000000

INSTANCE 0 ADDRESS: 0xE0000000

Stimulus Port Register 0

Table 26: STIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM0																															

Table 27: STIM0 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM0	0x0	RW	Stimulus Port Register 0.

3.7.2.2 STIM1 Register

Stimulus Port Register 1

OFFSET: 0xE0000004

INSTANCE 0 ADDRESS: 0xE0000004

Stimulus Port Register 1

Table 28: STIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM1																															

Table 29: STIM1 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM1	0x0	RW	Stimulus Port Register 1.

©2017 Ambiq Micro, Inc.
All rights reserved.

3.7.2.3 STIM2 Register

Stimulus Port Register 2

OFFSET: 0xE0000008

INSTANCE 0 ADDRESS: 0xE0000008

Stimulus Port Register 2

Table 30: STIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM2																															

Table 31: STIM2 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM2	0x0	RW	Stimulus Port Register 2.

3.7.2.4 STIM3 Register

Stimulus Port Register 3

OFFSET: 0xE000000C

INSTANCE 0 ADDRESS: 0xE000000C

Stimulus Port Register 3

Table 32: STIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM3																															

Table 33: STIM3 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM3	0x0	RW	Stimulus Port Register 3.

3.7.2.5 STIM4 Register

Stimulus Port Register 4

OFFSET: 0xE0000010

INSTANCE 0 ADDRESS: 0xE0000010

©2017 Ambiq Micro, Inc.
All rights reserved.

Stimulus Port Register 4

Table 34: STIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM4																															

Table 35: STIM4 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM4	0x0	RW	Stimulus Port Register 4.

3.7.2.6 STIM5 Register

Stimulus Port Register 5

OFFSET: 0xE0000014

INSTANCE 0 ADDRESS: 0xE0000014

Stimulus Port Register 5

Table 36: STIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM5																															

Table 37: STIM5 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM5	0x0	RW	Stimulus Port Register 5.

3.7.2.7 STIM6 Register

Stimulus Port Register 6

OFFSET: 0xE0000018

INSTANCE 0 ADDRESS: 0xE0000018

Stimulus Port Register 6

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 38: STIM6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM6																															

Table 39: STIM6 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM6	0x0	RW	Stimulus Port Register 6.

3.7.2.8 STIM7 Register

Stimulus Port Register 7

OFFSET: 0xE000001C

INSTANCE 0 ADDRESS: 0xE000001C

Stimulus Port Register 7

Table 40: STIM7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM7																															

Table 41: STIM7 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM7	0x0	RW	Stimulus Port Register 7.

3.7.2.9 STIM8 Register

Stimulus Port Register 8

OFFSET: 0xE0000020

INSTANCE 0 ADDRESS: 0xE0000020

Stimulus Port Register 8

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 42: STIM8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM8																															

Table 43: STIM8 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM8	0x0	RW	Stimulus Port Register 8.

3.7.2.10 STIM9 Register

Stimulus Port Register 9

OFFSET: 0xE0000024

INSTANCE 0 ADDRESS: 0xE0000024

Stimulus Port Register 9

Table 44: STIM9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM9																															

Table 45: STIM9 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM9	0x0	RW	Stimulus Port Register 9.

3.7.2.11 STIM10 Register

Stimulus Port Register 10

OFFSET: 0xE0000028

INSTANCE 0 ADDRESS: 0xE0000028

Stimulus Port Register 10

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 46: STIM10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM10																															

Table 47: STIM10 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM10	0x0	RW	Stimulus Port Register 10.

3.7.2.12 STIM11 Register

Stimulus Port Register 11

OFFSET: 0xE000002C

INSTANCE 0 ADDRESS: 0xE000002C

Stimulus Port Register 11

Table 48: STIM11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM11																															

Table 49: STIM11 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM11	0x0	RW	Stimulus Port Register 11.

3.7.2.13 STIM12 Register

Stimulus Port Register 12

OFFSET: 0xE0000030

INSTANCE 0 ADDRESS: 0xE0000030

Stimulus Port Register 12

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 50: STIM12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM12																															

Table 51: STIM12 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM12	0x0	RW	Stimulus Port Register 12.

3.7.2.14 STIM13 Register

Stimulus Port Register 13

OFFSET: 0xE0000034

INSTANCE 0 ADDRESS: 0xE0000034

Stimulus Port Register 13

Table 52: STIM13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM13																															

Table 53: STIM13 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM13	0x0	RW	Stimulus Port Register 13.

3.7.2.15 STIM14 Register

Stimulus Port Register 14

OFFSET: 0xE0000038

INSTANCE 0 ADDRESS: 0xE0000038

Stimulus Port Register 14

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 54: STIM14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM14																															

Table 55: STIM14 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM14	0x0	RW	Stimulus Port Register 14.

3.7.2.16 STIM15 Register

Stimulus Port Register 15

OFFSET: 0xE000003C

INSTANCE 0 ADDRESS: 0xE000003C

Stimulus Port Register 15

Table 56: STIM15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM15																															

Table 57: STIM15 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM15	0x0	RW	Stimulus Port Register 15.

3.7.2.17 STIM16 Register

Stimulus Port Register 16

OFFSET: 0xE0000040

INSTANCE 0 ADDRESS: 0xE0000040

Stimulus Port Register 16

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 58: STIM16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM16																															

Table 59: STIM16 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM16	0x0	RW	Stimulus Port Register 16.

3.7.2.18 STIM17 Register

Stimulus Port Register 17

OFFSET: 0xE0000044

INSTANCE 0 ADDRESS: 0xE0000044

Stimulus Port Register 17

Table 60: STIM17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM17																															

Table 61: STIM17 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM17	0x0	RW	Stimulus Port Register 17.

3.7.2.19 STIM18 Register

Stimulus Port Register 18

OFFSET: 0xE0000048

INSTANCE 0 ADDRESS: 0xE0000048

Stimulus Port Register 18

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 62: STIM18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM18																															

Table 63: STIM18 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM18	0x0	RW	Stimulus Port Register 18.

3.7.2.20 STIM19 Register

Stimulus Port Register 19

OFFSET: 0xE000004C

INSTANCE 0 ADDRESS: 0xE000004C

Stimulus Port Register 19

Table 64: STIM19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM19																															

Table 65: STIM19 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM19	0x0	RW	Stimulus Port Register 19.

3.7.2.21 STIM20 Register

Stimulus Port Register 20

OFFSET: 0xE0000050

INSTANCE 0 ADDRESS: 0xE0000050

Stimulus Port Register 20

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 66: STIM20 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM20																															

Table 67: STIM20 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM20	0x0	RW	Stimulus Port Register 20.

3.7.2.22 STIM21 Register

Stimulus Port Register 21

OFFSET: 0xE0000054

INSTANCE 0 ADDRESS: 0xE0000054

Stimulus Port Register 21

Table 68: STIM21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM21																															

Table 69: STIM21 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM21	0x0	RW	Stimulus Port Register 21.

3.7.2.23 STIM22 Register

Stimulus Port Register 22

OFFSET: 0xE0000058

INSTANCE 0 ADDRESS: 0xE0000058

Stimulus Port Register 22

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 70: STIM22 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM22																															

Table 71: STIM22 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM22	0x0	RW	Stimulus Port Register 22.

3.7.2.24 STIM23 Register

Stimulus Port Register 23

OFFSET: 0xE000005C

INSTANCE 0 ADDRESS: 0xE000005C

Stimulus Port Register 23

Table 72: STIM23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM23																															

Table 73: STIM23 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM23	0x0	RW	Stimulus Port Register 23.

3.7.2.25 STIM24 Register

Stimulus Port Register 24

OFFSET: 0xE0000060

INSTANCE 0 ADDRESS: 0xE0000060

Stimulus Port Register 24

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 74: STIM24 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM24																															

Table 75: STIM24 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM24	0x0	RW	Stimulus Port Register 24.

3.7.2.26 STIM25 Register

Stimulus Port Register 25

OFFSET: 0xE0000064

INSTANCE 0 ADDRESS: 0xE0000064

Stimulus Port Register 25

Table 76: STIM25 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM25																															

Table 77: STIM25 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM25	0x0	RW	Stimulus Port Register 25.

3.7.2.27 STIM26 Register

Stimulus Port Register 26

OFFSET: 0xE0000068

INSTANCE 0 ADDRESS: 0xE0000068

Stimulus Port Register 26

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 78: STIM26 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM26																															

Table 79: STIM26 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM26	0x0	RW	Stimulus Port Register 26.

3.7.2.28 STIM27 Register

Stimulus Port Register 27

OFFSET: 0xE000006C

INSTANCE 0 ADDRESS: 0xE000006C

Stimulus Port Register 27

Table 80: STIM27 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM27																															

Table 81: STIM27 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM27	0x0	RW	Stimulus Port Register 27.

3.7.2.29 STIM28 Register

Stimulus Port Register 28

OFFSET: 0xE0000070

INSTANCE 0 ADDRESS: 0xE0000070

Stimulus Port Register 28

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 82: STIM28 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM28																															

Table 83: STIM28 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM28	0x0	RW	Stimulus Port Register 28.

3.7.2.30 STIM29 Register

Stimulus Port Register 29

OFFSET: 0xE0000074

INSTANCE 0 ADDRESS: 0xE0000074

Stimulus Port Register 29

Table 84: STIM29 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM29																															

Table 85: STIM29 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM29	0x0	RW	Stimulus Port Register 29.

3.7.2.31 STIM30 Register

Stimulus Port Register 30

OFFSET: 0xE0000078

INSTANCE 0 ADDRESS: 0xE0000078

Stimulus Port Register 30

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 86: STIM30 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM30																															

Table 87: STIM30 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM30	0x0	RW	Stimulus Port Register 30.

3.7.2.32 STIM31 Register

Stimulus Port Register 31

OFFSET: 0xE000007C

INSTANCE 0 ADDRESS: 0xE000007C

Stimulus Port Register 31

Table 88: STIM31 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIM31																															

Table 89: STIM31 Register Bits

Bit	Name	Reset	RW	Description
31:0	STIM31	0x0	RW	Stimulus Port Register 31.

3.7.2.33 TER Register

Trace Enable Register.

OFFSET: 0xE0000E00

INSTANCE 0 ADDRESS: 0xE0000E00

Trace Enable Register.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 90: TER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STIMENA																															

Table 91: TER Register Bits

Bit	Name	Reset	RW	Description
31:0	STIMENA	0x0	RW	Bit mask to enable tracing on ITM stimulus ports. One bit per stimulus port..

3.7.2.34 TPR Register

Trace Privilege Register.

OFFSET: 0xE0000E40

INSTANCE 0 ADDRESS: 0xE0000E40

Trace Privilege Register.

Table 92: TPR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												PRIVMASK			

Table 93: TPR Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED.
3:0	PRIVMASK	0x0	RW	Bit mask to enable tracing on ITM stimulus ports. bit[0] = stimulus ports[7:0], bit[1] = stimulus ports[15:8], bit[2] = stimulus ports[23:16], bit[3] = stimulus ports[31:24].

3.7.2.35 TCR Register

Trace Control Register.

OFFSET: 0xE0000E80

INSTANCE 0 ADDRESS: 0xE0000E80

©2017 Ambiq Micro, Inc.
All rights reserved.

Trace Control Register.

Table 94: TCR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD								BUSY	ATB_ID							RSVD				TS_FREQ		TS_PRESCALE		RSVD			SWV_ENABLE	DWT_ENABLE	SYNC_ENABLE	TS_ENABLE	ITM_ENABLE

Table 95: TCR Register Bits

Bit	Name	Reset	RW	Description
31:24	RSVD	0x0	RO	RESERVED.
23	BUSY	0x0	RW	Set when ITM events present and being drained.
22:16	ATB_ID	0x0	RW	ATB ID for CoreSight system.
15:12	RSVD	0x0	RO	RESERVED.
11:10	TS_FREQ	0x0	RW	Global Timestamp Frequency.
9:8	TS_PRESCALE	0x0	RW	Timestamp prescaler: 0b00 = no prescaling 0b01 = divide by 4 0b10 = divide by 16 0b11 = divide by 64.
7:5	RSVD	0x0	RO	RESERVED.
4	SWV_ENABLE	0x0	RW	Enable SWV behavior â€“ count on TPIUEMIT and TPIUBAUD.
3	DWT_ENABLE	0x0	RW	Enables the DWT stimulus.
2	SYNC_ENABLE	0x0	RW	Enables sync packets for TPIU.
1	TS_ENABLE	0x0	RW	Enables differential timestamps. Differential timestamps are emitted when a packet is written to the FIFO with a non-zero timestamp counter, and when the timestamp counter overflows. Timestamps are emitted during idle times after a fixed number of cycles. This provides a time reference for packets and inter-packet gaps.
0	ITM_ENABLE	0x0	RW	Enable ITM. This is the master enable, and must be set before ITM Stimulus and Trace Enable registers can be written.

©2017 Ambiq Micro, Inc.
All rights reserved.

3.7.2.36 LOCKAREG Register

Lock Access Register

OFFSET: 0xE0000FB0

INSTANCE 0 ADDRESS: 0xE0000FB0

Lock Access Register

Table 96: LOCKAREG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LOCKAREG																															

Table 97: LOCKAREG Register Bits

Bit	Name	Reset	RW	Description
31:0	LOCKAREG	0x0	RW	Key register value. Key = 0xC5ACCE55 - Key

3.7.2.37 LOCKSREG Register

Lock Status Register

OFFSET: 0xE0000FB4

INSTANCE 0 ADDRESS: 0xE0000FB4

Lock Status Register

Table 98: LOCKSREG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													BYTEACC	ACCESS	PRESENT

Table 99: LOCKSREG Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	RESERVED.
2	BYTEACC	0x0	RO	You cannot implement 8-bit lock accesses.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 99: LOCKSREG Register Bits

Bit	Name	Reset	RW	Description
1	ACCESS	0x0	RO	Write access to component is blocked. All writes are ignored, reads are permitted.
0	PRESENT	0x1	RO	Indicates that a lock mechanism exists for this component.

3.7.2.38 PID4 Register

Peripheral Identification Register 4

OFFSET: 0xE0000FD0

INSTANCE 0 ADDRESS: 0xE0000FD0

Peripheral Identification Register 4

Table 100: PID4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PID4																															

Table 101: PID4 Register Bits

Bit	Name	Reset	RW	Description
31:0	PID4	0x4	R0	Peripheral Identification 4.

3.7.2.39 PID5 Register

Peripheral Identification Register 5

OFFSET: 0xE0000FD4

INSTANCE 0 ADDRESS: 0xE0000FD4

Peripheral Identification Register 5

Table 102: PID5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PID5																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 103: PID5 Register Bits

Bit	Name	Reset	RW	Description
31:0	PID5	0x0	R0	Peripheral Identification 5.

3.7.2.40 PID6 Register

Peripheral Identification Register 6

OFFSET: 0xE0000FD8

INSTANCE 0 ADDRESS: 0xE0000FD8

Peripheral Identification Register 6

Table 104: PID6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PID6																															

Table 105: PID6 Register Bits

Bit	Name	Reset	RW	Description
31:0	PID6	0x0	R0	Peripheral Identification 6.

3.7.2.41 PID7 Register

Peripheral Identification Register 7

OFFSET: 0xE0000FDC

INSTANCE 0 ADDRESS: 0xE0000FDC

Peripheral Identification Register 7

Table 106: PID7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PID7																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 107: PID7 Register Bits

Bit	Name	Reset	RW	Description
31:0	PID7	0x0	R0	Peripheral Identification 7.

3.7.2.42 PID0 Register

Peripheral Identification Register 0

OFFSET: 0xE0000FE0

INSTANCE 0 ADDRESS: 0xE0000FE0

Peripheral Identification Register 0

Table 108: PID0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PID0																															

Table 109: PID0 Register Bits

Bit	Name	Reset	RW	Description
31:0	PID0	0x1	R0	Peripheral Identification 0.

3.7.2.43 PID1 Register

Peripheral Identification Register 1

OFFSET: 0xE0000FE4

INSTANCE 0 ADDRESS: 0xE0000FE4

Peripheral Identification Register 1

Table 110: PID1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PID1																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 111: PID1 Register Bits

Bit	Name	Reset	RW	Description
31:0	PID1	0xb0	R0	Peripheral Identification 1.

3.7.2.44 PID2 Register

Peripheral Identification Register 2

OFFSET: 0xE0000FE8

INSTANCE 0 ADDRESS: 0xE0000FE8

Peripheral Identification Register 2

Table 112: PID2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PID2																															

Table 113: PID2 Register Bits

Bit	Name	Reset	RW	Description
31:0	PID2	0x3b	R0	Peripheral Identification 2.

3.7.2.45 PID3 Register

Peripheral Identification Register 3

OFFSET: 0xE0000FEC

INSTANCE 0 ADDRESS: 0xE0000FEC

Peripheral Identification Register 3

Table 114: PID3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PID3																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 115: PID3 Register Bits

Bit	Name	Reset	RW	Description
31:0	PID3	0x0	R0	Peripheral Identification 3.

3.7.2.46 CID0 Register

Component Identification Register 1

OFFSET: 0xE0000FF0

INSTANCE 0 ADDRESS: 0xE0000FF0

Component Identification Register 1

Table 116: CID0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CID0																															

Table 117: CID0 Register Bits

Bit	Name	Reset	RW	Description
31:0	CID0	0xd	R0	Component Identification 1.

3.7.2.47 CID1 Register

Component Identification Register 1

OFFSET: 0xE0000FF4

INSTANCE 0 ADDRESS: 0xE0000FF4

Component Identification Register 1

Table 118: CID1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CID1																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 119: CID1 Register Bits

Bit	Name	Reset	RW	Description
31:0	CID1	0xe0	R0	Component Identification 1.

3.7.2.48 CID2 Register

Component Identification Register 2

OFFSET: 0xE0000FF8

INSTANCE 0 ADDRESS: 0xE0000FF8

Component Identification Register 2

Table 120: CID2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CID2																															

Table 121: CID2 Register Bits

Bit	Name	Reset	RW	Description
31:0	CID2	0x5	R0	Component Identification 2.

3.7.2.49 CID3 Register

Component Identification Register 3

OFFSET: 0xE0000FFC

INSTANCE 0 ADDRESS: 0xE0000FFC

Component Identification Register 3

Table 122: CID3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CID3																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 123: CID3 Register Bits

Bit	Name	Reset	RW	Description
31:0	CID3	0xb1	R0	Component Identification 3.

3.8 MCUCTRL Registers

MCU Miscellaneous Control Logic

INSTANCE 0 BASE ADDRESS:0x40020000

©2017 Ambiq Micro, Inc.
All rights reserved.

3.8.1 Register Memory Map

Table 124: MCUCTRL Register Map

Address(s)	Register Name	Description
0x40020000	CHIP_INFO	Chip Information Register
0x40020004	CHIPID0	Unique Chip ID 0
0x40020008	CHIPID1	Unique Chip ID 1
0x4002000C	CHIPREV	Chip Revision
0x40020010	VENDORID	Unique Vendor ID
0x40020014	DEBUGGER	Debugger Access Control
0x40020060	BUCK	Analog Buck Control
0x40020064	BUCK2	Buck Control Reg2
0x40020068	BUCK3	Buck control reg 3
0x40020084	LDOREG2	LDO Control Register 2
0x40020100	BODPORCTRL	BOD and PDR control Register
0x4002010C	ADCCAL	ADC Calibration Control
0x40020110	ADCBATTLOAD	ADC Battery Load Enable
0x4002011C	ADCREFCOMP	ADC Reference Keeper and Comparator Control
0x40020124	XTALGENCTRL	XTAL Oscillator General Control
0x400201A0	BOOTLOADERLOW	Determines whether the bootloader code is visible at address 0x00000000
0x400201A4	SHADOWVALID	Register to indicate whether the shadow registers have been successfully loaded from the Flash Information Space.
0x400201C0	ICODEFAULTADDR	ICODE bus address which was present when a bus fault occurred.
0x400201C4	DCODEFAULTADDR	DCODE bus address which was present when a bus fault occurred.
0x400201C8	SYSFAULTADDR	System bus address which was present when a bus fault occurred.
0x400201CC	FAULTSTATUS	Reflects the status of the bus decoders' fault detection. Any write to this register will clear all of the status bits within the register.
0x400201D0	FAULTCAPTUREEN	Enable the fault capture registers
0x40020200	DBGR1	Read-only debug register 1
0x40020204	DBGR2	Read-only debug register 2
0x40020220	PMUENABLE	Control bit to enable/disable the PMU
0x40020250	TPIUCTRL	TPIU Control Register. Determines the clock enable and frequency for the M4's TPIU interface.

©2017 Ambiq Micro, Inc.
All rights reserved.

3.8.2 MCUCTRL Registers

3.8.2.1 CHIP_INFO Register

Chip Information Register

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x40020000

Chip Information Register

Table 125: CHIP_INFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PARTNUM																															

Table 126: CHIP_INFO Register Bits

Bit	Name	Reset	RW	Description
31:0	PARTNUM	0x3000000	RO	BCD part number. PARTNUM= 0x3000000 - Apollo2 part number is 0x03XXXXXX.

3.8.2.2 CHIPID0 Register

Unique Chip ID 0

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x40020004

Unique Chip ID 0

Table 127: CHIPID0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 128: CHIPID0 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RO	Unique chip ID 0. VALUE = Upper 32-bits of a 64-bit encoded unique chip ID

©2017 Ambiq Micro, Inc.
All rights reserved.

3.8.2.3 CHIPID1 Register

Unique Chip ID 1

OFFSET: 0x00000008

INSTANCE 0 ADDRESS: 0x40020008

Unique Chip ID 1

Table 129: CHIPID1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 130: CHIPID1 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RO	Unique chip ID 1. VALUE = Lower 32-bits of a 64-bit encoded unique chip ID

3.8.2.4 CHIPREV Register

Chip Revision

OFFSET: 0x0000000C

INSTANCE 0 ADDRESS: 0x4002000C

Chip Revision

Table 131: CHIPREV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								REVMAJ				REVMIN			

Table 132: CHIPREV Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	RESERVED.
7:4	REVMAJ	0x2	RO	Major Revision ID. B = 0x2 - Apollo2 revision B A = 0x1 - Apollo2 revision A

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 132: CHIPREV Register Bits

Bit	Name	Reset	RW	Description
3:0	REVMIN	0x2	RO	Minor Revision ID. REV2 = 0x2 - Apollo2 minor revision 2 REV0 = 0x0 - Apollo2 minor revision 0

3.8.2.5 VENDORID Register

Unique Vendor ID

OFFSET: 0x00000010

INSTANCE 0 ADDRESS: 0x40020010

Unique Vendor ID

Table 133: VENDORID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 134: VENDORID Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RO	Unique Vendor ID AMBIQ = 0x414D4251 - Ambiq Vendor ID

3.8.2.6 DEBUGGER Register

Debugger Access Control

OFFSET: 0x00000014

INSTANCE 0 ADDRESS: 0x40020014

Debugger Access Control

Table 135: DEBUGGER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															LOCKOUT

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 136: DEBUGGER Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED
0	LOCKOUT	0x0	RW	Lockout of debugger (SWD).

3.8.2.7 BUCK Register

Analog Buck Control

OFFSET: 0x00000060

INSTANCE 0 ADDRESS: 0x40020060

Analog Buck Control

Table 137: BUCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								MEMBUCKRST	CORE-BUCKRST	BYPBUCKMEM	MEMBUCKPWD	SLEEPBUCK-	CORE-BUCKPWD	BYPBUCKCORE	BUCKSWE

Table 138: BUCK Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	RESERVED.
7	MEMBUCKRST	0x0	RW	Reset control override for Mem Buck; 0=enabled, 1=reset; Value is propagated only when the BUCKSWE bit is active, otherwise contrl is from the power control module.
6	CORE-BUCKRST	0x0	RW	Reset control override for Core Buck; 0=enabled, 1=reset; Value is propagated only when the BUCKSWE bit is active, otherwise control is from the power control module.
5	BYPBUCKMEM	0x0	RW	Not used. Additional control of buck is available in the power control module
4	MEMBUCKPWD	0x0	RW	Memory buck power down override. 1=Powered Down; 0=Enabled; Value is propagated only when the BUCKSWE bit is active, otherwise control is from the power control module. EN = 0x0 - Memory Buck Enable.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 138: BUCK Register Bits

Bit	Name	Reset	RW	Description
3	SLEEPBUCK-ANA	0x0	RW	HFRC clkgen bit 0 override. When set, this will override to 0 bit 0 of the hfrc_freq_clkgen internal bus (see internal Shelby-1473)
2	COREBUCK-PWD	0x0	RW	Core buck power down override. 1=Powered Down; 0=Enabled; Value is propagated only when the BUCKSWE bit is active, otherwise control is from the power control module. EN = 0x0 - Core Buck enable.
1	BYPBUCK-CORE	0x0	RW	Not used. Additional control of buck is available in the power control module
0	BUCKSWE	0x0	RW	Buck Register Software Override Enable. This will enable the override values for MEMBUCKPWD, COREBUCKPWD, COREBUCKRST, MEMBUCKRST, all to be propagated to the control logic, instead of the normal power control module signal. Note - Must take care to have correct value for ALL the register bits when this SWE is enabled. OVERRIDE_DIS = 0x0 - BUCK Software Override Disable. OVERRIDE_EN = 0x1 - BUCK Software Override Enable.

3.8.2.8 BUCK2 Register

Buck Control Reg2

OFFSET: 0x00000064

INSTANCE 0 ADDRESS: 0x40020064

Buck Control Reg2

Table 139: BUCK2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																				RSVD		HYSTBUCKCORE	HYSTBUCKMEM	RSVD				RSVD			

Table 140: BUCK2 Register Bits

Bit	Name	Reset	RW	Description
31:12	RSVD	0x0	RO	RESERVED.
11:10	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 140: BUCK2 Register Bits

Bit	Name	Reset	RW	Description
9	HYSTBUCK-CORE	0x0	RW	Enable/disable hysteresis on core buck converters internal comparators. DIS = 0x0 - Disable hysteresis on core buck converters internal comparators. EN = 0x1 - Enable hysteresis on core buck converters internal comparators.
8	HYSTBUCK-MEM	0x0	RW	Enable/disable hysteresis on memory buck converters internal comparators. DIS = 0x0 - Disable hysteresis on memory buck converters internal comparators. EN = 0x1 - Enable hysteresis on memory buck converters internal comparators.
7:4	RSVD	0x0	RW	RESERVED
3:0	RSVD	0x0	RW	RESERVED

3.8.2.9 BUCK3 Register

Buck control reg 3

OFFSET: 0x00000068

INSTANCE 0 ADDRESS: 0x40020068

Buck control reg 3

Table 141: BUCK3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD										RSVD				MEMBUCKBURSTEN	RSVD				RSVD		RSVD				COREBUCKBURSTEN	COREBUCKZXTRIM					RSVD	

Table 142: BUCK3 Register Bits

Bit	Name	Reset	RW	Description
31:22	RSVD	0x0	RO	RESERVED.
21:18	RSVD	0x0	RW	RESERVED
17	MEMBUCK-BURSTEN	0x0	RW	MEM Buck burst enable 0=disable, 0=disabled, 1=enable.
16:13	RSVD	0x0	RW	RESERVED
12:11	RSVD	0x0	RW	RESERVED
10:7	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 142: BUCK3 Register Bits

Bit	Name	Reset	RW	Description
6	COREBUCK-BURSTEN	0x0	RW	Core Buck burst enable. 0=disabled, 1=enabled
5:2	COREBUCKZX-TRIM	0x0	RW	Core buck zero crossing trim value
1:0	RSVD	0x0	RW	RESERVED

3.8.2.10 LDOREG2 Register

LDO Control Register 2

OFFSET: 0x00000084

INSTANCE 0 ADDRESS: 0x40020084

LDO Control Register 2

Table 143: LDOREG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD									CORELDOVDDLEN	RAMLDOLPMODE	PWDRAMLDO	PWDANALDO	PWDMEMLDO	PWDCORELDO	SLEEPANALDO	SLEEPMEMLDO	SLEEPCORELDO	VREFSELANALDO	VREFSELSRAMLDO	VREFSELFLASHLDO	VREFSELCORELDO	RSVD				RSVD						LDO2SWE

Table 144: LDOREG2 Register Bits

Bit	Name	Reset	RW	Description
31:23	RSVD	0x0	RW	Reserved
22	CORELDOVD-DLEN	0x0	RW	Core LDO output enable. 0=Hi-Z, 1=enable. This value is propagated only when LDO2SWE bit is active(1).
21	RAMLDOLP-MODE	0x0	RW	RAM LDO LP Mode. 0=normal mode, 1=low power mode; This value is propagated only when LDO2SWE bit is active(1). LPMODE = 0x1 - RAM IN LP mode
20	PWDRAMLDO	0x0	RW	RAM LDO Power Down. 0=powered up, 1=powered down ; This value is propagated only when LDO2SWE bit is active(1). PWR_DN = 0x1 - Power down RAM LDO.
19	PWDANALDO	0x0	RW	Analog LDO Power Down. This value is propagated only when LDO2SWE bit is active(1). PWR_DN = 0x1 - Power down Analog LDO.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 144: LDOREG2 Register Bits

Bit	Name	Reset	RW	Description
18	PWDMEMLDO	0x0	RW	MEM LDO Power Down. This value is propagated only when LDO2SWE bit is active(1). PWR_DN = 0x1 - Power down Flash LDO.
17	PWDCORELDO	0x0	RW	CORE LDO Power Down. This value is propagated only when LDO2SWE bit is active(1). PWR_DN = 0x1 - Power down Core LDO.
16	SLEEPANALDO	0x0	RW	Analog LDO Sleep. This value is propagated only when LDO2SWE bit is active(1). SLEEP = 0x1 - Analog LDO sleep.
15	SLEEPMEM-LDO	0x0	RW	FLASH LDO Sleep. This value is propagated only when LDO2SWE bit is active(1). SLEEP = 0x1 - SRAM LDO sleep.
14	SLEEP-CORELDO	0x0	RW	CORE LDO Sleep. This value is propagated only when LDO2SWE bit is active(1). SLEEP = 0x1 - Core LDO sleep.
13	VREFSELA-NALDO	0x0	RW	CONTROL BIT IS NOT USED. PLEASE TREAT AS RESERVED
12	VREFSEL-SRAMLDO	0x0	RW	CONTROL BIT IS NOT USED. PLEASE TREAT AS RESERVED
11	VREF-SELFLASHLDO	0x0	RW	CONTROL BIT IS NOT USED. PLEASE TREAT AS RESERVED
10	VREFSEL-CORELDO	0x0	RW	CONTROL BIT IS NOT USED. PLEASE TREAT AS RESERVED
9:6	RSVD	0x0	RW	RESERVED
5:1	RSVD	0x0	RW	RESERVED
0	LDO2SWE	0x0	RW	LDO2 Software Override Enable. If enabled (=1), this will enable the override values from this register to be used instead of the normal control signals for the following fields: CORELDOVDDLEN, RAMLDOLPMODE, PWDRAMLDO, PWDANALDO, PWDMEMLDO, PWDCORELDO, SLEEP-ANALDO, SLEEPMEMLDO, SLEEPCORELDO. OVERRIDE_DIS = 0x0 - LDO2 Software Override Disable. OVERRIDE_EN = 0x1 - LDO2 Software Override Enable.

3.8.2.11 BODPORCTRL Register

BOD and PDR control Register

OFFSET: 0x00000100

INSTANCE 0 ADDRESS: 0x40020100

BOD and PDR control Register

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 145: BODPORCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												BODEXTREFSEL	PDREXTREFSEL	PWDBOD	PWDPDR

Table 146: BODPORCTRL Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED.
3	BODEXTREF-SEL	0x0	RW	BOD External Reference Select. SELECT = 0x1 - BOD external reference select.
2	PDREXTREF-SEL	0x0	RW	PDR External Reference Select. SELECT = 0x1 - PDR external reference select.
1	PWDBOD	0x0	RW	BOD Power Down. PWR_DN = 0x1 - BOD power down.
0	PWDPDR	0x0	RW	PDR Power Down. PWR_DN = 0x1 - PDR power down

3.8.2.12 ADCCAL Register

ADC Calibration Control

OFFSET: 0x0000010C

INSTANCE 0 ADDRESS: 0x4002010C

ADC Calibration Control

Table 147: ADCCAL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														ADCCALIBRATED	CALONPWRUP

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 148: ADCCAL Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	RESERVED.
1	ADCCALI-BRATED	0x0	RO	Status for ADC Calibration FALSE = 0x0 - ADC is not calibrated TRUE = 0x1 - ADC is calibrated
0	CALONPWRUP	0x1	RW	Run ADC Calibration on initial power up sequence DIS = 0x0 - Disable automatic calibration on initial power up EN = 0x1 - Enable automatic calibration on initial power up

3.8.2.13 ADCBATTLOAD Register

ADC Battery Load Enable

OFFSET: 0x00000110

INSTANCE 0 ADDRESS: 0x40020110

ADC Battery Load Enable

Table 149: ADCBATTLOAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															BATTLOAD

Table 150: ADCBATTLOAD Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED.
0	BATTLOAD	0x0	RW	Enable the ADC battery load resistor DIS = 0x0 - Battery load is disconnected EN = 0x1 - Battery load is enabled

3.8.2.14 ADCREFCOMP Register

ADC Reference Keeper and Comparator Control

OFFSET: 0x0000011C

INSTANCE 0 ADDRESS: 0x4002011C

ADC Reference Keeper and Comparator Control

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 151: ADCREFCOMP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD															ADCRFCMPEN	RSVD			RSVD					RSVD							ADC_REFCOMP_OUT

Table 152: ADCREFCOMP Register Bits

Bit	Name	Reset	RW	Description
31:17	RSVD	0x0	RO	RESERVED
16	ADCRFCMPEN	0x0	RW	ADC Reference comparator power down
15:13	RSVD	0x0	RO	RESERVED
12:8	RSVD	0x0	RW	RESERVED
7:1	RSVD	0x0	RO	RESERVED
0	ADC_REFCOM-P_OUT	0x0	RO	Output of the ADC reference comparator

3.8.2.15 XTALGENCTRL Register

XTAL Oscillator General Control

OFFSET: 0x00000124

INSTANCE 0 ADDRESS: 0x40020124

XTAL Oscillator General Control

Table 153: XTALGENCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																		RSVD						RSVD						ACWARMUP	

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 154: XTALGENCTRL Register Bits

Bit	Name	Reset	RW	Description
31:14	RSVD	0x0	RO	RESERVED.
13:8	RSVD	0x0	RW	RESERVED
7:2	RSVD	0x0	RW	RESERVED
1:0	ACWARMUP	0x0	RW	Auto-calibration delay control 1SEC = 0x0 - Warmup period of 1-2 seconds 2SEC = 0x1 - Warmup period of 2-4 seconds 4SEC = 0x2 - Warmup period of 4-8 seconds 8SEC = 0x3 - Warmup period of 8-16 seconds

3.8.2.16 BOOTLOADERLOW Register

Determines whether the bootloader code is visible at address 0x00000000

OFFSET: 0x000001A0

INSTANCE 0 ADDRESS: 0x400201A0

Determines whether the bootloader code is visible at address 0x00000000

Table 155: BOOTLOADERLOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															VALUE

Table 156: BOOTLOADERLOW Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED.
0	VALUE	0x1	RW	Determines whether the bootloader code is visible at address 0x00000000 or not. ADDR0 = 0x1 - Bootloader code at 0x00000000.

3.8.2.17 SHADOWVALID Register

Register to indicate whether the shadow registers have been successfully loaded from the Flash Information Space.

OFFSET: 0x000001A4

INSTANCE 0 ADDRESS: 0x400201A4

©2017 Ambiq Micro, Inc.
All rights reserved.

Register to indicate whether the shadow registers have been successfully loaded from the Flash Information Space.

Table 157: SHADOWVALID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														BL_DSLEEP	VALID

Table 158: SHADOWVALID Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	RESERVED.
1	BL_DSLEEP	0x1	RO	Indicates whether the bootloader should sleep or deep sleep if no image loaded. DEEPSLEEP = 0x1 - Bootloader will go to deep sleep if no flash image loaded
0	VALID	0x1	RO	Indicates whether the shadow registers contain valid data from the Flash Information Space. VALID = 0x1 - Flash information space contains valid data.

3.8.2.18 ICODEFAULTADDR Register

ICODE bus address which was present when a bus fault occurred.

OFFSET: 0x000001C0

INSTANCE 0 ADDRESS: 0x400201C0

ICODE bus address which was present when a bus fault occurred.

Table 159: ICODEFAULTADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ADDR																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 160: ICODEFAULTADDR Register Bits

Bit	Name	Reset	RW	Description
31:0	ADDR	0x0	RO	The ICODE bus address observed when a Bus Fault occurred. Once an address is captured in this field, it is held until the corresponding Fault Observed bit is cleared in the FAULTSTATUS register.

3.8.2.19 DCODEFAULTADDR Register

DCODE bus address which was present when a bus fault occurred.

OFFSET: 0x000001C4

INSTANCE 0 ADDRESS: 0x400201C4

DCODE bus address which was present when a bus fault occurred.

Table 161: DCODEFAULTADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ADDR																															

Table 162: DCODEFAULTADDR Register Bits

Bit	Name	Reset	RW	Description
31:0	ADDR	0x0	RO	The DCODE bus address observed when a Bus Fault occurred. Once an address is captured in this field, it is held until the corresponding Fault Observed bit is cleared in the FAULTSTATUS register.

3.8.2.20 SYSFAULTADDR Register

System bus address which was present when a bus fault occurred.

OFFSET: 0x000001C8

INSTANCE 0 ADDRESS: 0x400201C8

System bus address which was present when a bus fault occurred.

Table 163: SYSFAULTADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ADDR																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 164: SYSFAULTADDR Register Bits

Bit	Name	Reset	RW	Description
31:0	ADDR	0x0	RO	SYS bus address observed when a Bus Fault occurred. Once an address is captured in this field, it is held until the corresponding Fault Observed bit is cleared in the FAULTSTATUS register.

3.8.2.21 FAULTSTATUS Register

Reflects the status of the bus decoders' fault detection. Any write to this register will clear all of the status bits within the register.

OFFSET: 0x000001CC

INSTANCE 0 ADDRESS: 0x400201CC

Reflects the status of the bus decoders' fault detection. Any write to this register will clear all of the status bits within the register.

Table 165: FAULTSTATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													SYS	DCODE	ICODE

Table 166: FAULTSTATUS Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	RESERVED.
2	SYS	0x0	RW	SYS Bus Decoder Fault Detected bit. When set, a fault has been detected, and the SYSFAULTADDR register will contain the bus address which generated the fault. NOFAULT = 0x0 - No bus fault has been detected. FAULT = 0x1 - Bus fault detected.
1	DCODE	0x0	RW	DCODE Bus Decoder Fault Detected bit. When set, a fault has been detected, and the DCODEFAULTADDR register will contain the bus address which generated the fault. NOFAULT = 0x0 - No DCODE fault has been detected. FAULT = 0x1 - DCODE fault detected.
0	ICODE	0x0	RW	The ICODE Bus Decoder Fault Detected bit. When set, a fault has been detected, and the ICODEFAULTADDR register will contain the bus address which generated the fault. NOFAULT = 0x0 - No ICODE fault has been detected. FAULT = 0x1 - ICODE fault detected.

©2017 Ambiq Micro, Inc.
All rights reserved.

3.8.2.22 FAULTCAPTUREEN Register

Enable the fault capture registers

OFFSET: 0x000001D0

INSTANCE 0 ADDRESS: 0x400201D0

Enable the fault capture registers

Table 167: FAULTCAPTUREEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															ENABLE

Table 168: FAULTCAPTUREEN Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED.
0	ENABLE	0x0	RW	Fault Capture Enable field. When set, the Fault Capture monitors are enabled and addresses which generate a hard fault are captured into the FAULTADDR registers. DIS = 0x0 - Disable fault capture. EN = 0x1 - Enable fault capture.

3.8.2.23 DBGR1 Register

Read-only debug register 1

OFFSET: 0x00000200

INSTANCE 0 ADDRESS: 0x40020200

Read-only debug register 1

Table 169: DBGR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ONETO8																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 170: DBGR1 Register Bits

Bit	Name	Reset	RW	Description
31:0	ONETO8	0x12345678	RO	Read-only register for communication validation

3.8.2.24 DBGR2 Register

Read-only debug register 2

OFFSET: 0x00000204

INSTANCE 0 ADDRESS: 0x40020204

Read-only debug register 2

Table 171: DBGR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
COOLCODE																															

Table 172: DBGR2 Register Bits

Bit	Name	Reset	RW	Description
31:0	COOLCODE	0xc001c0de	RO	Read-only register for communication validation

3.8.2.25 PMUENABLE Register

Control bit to enable/disable the PMU

OFFSET: 0x00000220

INSTANCE 0 ADDRESS: 0x40020220

Control bit to enable/disable the PMU

Table 173: PMUENABLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															ENABLE

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 174: PMUENABLE Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED.
0	ENABLE	0x1	RW	PMU Enable Control bit. When set, the MCU's PMU will place the MCU into the lowest power consuming Deep Sleep mode upon execution of a WFI instruction (dependent on the setting of the SLEEPDEEP bit in the ARM SCR register). When cleared, regardless of the requested sleep mode, the PMU will not enter the lowest power Deep Sleep mode, instead entering the Sleep mode. DIS = 0x0 - Disable MCU power management. EN = 0x1 - Enable MCU power management.

3.8.2.26 TPIUCTRL Register

TPIU Control Register. Determines the clock enable and frequency for the M4's TPIU interface.

OFFSET: 0x00000250

INSTANCE 0 ADDRESS: 0x40020250

TPIU Control Register. Determines the clock enable and frequency for the M4's TPIU interface.

Table 175: TPIUCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					CLKSEL			RSVD							ENABLE

Table 176: TPIUCTRL Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	RESERVED.
10:8	CLKSEL	0x0	RW	This field selects the frequency of the ARM M4 TPIU port. LOW_PWR = 0x0 - Low power state. 0MHz = 0x0 - Low power state. HFRC_DIV_2 = 0x1 - Selects HFRC divided by 2 as the source TPIU clk HFRC_DIV_8 = 0x2 - Selects HFRC divided by 8 as the source TPIU clk HFRC_DIV_16 = 0x3 - Selects HFRC divided by 16 as the source TPIU clk HFRC_DIV_32 = 0x4 - Selects HFRC divided by 32 as the source TPIU clk
7:1	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 176: TPIUCTRL Register Bits

Bit	Name	Reset	RW	Description
0	ENABLE	0x0	RW	TPIU Enable field. When set, the ARM M4 TPIU is enabled and data can be streamed out of the MCU's SWO port using the ARM ITM and TPIU modules. DIS = 0x0 - Disable the TPIU. EN = 0x1 - Enable the TPIU.

3.9 Memory Subsystem

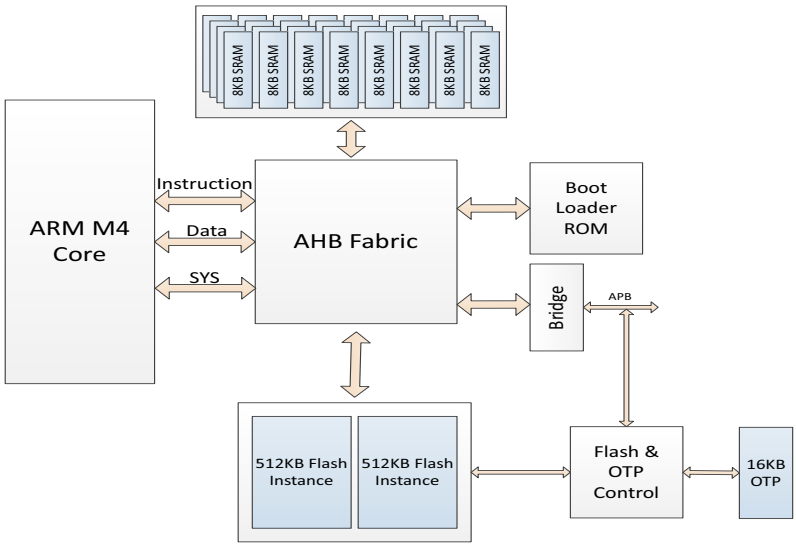


Figure 5. Block Diagram for Flash and OTP Memory Subsystem

3.9.1 Features

The Apollo2 Blue integrates four kinds of memory as shown in Figure 5:

- SRAM
- Flash (with Flash cache)
- Boot Loader ROM
- One Time Programmable (OTP) memory

Key features include:

- 256KB SRAM
- 2 instances of 512 KB flash Memory (1 MB total)

©2017 Ambiq Micro, Inc.
All rights reserved.

- 16 KB Flash cache (2-way set-associative, 512 entry, 128b linesize)
- 16 KBytes OTP
  - 8 KBytes contain factory preset per chip trim values.
  - 8 KBytes for customer use, including flash protection fields
- Flash Protection specified in 16 KB Chunks
  - 64 OTP bits specify Write Protected Chunks
  - 64 OTP bits specify Read Protected Chunks
  - A Chunk is Execute Only if Both Corresponding Protection Bits Specified
  - OTP bits Specify Debugger Lock Out State
  - OTP bits Can Protect SRAM Contents From Debugger Inspection

3.9.2 Functional Overview

The Apollo2 Blue Integrates up to 1024 KBytes of on-board flash memory and 16 Kbytes of one time programmable memory. These two memories are managed by the APB flash controller for write operations.

During normal MCU code execution, the Flash Cache Controller translates requests from the CPU core to the Flash Memory instance for instruction and data fetches. The Controller is designed to return data in zero wait-states when accesses hit into the cache and can operate up to the maximum operating frequency of the CPU core. On cache misses, the controller issues miss requests to the Flash memory controller.

The Flash Memory Controller facilitates flash erase and programming operations. When erase or programming operations are active, instructions cannot be fetched for execution from the Flash memory, so the on-chip SRAM would have to be used for code execution. The cache controller ensures these operations are synchronized. To facilitate the management of flash updates and OTP programming, a number of flash helper functions are provided in the boot loader ROM.

NOTE: To ensure reliable Flash program/read operation, the same bit-cell cannot be programmed to "0" more than once before it is erased. Further, for any given 128-byte address range (0x0 to 0x7f, 0x80 to 0xff, etc.), the total number of programming operations before the entire range is erased cannot exceed 128 programming pulses.

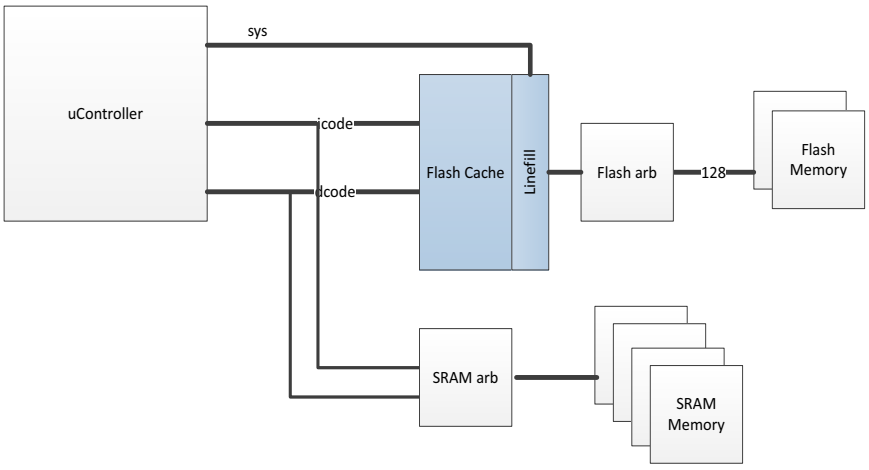
The boot loader ROM contains approximately 2 KB of instructions that are executed upon power up of the processor. Once it is established that the reset vector at offset 0x4 in flash memory is valid (points to a location in flash) and the stack pointer is valid (points into RAM), the boot loader transfers control to the user’s application by loading the SP and PC from the respective values in the vector table and branches to the reset vector in flash. This process is done in less than 100 instructions in the boot loader. The remainder of the boot loader is occupied by a set of flash helper functions.

©2017 Ambiq Micro, Inc.
All rights reserved.

3.9.3 Flash Cache

3.9.3.1 Functional Overview

Figure 6. Block Diagram for Apollo2 with Flash Cache



Apollo2 Blue incorporates a Flash cache to the ICode and DCode path from the microcontroller. This controller is intended to provide single cycle read access to Flash and reduce overall accesses to the Flash to reduce power. The controller is a unified ICode and DCode cache controller. The cache fill path is arbitrated between cache misses as well as the other Flash read agents (Info, Reg, BIST).

The cache is configurable 2-way set associative, 512 entry and 128b linesize.

3.9.3.1.1 Cache Operation

To enable the cache, software should write the CACHECFG register with the desired setting. The ENABLE field in this register will power up the cache SRAMs and initiate the cache startup sequence which will flush the cache RAMs. Once the sequence is complete (indicated by the CACHE_READY bit in the CACHECTRL register), the cache will automatically begin servicing instruction and/or data fetches from the cache depending on the state of the ICACHE_ENABLE and DCACHE_ENABLE values. Software can choose to enable/disable these independently and they can be dynamically changed during operation. Additionally, the non-cachable region registers can be used to mark regions as non-cached, which supercedes the I/D enable bits and causes all fetches from within this range to be non-cached.

The cache will automatically flush data contents if flash is erased/programmed or if the primary cache enable bit is disabled. Additionally, software can invalidate the cache by writing the INVALIDATE bit of the CACHECTRL register. Since this register contains only status information (on reads) and activates controls based on bits set, there is no need to perform a read-modify-write.

For any mode changes, the cache should first be disabled by writing the ENABLE bit to 0, changing the configuration, then re-writing the enable bit to a 1.

3.9.3.1.2 Cache Performance Monitors

The cache also includes logic to monitor cache performance, which should be used in conjunction with the STIMER or CTIMER to determine elapsed time. The instruction and data buses have independent monitoring logic that keep counts of the following conditions:

- ACCESS_COUNT - total number of reads performed on the bus
- LOOKUP_COUNT - number of tag lookups performed

©2017 Ambiq Micro, Inc.
All rights reserved.

- HIT_COUNT - number of tag lookups that result in a hit
- LINE_COUNT - number of reads that were serviced from the line buffers (on a miss or non-cached access) or directly from the RAM because they fell within the same line as the previous lookup.

The LOOKUP and LINE counts should sum to the ACCESS COUNT and the number of cache misses can be calculated as LOOKUP_COUNT - HIT_COUNT.

NOTE: The DMONn and IMONn registers should be read with the cache monitor disabled (CACHECFG[ENABLE_MONITOR] = 0x0).

Cache monitor counters will automatically freeze the counts when either of the access counters reaches a value of 0xFFFF0000 to prevent the counters from rolling over. The monitor counts can be reset at any time by writing the RESET_STAT bit in the CACHECTRL register.

The monitors do not provide an indication of waitstates added to accesses, so the elapsed time should be used to infer this value (waitstates are added as a result of cache misses or contention for the tag lookup if both busses require a simultaneous lookup).

3.9.3.2 CACHECTRL Registers

Flash Cache Controller

INSTANCE 0 BASE ADDRESS:0x40018000

©2017 Ambiq Micro, Inc.
All rights reserved.

3.9.3.2.1 Register Memory Map

Table 177: CACHECTRL Register Map

Address(s)	Register Name	Description
0x40018000	CACHECFG	Flash Cache Control Register
0x40018004	FLASHCFG	Flash Control Register
0x40018008	CACHECTRL	Cache Control
0x40018010	NCR0START	Flash Cache Noncachable Region 0 Start Address.
0x40018014	NCR0END	Flash Cache Noncachable Region 0 End
0x40018018	NCR1START	Flash Cache Noncachable Region 1 Start
0x4001801C	NCR1END	Flash Cache Noncachable Region 1 End
0x40018030	CACHEMODE	Flash Cache Mode Register. Used to trim performance/power.
0x40018040	DMON0	Data Cache Total Accesses
0x40018044	DMON1	Data Cache Tag Lookups
0x40018048	DMON2	Data Cache Hits
0x4001804C	DMON3	Data Cache Line Hits
0x40018050	IMON0	Instruction Cache Total Accesses
0x40018054	IMON1	Instruction Cache Tag Lookups
0x40018058	IMON2	Instruction Cache Hits
0x4001805C	IMON3	Instruction Cache Line Hits

©2017 Ambiq Micro, Inc.
All rights reserved.

3.9.3.2.2 CACHECTRL Registers

3.9.3.2.2.1 CACHECFG Register

Flash Cache Control Register

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x40018000

Flash Cache Control Register

Table 178: CACHECFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD							ENABLE_MONITOR	RSVD			DATA_CLKGATE	SMDLY				DLY				CACHE_LS	CACHE_CLKGATE	DCACHE_ENABLE	ICACHE_ENABLE	SERIAL	CONFIG			ENABLE_NC1	ENABLE_NC0	LRU	ENABLE

Table 179: CACHECFG Register Bits

Bit	Name	Reset	RW	Description
31:25	RSVD	0x0	RO	This bitfield is reserved for future use.
24	ENABLE_MONITOR	0x0	RW	Enable Cache Monitoring Stats.Only enable this for debug/performance analysis since it will consume additional power.See IMON/DMON registers for data.
23:21	RSVD	0x0	RO	This bitfield is reserved for future use.
20	DATA_CLKGATE	0x1	RW	Enable clock gating of entire cache data array subsystem. This should be enabled for normal operation.
19:16	SMDLY	0x6	RW	Unused. Should be left at default value.
15:12	DLY	0x6	RW	Unused. Should be left at default value.
11	CACHE_LS	0x1	RW	Enable LS (light sleep) of cache RAMs. This should not be enabled for normal operation. When this bit is set, the cache's RAMS will be put into light sleep mode while inactive. NOTE: If the cache is actively used, this may have an adverse affect on power since entering/exiting LS mode may consume more power than would be saved.
10	CACHE_CLKGATE	0x1	RW	Enable clock gating of individual cache RAMs. This bit should be enabled for normal operation for lowest power consumption.
9	DCACHE_ENABLE	0x0	RW	Enable Flash Data Caching. When set to 1, all instruction accesses to flash will be cached.
8	ICACHE_ENABLE	0x0	RW	Enable Flash Instruction Caching. When set to 1, all instruction accesses to flash will be cached.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 179: CACHECFG Register Bits

Bit	Name	Reset	RW	Description
7	SERIAL	0x0	RW	Bitfield should always be programmed to 0.
6:4	CONFIG	0x5	RW	Sets the cache configuration. Only a single configuration of 0x5 is valid. W2_128B_512E = 0x5 - Two-way set associative, 128-bit linesize, 512 entries (8 SRAMs active)
3	ENABLE_NC1	0x0	RW	Enable Non-cacheable region 1. See the NCR1 registers to set the region boundaries and size.
2	ENABLE_NC0	0x0	RW	Enable Non-cacheable region 0. See the NCR0 registers to set the region boundaries and size.
1	LRU	0x0	RW	Sets the cache replacement policy. 0=LRR (least recently replaced), 1=LRU (least recently used). LRR minimizes writes to the TAG SRAM and is recommended.
0	ENABLE	0x0	RW	Enables the main flash cache controller logic and enables power to the cache RAMs. Instruction and Data caching need to be enabled independently using the ICACHE_ENABLE and DCACHE_ENABLE bits.

3.9.3.2.2.2FLASHCFG Register

Flash Control Register

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x40018004

Flash Control Register

Table 180: FLASHCFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													RD_WAIT		

Table 181: FLASHCFG Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	This bitfield is reserved for future use.
2:0	RD_WAIT	0x1	RW	Sets read waitstates for flash accesses (in clock cycles). This should be left at the default value for normal flash operation.

3.9.3.2.2.3CACHECTRL Register

Cache Control

OFFSET: 0x00000008

©2017 Ambiq Micro, Inc.
All rights reserved.

INSTANCE 0 ADDRESS: 0x40018008

Cache Control

Table 182: CACHECTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					FLASH1_SLM_ENABLE	FLASH1_SLM_DISABLE	FLASH1_SLM_STATUS	RSVD	FLASH0_SLM_ENABLE	FLASH0_SLM_DISABLE	FLASH0_SLM_STATUS	RSVD	CACHE_READY	RESET_STAT	INVALIDATE

Table 183: CACHECTRL Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	This bitfield is reserved for future use.
10	FLASH1_SLM_ENABLE	0x0	WO	Enable Flash Sleep Mode. After writing this bit, the flash instance 1 will enter a low-power mode until the CPU writes the SLM_DISABLE bit or a flash access occurs. Wake from SLM requires ~5us, so this should only be set if the flash will not be accessed for reasonably long time.
9	FLASH1_SLM_-DISABLE	0x0	WO	Disable Flash Sleep Mode. Allows CPU to manually disable SLM mode. Performing a flash read will also wake the array.
8	FLASH1_SLM_STATUS	0x0	RO	Flash Sleep Mode Status. When 1, flash instance 1 is asleep.
7	RSVD	0x0	RO	This bitfield is reserved for future use.
6	FLASH0_SLM_ENABLE	0x0	WO	Enable Flash Sleep Mode. After writing this bit, the flash instance 0 will enter a low-power mode until the CPU writes the SLM_DISABLE bit or a flash access occurs. Wake from SLM requires ~5us, so this should only be set if the flash will not be accessed for reasonably long time.
5	FLASH0_SLM_-DISABLE	0x0	WO	Disable Flash Sleep Mode. Allows CPU to manually disable SLM mode. Performing a flash read will also wake the array.
4	FLASH0_SLM_STATUS	0x0	RO	Flash Sleep Mode Status. When 1, flash instance 0 is asleep.
3	RSVD	0x0	RO	This bitfield is reserved for future use.
2	CACHE_READY	0x0	RO	Cache Ready Status. A value of 1 indicates the cache is enabled and not processing an invalidate operation.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 183: CACHECTRL Register Bits

Bit	Name	Reset	RW	Description
1	RESET_STAT	0x0	WO	Writing a 1 to this bitfield will reset the cache monitor statistics (DMON0-3, IMON0-3). Statistic gathering can be paused/stopped by disabling the MONITOR_ENABLE bit in CACHECFG, which will maintain the count values until the stats are reset by writing this bitfield. CLEAR = 0x1 - Clear Cache Stats
0	INVALIDATE	0x0	WO	Writing a 1 to this bitfield invalidates the flash cache contents. GO = 0x1 - Initiate a programming operation to flash info.

3.9.3.2.2.4NCR0START Register

Flash Cache Noncachable Region 0 Start Address.

OFFSET: 0x00000010

INSTANCE 0 ADDRESS: 0x40018010

Flash Cache Noncachable Region 0 Start Address.

Table 184: NCR0START Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD												ADDR																RSVD			

Table 185: NCR0START Register Bits

Bit	Name	Reset	RW	Description
31:20	RSVD	0x0	RO	This bitfield is reserved for future use.
19:4	ADDR	0x0	RW	Start address for non-cacheable region 0. The physical address of the start of this region should be programmed to this register and must be aligned to a 16-byte boundary (thus the lower 4 address bits are unused).
3:0	RSVD	0x0	RO	This bitfield is reserved for future use.

3.9.3.2.2.5NCR0END Register

Flash Cache Noncachable Region 0 End

OFFSET: 0x00000014

INSTANCE 0 ADDRESS: 0x40018014

Flash Cache Noncachable Region 0 End

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 186: NCR0END Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD												ADDR																RSVD			

Table 187: NCR0END Register Bits

Bit	Name	Reset	RW	Description
31:20	RSVD	0x0	RO	This bitfield is reserved for future use.
19:4	ADDR	0x0	RW	End address for non-cacheable region 0. The physical address of the end of this region should be programmed to this register and must be aligned to a 16-byte boundary (thus the lower 4 address bits are unused).
3:0	RSVD	0x0	RO	This bitfield is reserved for future use.

3.9.3.2.2.6NCR1START Register

Flash Cache Noncachable Region 1 Start

OFFSET: 0x00000018

INSTANCE 0 ADDRESS: 0x40018018

Flash Cache Noncachable Region 1 Start

Table 188: NCR1START Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD												ADDR																RSVD			

Table 189: NCR1START Register Bits

Bit	Name	Reset	RW	Description
31:20	RSVD	0x0	RO	This bitfield is reserved for future use.
19:4	ADDR	0x0	RW	Start address for non-cacheable region 1. The physical address of the start of this region should be programmed to this register and must be aligned to a 16-byte boundary (thus the lower 4 address bits are unused).
3:0	RSVD	0x0	RO	This bitfield is reserved for future use.

©2017 Ambiq Micro, Inc.
All rights reserved.

3.9.3.2.2.7NCR1END Register

Flash Cache Noncachable Region 1 End

OFFSET: 0x0000001C

INSTANCE 0 ADDRESS: 0x4001801C

Flash Cache Noncachable Region 1 End

Table 190: NCR1END Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD												ADDR																RSVD			

Table 191: NCR1END Register Bits

Bit	Name	Reset	RW	Description
31:20	RSVD	0x0	RO	This bitfield is reserved for future use.
19:4	ADDR	0x0	RW	End address for non-cacheable region 1. The physical address of the end of this region should be programmed to this register and must be aligned to a 16-byte boundary (thus the lower 4 address bits are unused).
3:0	RSVD	0x0	RO	This bitfield is reserved for future use.

3.9.3.2.2.8DMON0 Register

Data Cache Total Accesses

OFFSET: 0x00000040

INSTANCE 0 ADDRESS: 0x40018040

Data Cache Total Accesses

Table 192: DMON0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DACCESS_COUNT																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 193: DMON0 Register Bits

Bit	Name	Reset	RW	Description
31:0	DAC-CESS_COUNT	0x0	RO	Total accesses to data cache

3.9.3.2.2.9DMON1 Register

Data Cache Tag Lookups

OFFSET: 0x00000044

INSTANCE 0 ADDRESS: 0x40018044

Data Cache Tag Lookups

Table 194: DMON1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLOOKUP_COUNT																															

Table 195: DMON1 Register Bits

Bit	Name	Reset	RW	Description
31:0	DLOOK-UP_COUNT	0x0	RO	Total tag lookups from data cache

3.9.3.2.2.10DMON2 Register

Data Cache Hits

OFFSET: 0x00000048

INSTANCE 0 ADDRESS: 0x40018048

Data Cache Hits

Table 196: DMON2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DHIT_COUNT																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 197: DMON2 Register Bits

Bit	Name	Reset	RW	Description
31:0	DHIT_COUNT	0x0	RO	Cache hits from lookup operations

3.9.3.2.2.11DMON3 Register

Data Cache Line Hits

OFFSET: 0x0000004C

INSTANCE 0 ADDRESS: 0x4001804C

Data Cache Line Hits

Table 198: DMON3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLINE_COUNT																															

Table 199: DMON3 Register Bits

Bit	Name	Reset	RW	Description
31:0	DLINE_COUNT	0x0	RO	Cache hits from line cache

3.9.3.2.2.12IMON0 Register

Instruction Cache Total Accesses

OFFSET: 0x00000050

INSTANCE 0 ADDRESS: 0x40018050

Instruction Cache Total Accesses

Table 200: IMON0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IACCESS_COUNT																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 201: IMON0 Register Bits

Bit	Name	Reset	RW	Description
31:0	IAC-CESS_COUNT	0x0	RO	Total accesses to Instruction cache

3.9.3.2.2.13IMON1 Register

Instruction Cache Tag Lookups

OFFSET: 0x00000054

INSTANCE 0 ADDRESS: 0x40018054

Instruction Cache Tag Lookups

Table 202: IMON1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ILOOKUP_COUNT																															

Table 203: IMON1 Register Bits

Bit	Name	Reset	RW	Description
31:0	ILOOK-UP_COUNT	0x0	RO	Total tag lookups from Instruction cache

3.9.3.2.2.14IMON2 Register

Instruction Cache Hits

OFFSET: 0x00000058

INSTANCE 0 ADDRESS: 0x40018058

Instruction Cache Hits

Table 204: IMON2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IHIT_COUNT																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 205: IMON2 Register Bits

Bit	Name	Reset	RW	Description
31:0	IHIT_COUNT	0x0	RO	Cache hits from lookup operations

3.9.3.2.2.15IMON3 Register

Instruction Cache Line Hits

OFFSET: 0x0000005C

INSTANCE 0 ADDRESS: 0x4001805C

Instruction Cache Line Hits

Table 206: IMON3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ILINE_COUNT																															

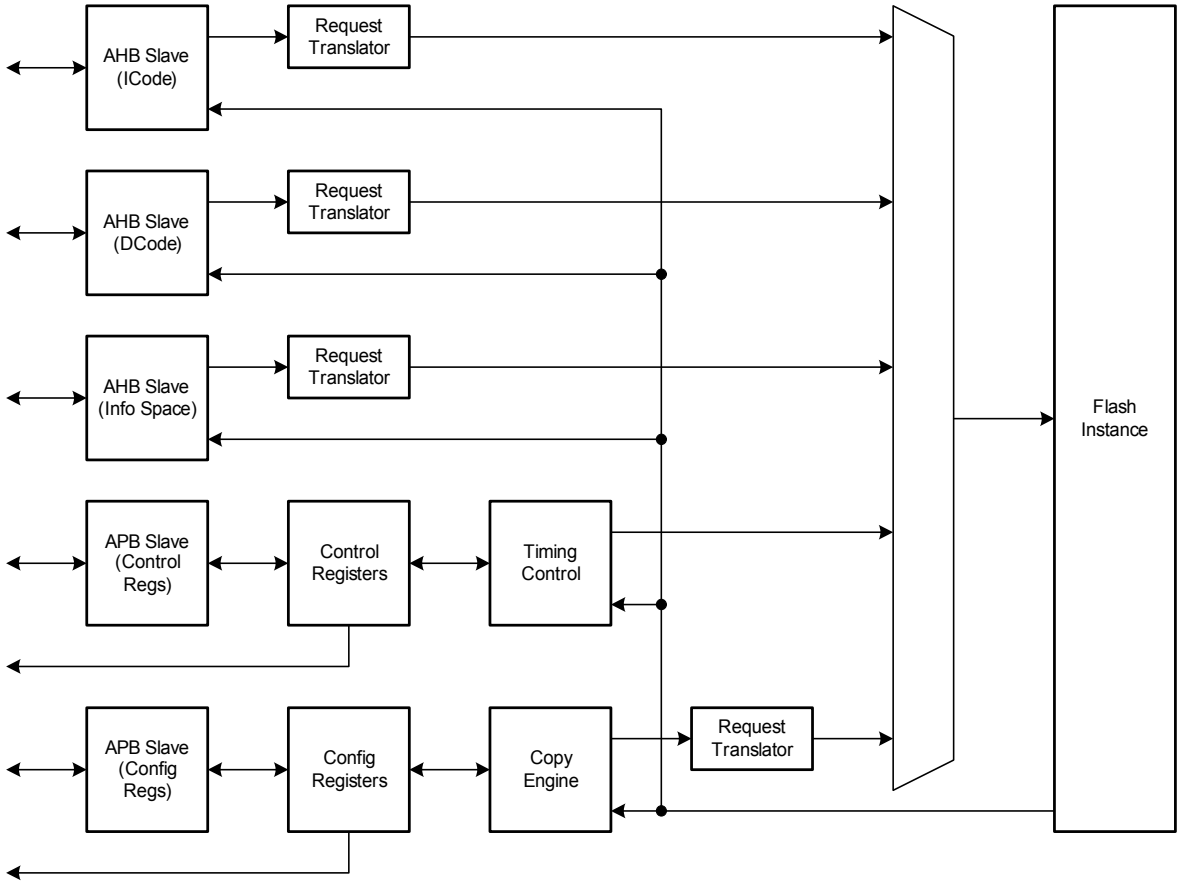
Table 207: IMON3 Register Bits

Bit	Name	Reset	RW	Description
31:0	ILINE_COUNT	0x0	RO	Cache hits from line cache

©2017 Ambiq Micro, Inc.
All rights reserved.

3.9.3.3 Flash Memory Controller

Figure 7. Block diagram for the Flash Memory Controller



3.9.3.3.1 Functional Overview

During normal MCU code execution, the Flash Memory Controller translates requests from the CPU core (via the Flash cache) to the Flash Memory instance for instruction and data fetches. The Controller is designed to return data to the cache in single wait-state and can operate up to the maximum operating frequency of half the CPU core.

The Controller facilitates flash erase and programming operations through the control registers. When erase or programming operations are active, data cannot be fetched from the Flash memory. This will be naturely handled by the cache controller fill logic to stall until the program operation is complete and the Flash device is available. With the cache enabled, this collision should happen very infrequently.

Another function of the Controller is to capture the configuration values which are distributed to the various on-chip peripherals of the MCU at chip power-up. These are read from the Information Space of the Flash Memory and captured in registers to be used by the other peripherals. The configuration values are reloaded each time a full-chip POI cycle occurs.

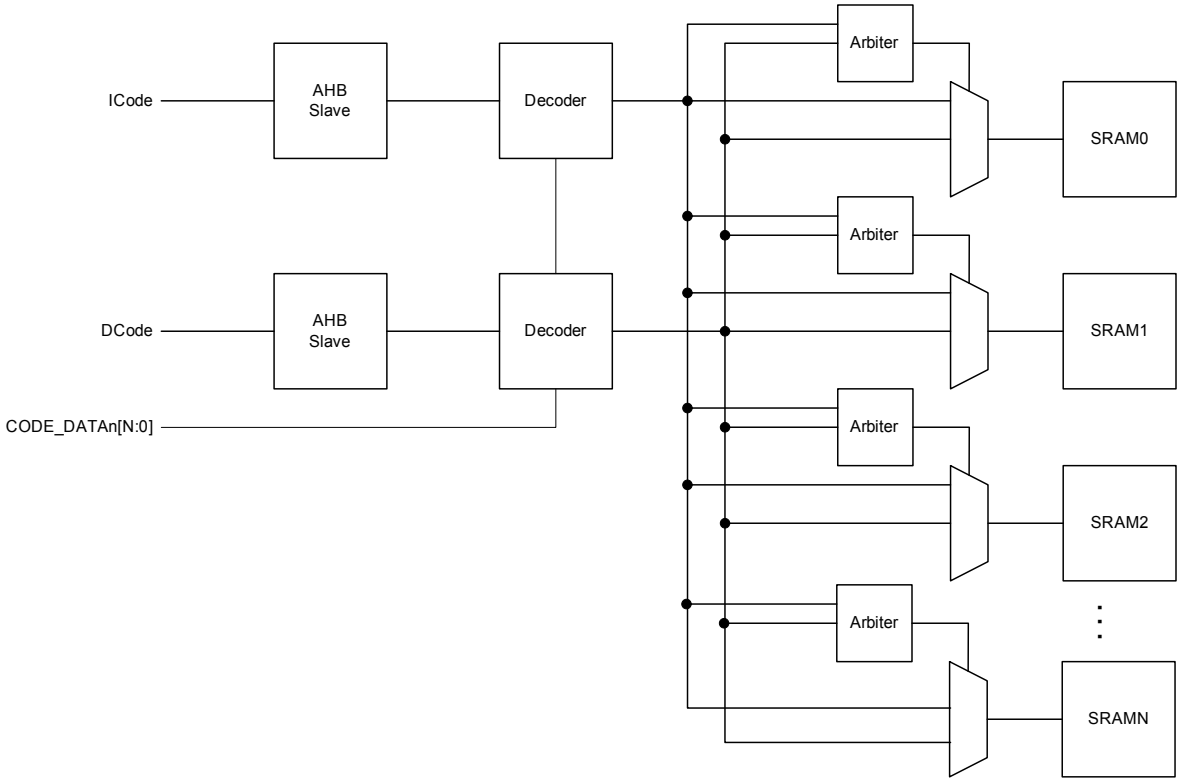
Figure 7 shows a block diagram of the Flash Memory Controller.

©2017 Ambiq Micro, Inc.
All rights reserved.

3.9.4 SRAM Interface

3.9.4.1 Functional Overview

Figure 8. Block diagram for the SRAM Interface



The SRAM Interface translates requests from the CPU core to the SRAM Memory Instances for instruction s and data fetches. The Interface is designed to return data in zero wait-states and can operate up to the maximum operating frequency of the CPU core. The Interface contains arbitration logic for each SRAM instance which allows one of 2 bus slaves access to the SRAM on any given cycle.

Figure 8 shows a logical block diagram of the SRAM Interface.

©2017 Ambiq Micro, Inc.
All rights reserved.

4. Bluetooth Low Energy Sub-system

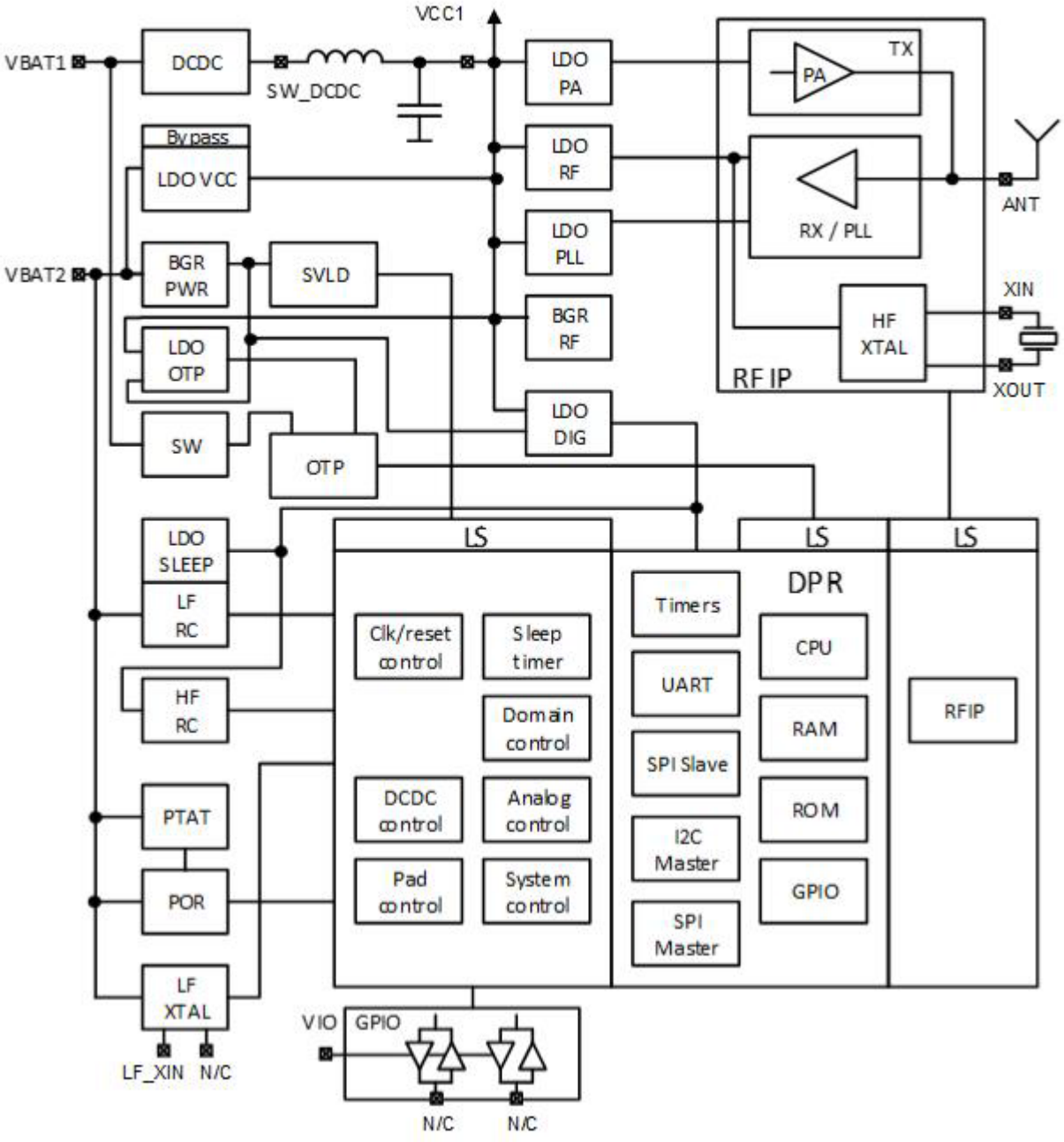


Figure 9. Block Diagram for the Bluetooth Low Energy Sub-system

4.1 Functional Overview

4.1.1 Introduction

The low power Bluetooth low energy sub-system (BLE) is optimized for Bluetooth V4.2 low energy applications. Included in ROM is a Bluetooth V4.2 link layer with a Host Controller Interface (HCI). The

©2017 Ambiq Micro, Inc.
All rights reserved.

Bluetooth low energy controller and host can be configured to support up to eight simultaneous connections. Secure connections and extended packet length are also supported per the Bluetooth V4.2 standard.

The BLE includes a sophisticated on-chip power management system with automatic configuration for 1.5V or 3V batteries. Current consumption is minimized for all modes of the application utilizing an efficient scheduler and memory manager. Several memory configuration options allow for optimum performance for any given application. A stable, low-power sleep oscillator (RC) minimizes power consumption while in a connected state. The XTAL input pad is internally connected to the Apollo2 MCU.

The BLE features a state-of-the-art 2.4 GHz transceiver, which is an extremely low-power receiver with excellent sensitivity/selectivity, and a programmable transmitter for optimized output power and current consumption.

4.1.2 Main Features

The highlighted features of the BLE are as follows:

Bluetooth V4.2 Low Energy Technology

- Full on-chip link layer and stack in ROM
- SPI HCI Transport Layer
- Up to eight simultaneous connections supported
- Extended PDU length and enhanced security
- AES-128 Hardware Encryption Engine

Firmware Over-the-Air Updating

- Per application, function, or configuration

High Performance RF

- -95dBm Bluetooth low energy receiver sensitivity
- -40 to +5dBm transmitter output power range

4.1.3 Typical Applications

The BLE is a 2.4 GHz RF system on chip with the following target applications:

- Bluetooth V4.2 Controller Mode
  - Host connect to controller via Host Controller Interface (HCI)
  - HCI interface implemented via SPI transport layer
  - Link layer implemented in ROM
  - Up to 8 simultaneous connections supported
  - Long packet lengths (Payload up to 251 bytes) supported

4.2 Functional Description

A block diagram of the BLE is shown in Figure 9 with the power management configured in Step-Down Mode. Note that not all of the functionality depicted in the figure is accessible or available for general use. The main blocks are the Digital Processing Block (DPR), the RF block, the Power Management Logic (PML), the Power Management Blocks, and the General Purpose Input Output blocks (GPIO).

The battery is connected to VBAT1 and VBAT2. The DCDC block generates VCC through the switching node and external filter. (VCC is optionally generated by the LDO_VCC block if the external filter is not present.) A number of power management blocks are connected to VBAT2 including a low-power band-gap voltage reference circuit (BGR_PWR), a supply voltage level detector (SVLD), a low drop-out regulator for the one-time programmable (OTP) memory (LDO_OTP), a low-frequency RC oscillator (LF_RC), a low-frequency crystal oscillator (LF_XTAL), a temperature-dependent bias generator, and a power-on-reset

©2017 Ambiq Micro, Inc.
All rights reserved.

(POR) block. OTP writing requires 2.25V minimum to operate and so the OTP is also connected to VBAT1 through a switch. The SVLD uses a precision band-gap (BGR_PWR) voltage reference for accurate voltage level. The main low drop-out regulators for the IC are connected to VCC, which include three regulators for the RF block (LDO_PA for the power amplifier, LDO_PLL for the frequency synthesizer, and LDO_RF for the remaining RF circuits), the DPR block (LDO_DIG), and a linear regulator used for sleep mode (LDO_SLEEP). The DPR uses BGR_PWR for a voltage reference, while the RF regulators use a low-noise bandgap circuit (BGR_RF) which is only powered when the RF block is active. The LF_XTAL block operation is optional but requires an external 32.768kHz quartz crystal if used.

The RF block operates at 2.4GHz and includes a transmitter (TX) with a programmable power amplifier (PA), a receiver (RX), and a phase-locked loop (PLL) frequency synthesizer. The PLL includes a high frequency crystal oscillator (HF_XTAL), which requires an external 48MHz quartz crystal. The RF has a significant portion implemented in logic including the modem, packet processing, and encryption, which is interfaced to the DPR CPU bus.

Level shifters (LS) are included between the various power domains to prevent cross-domain currents.

4.3 BLE Hardware Architecture

A 32-bit MCU efficiently controls the movement of data between the RF modem, memory, and the digital interfaces. Peripherals include an interrupt manager, timers, and encryption engines. The firmware is implemented in a power efficient manner using a scheduler, memory manager, hardware drivers, link layer, and stack implemented in a single ROM. The state can be retained in 4kB, 8kB, or 20kB retention memory selectable to optimize features versus memory leakage. And a one-time programmable (OTP) memory is used for trimming, unique identification numbers, profiles and patches.

The firmware can be updated or “patched” through SPI. Patches can be loaded into and executed from RAM or OTP.

A very sensitive RF front-end achieves a -95dBm typical sensitivity for Bluetooth low energy applications, while dissipating very low current (3.5mA peak). An efficient transmitter at 0dBm output power and dissipates only 5.5mA. Programmable RF power levels from -40dBm up to +5dBm are possible. A direct connection to a 50 ohm antenna is possible; however some applications will require an RF filter to suppress spurious emissions. Fast mode transition times and extremely low sleep current enable very low energy application implementations.

Power consumption and battery life are optimized in all conditions. Most common battery cell technologies are directly supported including Lithium, Alkaline, Zinc-Air and Silver Oxide. For batteries providing voltage between the minimum required 1.755V and 1.9V, the on-chip DCDC converter steps up the voltage to the required internal levels. For batteries providing 1.9V up to the maximum allowable voltage of 3.6V, the on-chip DCDC converter steps the voltage down internally for efficient power consumption. Very few external components are necessary for the DCDC converter operation; however, it is also possible to operate without the converter or using an external converter to minimize component count even further.

Memories are included for the following functions (size shown in parentheses):

- ROM (136kB) – used for the start-up sequence, Bluetooth low energy link layer, and stack
- iRAM (48kB) – used for patch development
- dRAMs (4, 4, and 12kB) – used for data with optional state retention
- dRAM (8kB) – used for data without state retention
- iRAM (4kB) – used for the subroutine jump table
- OTP (128k) – used for configuration data and ROM patches

The memory architecture is divided into several different power domains for power consumption optimizations. When a memory is not being used, it can be switched off to reduce current consumption. During Bluetooth connected sleep mode the entire MCU subsystem can be shut off and only the power management system and required state retention memories (if any) need to be powered. The power

©2017 Ambiq Micro, Inc.
All rights reserved.

management system will properly wakeup the MCU subsystem when it is needed. The RF modem is also on a separate supply domain and is turned on and off as needed in order to minimize energy consumption.

The SPI slave is used for communication with the Apollo2 MCU. The standard Host-Controller Interface (HCI) is implemented for communicating with the link layer, and a proprietary Application-Controller Interface (ACI) is implemented for communicating with the stack and profiles. Other peripherals include an interrupt manager and three timers for low power implementations, and an AES-128 encryption engine for security implementation. A NIST compliant true random number generator is also included for key generation.

4.4 BLE Software Architecture

The firmware is implemented in a power efficient manner using a basic scheduler and memory manager. Details of the support software are provided under separate cover, and is discussed here at only a high level. The embedded software or firmware provides an embedded application framework to support Bluetooth connectivity and communication when coupled with a link layer and Bluetooth stack.

The Bluetooth V4.2 compliant link layer is implemented at the bottom of the stack and accessed through the standard HCI interface. The link layer accesses the peripherals through hardware drivers. All Bluetooth V4.2 HCI commands are implemented and additionally some vendor specific commands are implemented. The link layer is designed to optimize power consumption in each role. The CPU is normally halted and is only activated when a task needs to be accomplished. When sleeping, states and connection information are properly stored in the retention memory and all other memories and peripherals are turned off. A low power timer is used to properly wakeup the system.

The OTP area of the BLE can be used to store configuration patches, bug fixes and data. The OTP can be written until the 128 kB space gets exhausted, this provides the opportunity to load multiple patches, multiple configurations, etc. The configuration patches help to configure the controller for various modes, for example, when more than 1 slave need to be connected or a patch supporting multiple slaves needs to be downloaded in the OTP.

To make this easy, Apollo2 Blue SDK allows downloading patches from the Apollo2 MCU to the OTP of EM9304. To create a valid patch use the EM9304's configuration tool.

4.5 RF Description

The RF transceiver exceeds the specifications and requirements of the Bluetooth V4.2 PHY specification. The main features of the RF transceiver are the following:

- Ultra-low-power: The average current in receive mode is 3.5 mA and in transmit mode at 0dBm is 5.5mA in a typical application
- Excellent RF performance: including -95dBm sensitivity and a programmable output power range from -40dBm to +5dBm
- Low-voltage: Operation from 3.6V down to 1.755V
- Ease of use: Separate power supply for optimized power consumption and no external matching components
- Very high degree of integration: small footprint and very few external components including a single-ended 50 ohm interface

The RF transceiver block diagram is shown in Figure 10.

©2017 Ambiq Micro, Inc.
All rights reserved.

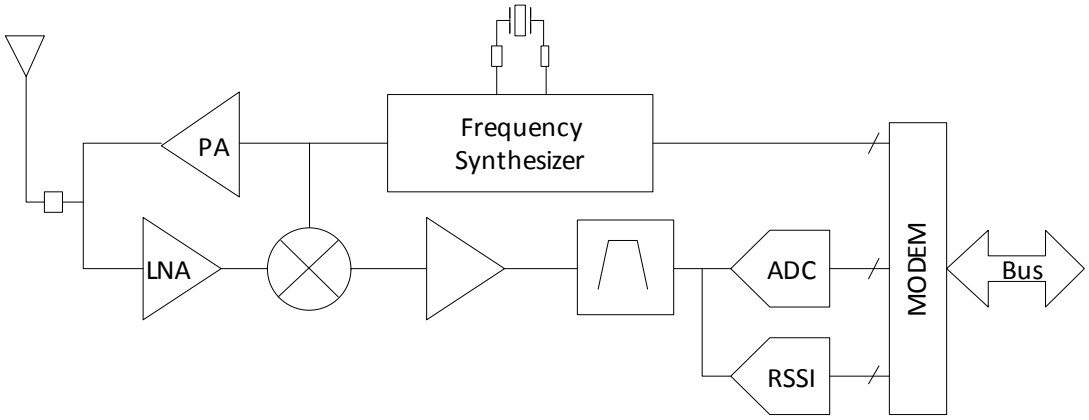


Figure 10. RF Transceiver Block Diagram

The RF transceiver is based on a low-IF architecture and comprises the following building blocks:

- Single-ended 50 Ohm RF port with on-chip harmonic filter and matching network
- High gain, low power, LNA and mixer
- Power Amplifier with programmable output power range from -
- 40Bm to +5dBm
- Low-IF receiver with 5th order channel filter and ADC converter
- RSSI with 60 dB nominal range
- Fully integrated frequency synthesis with fast settling time and digital modulation
- 48MHz XTAL reference with finely trimmable internal loading capacitor
- Fully integrated FSK-based modem, with programmable pulse shape, data rate and modulation index
- Digital baseband (DBB) with Link layer functionalities, including automatic packet handling with preamble & sync, CRC, separate Rx and Tx 128-bytes FIFOs, support of Bluetooth
- V4.2 specification long packets, early signaling of incoming packet, and integrated CCM-AES

4.6 Power Management

An advanced power management system is implemented in the BLE. Key low-power circuits include a configurable and highly-efficient DCDC converter, low noise band-gap references, low drop-out regulators (LDOs), a high frequency RC oscillator for efficient MCU operation, and a high accuracy, low frequency, RC oscillator for sleep mode control. A sophisticated digital control system optimizes power consumption and battery life in all conditions.

4.6.1 Power Management Configurations

The two power configurations which can be used on the Apollo2 Blue for the BLE are the DCDC Step-Down configuration and the DCDC Step-Up configuration. The Step-Down configuration is required when the supplied voltage is between 1.9V and Apollo2 Blue's specified upper limit of 3.6V, while the Step-Up configuration supports supply voltages between Apollo2 Blue's lower specified limit of 1.755V and 1.9V.

In Step-Down configuration, the supply voltage is applied to VBAT1 which powers the DCDC converter and OTP, and VBAT2 which powers key analog circuits in the power management. Using the SW_DCDC pin, a coil and capacitor, the DCDC converter operates in step-down mode and efficiently generates 1.25V on the VCC pin. This is the main supply voltage for the rest of the BLE during normal operation. During sleep mode the DCDC operation is off and an optional charging circuit can be used to maintain VCC.

Please refer to the Apollo2 Blue EVB schematic on the Ambiq Micro website as a reference for how power should be connected to the Apollo2 Blue device for BLE operation in Step-Down power mode.

©2017 Ambiq Micro, Inc.
All rights reserved.

In Step-Up configuration, a typical application is connecting a battery or other supply of at least 1.755V to the BLE with the Apollo2 Blue operating between 1.755V and 1.9V. The supply voltage is applied to VCC which is the main supply for the BLE including the RF portion, and VBAT2 which powers key analog circuits in the power management. Using the SW_DCDC pin, a coil and capacitor, the DCDC converter operates in step-up mode and efficiently generates 2.6V on the VBAT1 pin to supply the OTP. During sleep mode the DCDC operation is off and an optional charging circuit is used to maintain VBAT1.

Please reference section 3.3 of the EM9304 datasheet for more information about power supply connections and power supply management. The datasheet is available here - http://www.emmicroelectronic.com/sites/default/files/public/products/datasheets/9304-ds_0.pdf.

4.7 BLE Operating Modes

The BLE has several modes of operation including several active, standby and sleep modes. Power consumption is optimized in each of these modes.

4.7.1 Mode Descriptions

The BLE operating modes are described in Table 208. Operating modes are designed to optimize power consumption during operation.

Table 208: Operating Modes

Mode	VDD supply	Clock	Description
Active RC (active mode)	Full, high load DC/DC on	RC 48MHz	CPU enabled, logic power domains controlled by CPU
Active XTAL (active mode)	Full, high load DC/DC on	XTAL 48MHz	CPU enabled, logic power domains controlled by CPU, RF controlled by CPU
Sleep (sleep mode)	DC/DC off	RC 250kHz	CPU powered-down; VCC optionally charged (on by default) DCCM0 and optionally DCCM1, DCCM2, and ICCM0 in retention mode LF RC oscillator with normal precision, PML clock reduced to 250kHz
Deep Sleep (sleep mode)	DC/DC off	RC 250kHz	CPU powered down, VCC not charged DCCM0 and optionally DCCM1, DCCM2, and ICCM0 in retention mode LF RC oscillator in low precision operation, PML clock reduced to 250kHz
Chip Disable	None	None	Chip disabled

When the CPU is active, two modes are possible. Active RC mode is used with a high-frequency (HF) RC oscillator for fast turn-on and turn-off performance. This can be used to service the peripherals, for example. When the RF is required, Active XTAL mode is used with a high-accuracy crystal oscillator for channel frequency precision required by the RF standards. The crystal oscillator takes longer to turn on than the RC oscillator and more energy is consumed when in use.

In Sleep and Deep Sleep modes, the Sleep timer clock (device timing reference) can be connected either to the digitally calibrated RF low-frequency (LF) RC oscillator or to the low-frequency crystal (LF XTAL) oscillator. If the LF crystal oscillator is used, the LF RC oscillator is switched to a relaxed mode with less supply current and less accuracy. LF RC runs all the time since it is used for the power management logic. The LF crystal option brings higher clock accuracy (about 10 times), which requires a shorter RF window in

©2017 Ambiq Micro, Inc.
All rights reserved.

time for TDMA functions, hence lower average current. However, it requires an external crystal component.

Chip Disable mode is provided as the lowest power mode possible with the battery voltage still applied to the IC but all functions are disabled.

4.7.2 Mode Transitions

The mode transition diagram is shown in Figure 11. When the chip is powered from the OFF mode, enabled from Chip Disabled mode, or woken from Sleep or Deep Sleep modes, it enters the Active RC mode. Active XTAL mode is then entered if the radio is to be used to send or receive data or the HF crystal is required for other reasons. When no CPU tasks are pending the CPU is halted. If there is enough time before the next pending CPU task Sleep mode is entered. Alternatively, Deep Sleep mode can be entered by issuing the appropriate command. Sleep Mode can be disabled by software (during software development, for example) in which case the chip will remain in the Active state with the CPU halted. The chip can be woken up by the sleep timer (scheduled by the link-layer) or from pad activity such as an HCI command and enters Active RC mode as previously described. Chip Disabled mode is entered at any time by setting the ENABLE pin to logic 0.

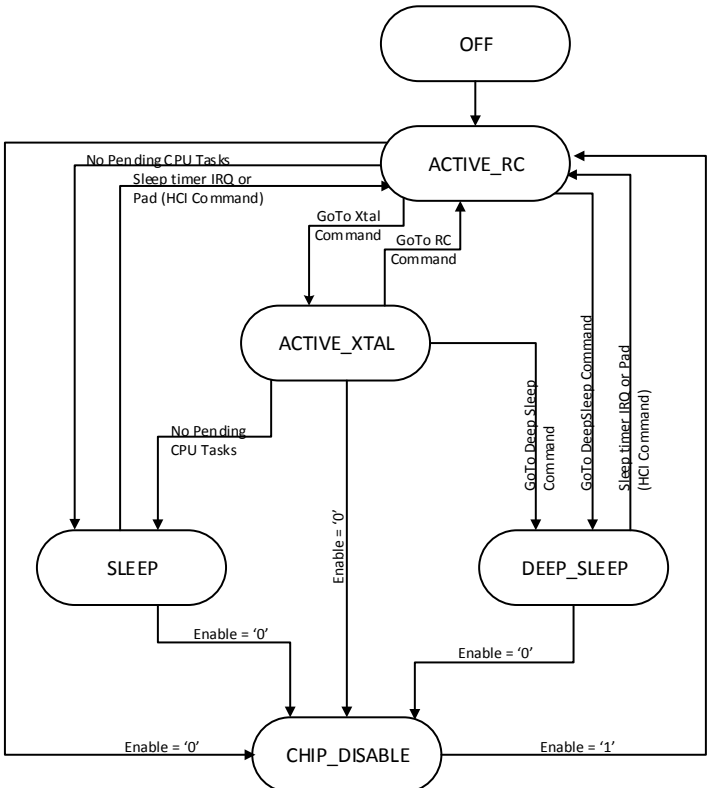


Figure 11. Mode Transitions

4.8 BLE Connections

4.8.1 External Pin Connections

Analog pins include voltage supply pins, pins for crystal oscillators, and an antenna pin for the RF.

Power is supplied through VBAT1, VBAT2, VIO and VCC depending on the power management configuration. Ground is connected to the various V_{SS} pins. Impedance of these connections should be

©2017 Ambiq Micro, Inc.
All rights reserved.

minimized for low noise performance. Ideally they should be connected directly to a ground plane on the PCB using multiple vias where possible.

NOTE: The VIO supply for the BLE and the Apollo2 VDDH supply must be at the same voltage, ideally tied to the same supply, for operational internal communication.

Two pins are provided for the 48MHz crystal (XIN, XOUT) and two are provided for the optional 32kHz crystal (LF_XIN, LF_XOUT). The RF antenna is connected to the ANT pin.

4.8.2 Internal Die-to-Die Connections

Connections between the Apollo2 Blue MCU die and the BLE die are as shown in Figure 12. Note that all pads must be configured to the functions specified in this table for proper connection to the BLE.

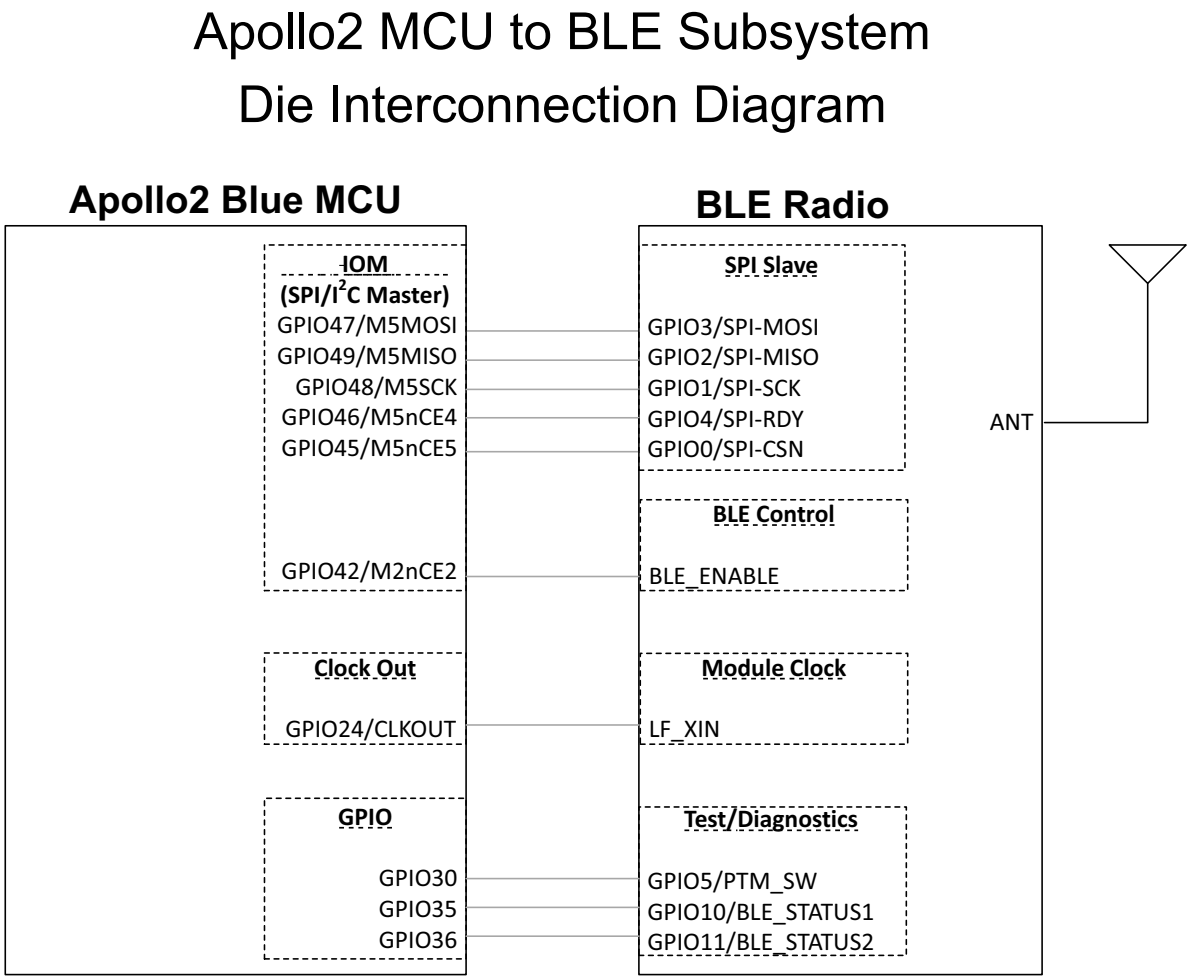


Figure 12. Die-to-Die Interconnection Diagram

Table 209provides more detail about the die-to-die interconnections.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 209: Die-to-Die Interconnection Table

Apollo2 Blue Pad	Pad Function	BLE Connection	Connections Description
GPIO24	CLKOUT	LF_XIN	32KHz clock from Apollo2 Blue to BLE.
GPIO30	GPIO30	PTM_SW (Test Pin)	BLE pins can be tri-stated to use Apollo2 Blue pins if more GPIO are needed by customer. Cannot be used if Apollo2 Blue is using BLE test and status pins.
GPIO35	GPIO35	BLE_STATUS1 (Status Info)	
GPIO36	GPIO36	BLE_STATUS2 (Status Info)	
GPIO42	M2nCE2	BLE_ENABLE (Shutdown Control)	Cannot be used since Apollo2 Blue is connected to BLE Enable pin.
GPIO45	M5nCE5	SPI- CSN	SPI connections between Apollo2 Blue and BLE Subsystem (internal connection). Brought out to package pins to allow debugging.
GPIO46	M5nCE4	SPI- RDY	
GPIO47	M5MOSI	SPI- MOSI	
GPIO48	M5SCK	SPI- SCK	
GPIO49	M5MISO	SPI- MISO	

©2017 Ambiq Micro, Inc.
All rights reserved.

5. I2C/SPI Master Module

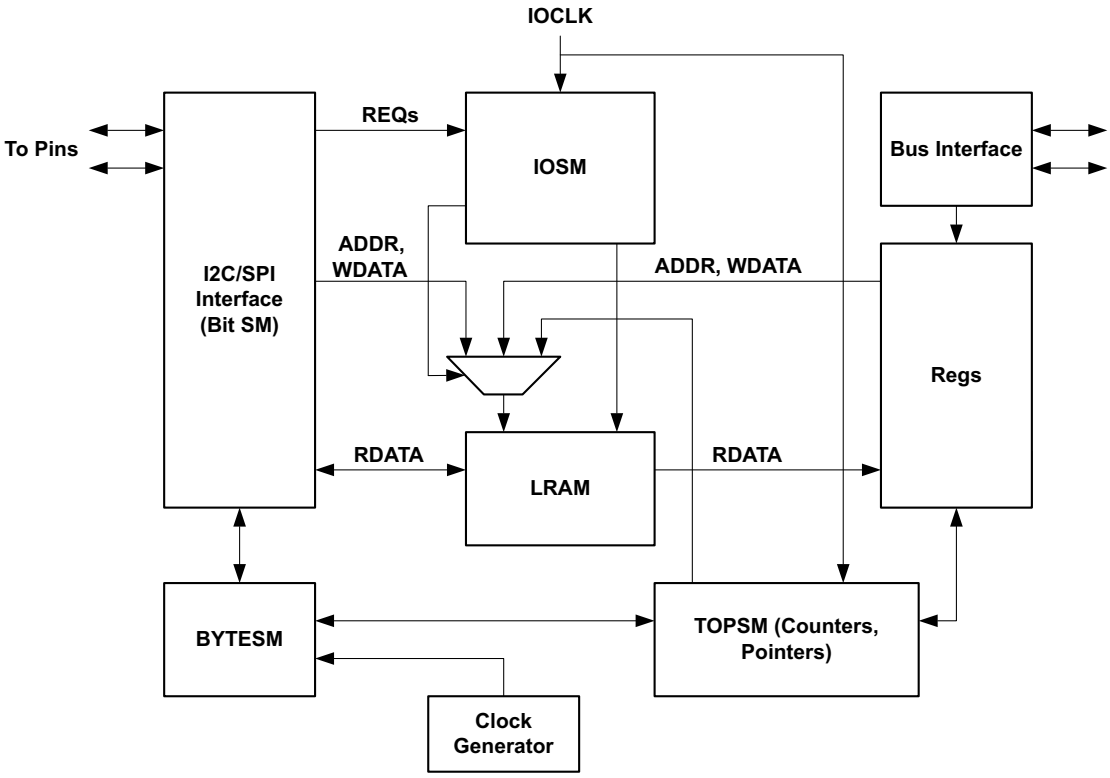


Figure 13. Block Diagram for the I2C/SPI Master Module

5.1 Functional Overview

The Apollo2 Blue includes four I2C/SPI Master Modules, shown in Figure 13, each of which functions as the Master of an I2C or SPI interface as selected by the REG_IOMSTRn_IOMCFG_IFCSEL bit (n=0 or 1). A 128-byte bidirectional FIFO and a sophisticated Command mechanism allow simple initiation of I/O operations without requiring software interaction.

In I2C mode the I2C/SPI Master supports 7- and 10-bit addressing, multi-master arbitration, interface frequencies from 1.2 kHz to 1.0 MHz and up to 255-byte burst operations. In SPI mode the I2C/SPI Master supports up to 8 slaves with automatic nCE selection, 3 and 4-wire implementation, all SPI polarity/phase combinations and up to 4095-byte burst operations, with both standard embedded address operations and raw read/write transfers. Interface timing limits are as specified in Table 782 and Table 783.

The Apollo2 Blue supports three Master SPI ports (1, 2 and 5) and two High Speed Master SPI ports (0 and 4). Master SPI port 5 is used for internal communication between the Apollo2 Blue and the BLE module and cannot be used for communication with external peripherals.

5.2 Interface Clock Generation

The I2C/SPI Master can generate a wide range of I/O interface clocks, as shown in Figure 14. The source clock is a scaled version of the HFRC 48 MHz clock, selected by REG_IOMSTRn_CLKCFG_FSEL. A divide-by-3 circuit may be selected by REG_IOMSTRn_CLKCFG_DIV3, which is particularly important in

©2017 Ambiq Micro, Inc.
All rights reserved.

creating a useful SPI frequency of 16 MHz. The output of the divide-by-3 circuit may then be divided by an 8-bit value, REG_IOMSTRn_CLKCFG_TOTPER + 1, to produce the interface clock. This structure allows very precise specification of the interface frequency, and produces a minimum available interface frequency of 1.2 kHz. If TOTPER division is enabled by REG_IOMSTRn_CLKCFG_DIVEN, the length of the low period of the clock is specified by REG_IOMSTRn_CLKCFG_LOWPER + 1. Otherwise, the clock will have a 50% duty cycle.

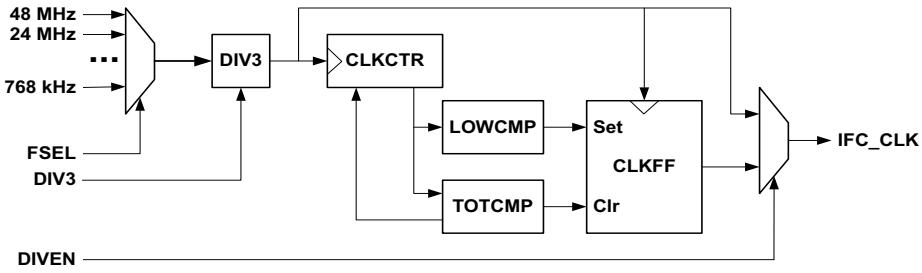


Figure 14. I²C/SPI Master Clock Generation

5.3 Command Operation

In order to minimize the amount of time the CPU must be awake during I²C/SPI Master operations, the architecture of the I²C/SPI Master is organized around processing commands which transfer data to and from an internal 128-byte FIFO. Table 210 shows the format of the CMD Register for an I2C operation, when the REG_IOMSTRn_IOMCFG_IFCSEL bit is 0. Table 211 shows the format of the CMD Register for a SPI operation, when the REG_IOMSTRn_IOMCFG_IFCSEL bit is a 1.

Table 210: CMD Register for I²C Operations

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPER			CONT	LSB	10-BIT	ADDRESS										OFFSET								LENGTH								

Table 211: CMD Register for SPI Operations

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPER			CONT	LSB	UPLNGTH				RSVD				CHN			OFFSET								LENGTH								

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 212: CMD Register Field Description

Bit	Name	Reset	RW	Description
31:29	OPER	0x0	RW	This field describes the operation. The valid operations are: 000: Normal Write 010: Raw Write 100: Normal Read 110: Raw Read
28	CONT	0x0	RW	If set to 1, the operation will be continued (see Section 5.5.12 and 5.6.8)
27	LSB	0x0	RW	If set to 0, data bytes are transferred most significant bit first. If set to 1, data bytes are transferred least significant bit first.
26	10-BIT (I^2C ONLY)	0x0	RW	If set to 1, 10-bit I^2C addressing is used. If set to 0, 7-bit I^2C addressing is used.
25:16	ADDRESS (I^2C ONLY)	0x0	RW	Address of the slave device on the I^2C bus. If 7-bit addressing is specified, only the lower 7 bits of this fields are used.
26:23	UPLNGTH (SPI ONLY)	0x0	RW	This field contains the upper four bits of the 12-bit length field, allowing transfers up to 4095 bytes in SPI mode.
22:19	RSVD (SPI ONLY)	0x0	RW	RESERVED
18:16	CHN (SPI ONLY)	0x0	RW	This field selects which of the eight nCE outputs will be asserted for this transfer. This allows Apollo2 Blue to interface to up to eight separate SPI devices by simply using different CHN values.
15:8	OFFSET	0x0	RW	In I^2C mode, this field specifies the data transferred in the OFFSET byte for Normal Read and Write transfers. In SPI mode, this field specifies the first byte written in Normal Read and Write transfers. Raw transfers in either I^2C or SPI mode do not use the OFFSET field.
7:0	LENGTH	0x0	RW	This field defines the length of the transfer in bytes. For Normal Read and Write operations, the LENGTH field may be set to 0, so that only the OFFSET byte is written and no other data is transferred. In SPI mode, the UPLNGTH field contains the upper 4 bits of the LENGTH so that up to 4095 bytes may be transferred in a single operation.

For writes to the interface, software writes data to the FIFO (REG_IOMSTRn_FIFO_FIFO) and then sends a single command to the REG_IOMSTRn_CMD Register. Unless the LENGTH field of the CMD is zero, at least one word (4 bytes) of data must be written into the FIFO prior to writing the CMD Register or an ICMD interrupt will be generated and the operation will be terminated.The Command includes either the I^2C slave address or the SPI channel select, the desired address offset and the length of the transfer. At that point the I^2C/SPI Master executes the entire transfer, so the CPU can go to sleep. If more than 128 bytes are to be transferred, the Master will generate a THR interrupt when the FIFOSIZ value, REG_IOMSTRn_FIFOPTR_FIFOSIZ, drops below the write threshold REG_IOMSTRn_FIFOTHR_FIFOWTHR so the CPU can wake up and refill the FIFO. The I^2C/SPI Master will generate the CMDCMP interrupt when the command is complete. In each case, the total number of bytes transferred in each operation is specified in the LENGTH field of the CMD Register. If software executes a write to the FIFO when it is full (FIFOSIZ is greater than 124) the FOVFL interrupt will be generated and the transfer will be terminated.

For reads, the CMD Register is first written with the command and the CPU can go to sleep. The Master initiates the read and transfers read data to the FIFO. If the FIFOSZ value exceeds the read threshold REG_IOMSTRn_FIFOTHR_FIFORTHR, a THR interrupt is generated so the CPU can wake up and empty the FIFO. A CMDCMP interrupt is also generated when the Command completes. If software executes a read from the FIFO when it has less than a word of data the FUNDFL interrupt will be generated and the

©2017 Ambiq Micro, Inc.
All rights reserved.

transfer will be terminated. FUNDFL will not be generated if the read transfer has already completed, so that software can read the last FIFO word even if it is incomplete.

If the FIFO empties on a write or fills on a read, the I2C/SPI Master will simply pause the interface clock until the CPU has read or written a byte from the FIFO. This avoids the requirement that the thresholds be set conservatively so that the processor can wake up fewer times on long transfers without a risk of an underflow or overflow aborting a transfer in progress.

If software initiates an incorrect operation, such as attempting to read the FIFO on a write operation or when it is empty, or write the FIFO on a read operation or when it is full, the Master will generate an IACC error interrupt. If software attempts to write the Command Register when another Command is underway or write the CMD register with a write command when the FIFO is empty (unless the LENGTH field in the CMD is zero), the Master will generate an ICMD error interrupt.

Each operation is self-contained, and the FIFO pointers are reset at the completion of each operation. For example, it is not possible to load the data from multiple transfers into the FIFO and then execute several CMD register writes.

5.4 FIFO

The I2C/SPI Master includes a 128-byte local RAM (LRAM) for data transfers. The LRAM functions as a FIFO. Only 32-bit word accesses are supported to the FIFO from the CPU. When a write operation is underway, a word written to the FIFO will increment the REG_IOMSTRn_FIFOPTR_FIFOSIZ register by 4 and decrement the REG_IOMSTRn_FIFOPTR_FIFOREM register by 4. Reading a byte from the FIFO via the I/O interface decrements FIFOSIZ by 1 and increments FIFOREM by 1. When a read operation is underway, a word read from the FIFO decrements FIFOSIZ by 4 and increments FIFOREM by 4. A byte read from the I/O interface into the FIFO increments FIFOSIZ by 1 and decrements FIFOREM by 1. If FIFOSIZ becomes one during a write operation or 0x40 on a read operation and there is more data to be transferred, the clock of the I/O interface is paused until software accesses the FIFO.

Two threshold registers, FIFORTHR and FIFOWTHR indicate when a THR interrupt should be generated to signal the processor that data should be transferred.

5.5 I2C Interface

The I2C/SPI Master supports a flexible set of Commands to implement a variety of standard I2C operations. The I2C interface consists of two lines: one bi-directional data line (SDA) and one clock line (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor. By definition, a device that sends a message is called the “transmitter”, and the device that accepts the message is called the “receiver”. The device that controls the message transfer by driving SCL is called “master”. The devices that are controlled by the master are called “slaves”. The Apollo2 Blue I2C Master is always a master device.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

A number of bus conditions have been defined (see Figure 15) and are described in the following sections.

©2017 Ambiq Micro, Inc.
All rights reserved.

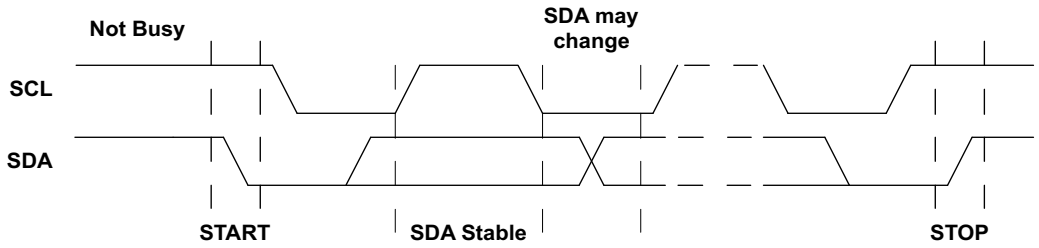


Figure 15. Basic I2C Conditions

5.5.1 Bus Not Busy

Both SDA and SCL remain high.

5.5.2 Start Data Transfer

A change in the state of SDA from high to low, while SCL is high, defines the START condition. A START condition which occurs after a previous START, but before a STOP, is called a RESTART condition, and functions exactly like a normal STOP followed by a normal START.

5.5.3 Stop Data Transfer

A change in the state of SDA from low to high, while SCL is high, defines the STOP condition.

5.5.4 Data Valid

After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

5.5.5 Acknowledge

Each byte of eight bits is followed by one acknowledge (ACK) bit as shown in Figure 16. This acknowledge bit is a low level driven onto SDA by the receiver, whereas the master generates an extra acknowledge related SCL pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, on a read transfer, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related SCL pulse. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge (a NAK) on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.If I/O Host attempts an I2C operation but no slave device generates an ACK, or if a slave fails to generate an ACK on a data byte before the transfer is complete, a NAK interrupt will be generated.

©2017 Ambiq Micro, Inc.
All rights reserved.

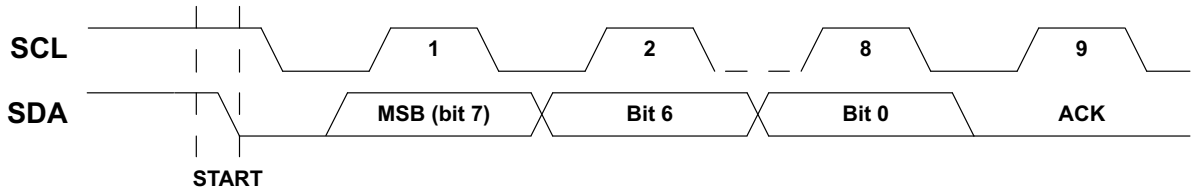


Figure 16. I²C Acknowledge

5.5.6 I²C Slave Addressing

For normal I²C reads and writes, the Command specifies the address to be sent on the interface. Both 7-bit and 10-bit addressing are supported, as selected by 10BIT in the Command. The address is specified in the ADDRESS field.

Figure 17 shows the operation in 7-bit mode in which the master addresses the slave with a 7-bit address configured as 0xD0 in the lower 7 bits of the ADDRESS field. After the START condition, the 7-bit address is transmitted MSB first. If this address matches the lower 7 bits of an attached slave device, the eighth bit indicates a write (RW = 0) or a read (RW = 1) operation and the slave supplies the ACK. If no slave acknowledges the address, the transfer is terminated and a NAK error interrupt is generated.

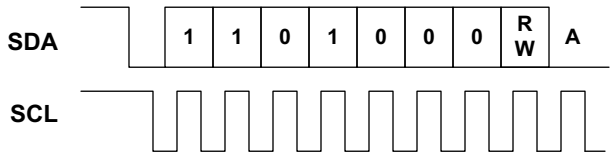


Figure 17. I²C 7-bit Address Operation

Figure 18 shows the operation with which the master addresses the Apollo2 Blue with a 10-bit address configured at 0x536. After the START condition, the 10-bit preamble 0b11110 is transmitted first, followed by the upper two bits of the ADDRESS field and the eighth bit indicating a write (RW = 0) or a read (RW = 1) operation. If the upper two bits match the address of an attached slave device, it supplies the ACK. The next transfer includes the lower 8 bits of the ADDRESS field, and if these bits also match I2CADDR the slave again supplies the ACK. If no slave acknowledges either address byte, the transfer is terminated and a NAK error interrupt is generated.

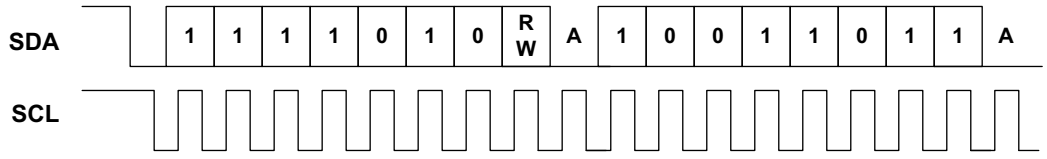


Figure 18. I²C 10-bit Address Operation

5.5.7 I²C Offset Address Transmission

If the OPER field of the CMD selects a Normal Read or Write, the I²C/SPI Master will first send an 8-bit Offset Address byte, where the offset is specified in the OFFSET field of CMD. This transfer is shown in Figure 19. The Offset Address is loaded into the Address Pointer of the slave.

©2017 Ambiq Micro, Inc.
All rights reserved.

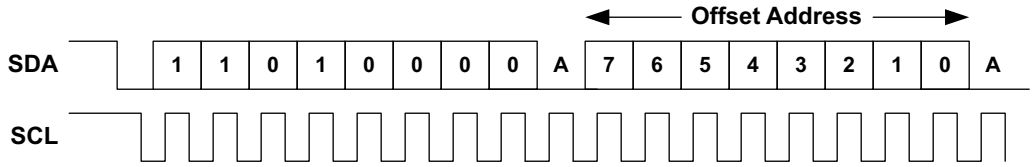


Figure 19. I²C Offset Address Transmission

5.5.8 I²C Normal Write Operation

In a Normal write operation the I²C/SPI Master transmits to a slave receiver. The Address Operation has a RW value of 0, and the second byte contains the Offset Address, as in Figure 19. The next byte is written to the slave register selected by the Address Pointer (which was loaded with the Offset Address) and the Address Pointer is incremented. Subsequent transfers write bytes into successive registers until a STOP condition is received, as shown in Figure 20.

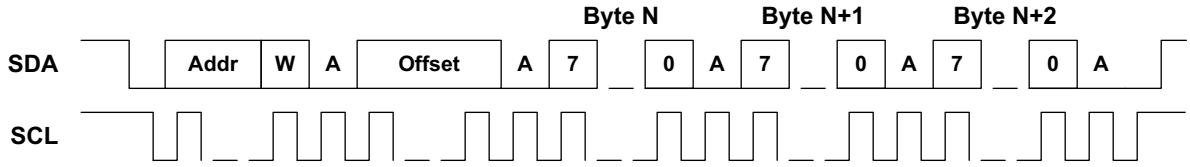


Figure 20. I²C Normal Write Operation

5.5.9 I²C Normal Read Operation

If a Normal Read operation is selected in the OPER field of the Command, the I²C/SPI Master first executes an Offset Address Transmission to load the Address Pointer of the slave with the desired Offset Address. A subsequent operation will again issue the address of the slave but with the RW bit as a 1 indicating a read operation. As shown in Figure 21, this transaction begins with a RESTART condition so that the interface will be held in a multi-master environment. After the address operation, the slave becomes the transmitter and sends the register value from the location pointed to by the Address Pointer, and the Address Pointer is incremented. Subsequent transactions produce successive register values, until the I²C/SPI Master receiver responds with a NAK and a STOP to complete the operation.

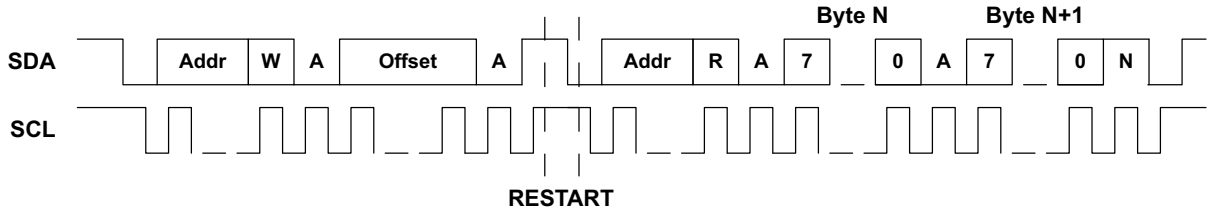


Figure 21. I²C Normal Read Operation

©2017 Ambiq Micro, Inc.
All rights reserved.

5.5.10 I²C Raw Write Operation

If a Raw Write is selected in the OPER field of the Command, the I²C/SPI Master does not execute the Offset Address Transmission, but simply begins transferring bytes as shown in Figure 22. This provides support for slave devices which do not implement the standard offset address architecture. The OFFSET field of Command is not used in this case.

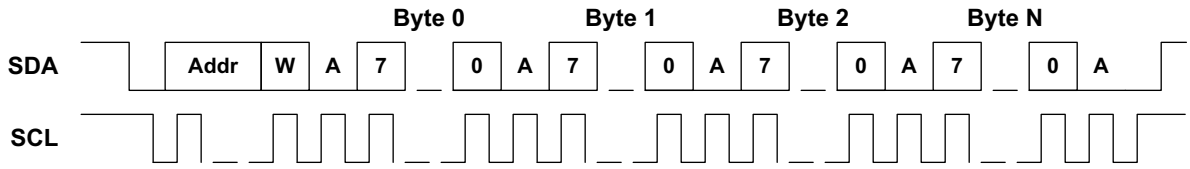


Figure 22. I²C Raw Write Operation

5.5.11 I²C Raw Read Operation

If a Raw Read is selected in the OPER field of Command, the I²C/SPI Master does not execute the Offset Address Transmission, but simply begins transferring bytes with a read as shown in Figure 23. This is important for slave devices which do not support an Address Pointer architecture. For devices which do include an Address Pointer, multiple Raw Reads may be executed after a Normal Read to access subsequent registers as the Address Pointer increments, without having to execute the Offset Address Transmission for each access.

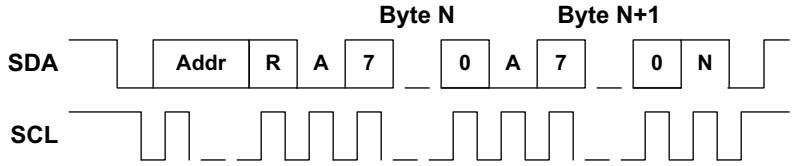


Figure 23. I²C Raw Read Operation

5.5.12 Holding the Interface with CONT

In all of the previously described transactions, the I²C/SPI Master terminates the I²C operation with a STOP sequence. In environments where there are other masters connected to the I²C interface, it may be necessary for the Apollo2 Blue to hold the interface between Commands to insure that another master does not inadvertently access the same slave that the Apollo2 Blue is accessing. In order to implement this functionality, the CONT bit should be set in the CMD Register. This will cause the I²C/SPI Master to keep SDA high at the end of the transfer so that a STOP does not occur, and the next transaction begins with a RESTART instead of a START. Note that for a Normal Read the interface is held between the Offset Address Transmission and the actual read independent of the state of CONT, but it CONT is set the read transaction will not terminate with a STOP.

5.5.13 I²C Multi-master Arbitration

The Apollo2 Blue I²C/SPI Master supports multi-master arbitration in I²C mode. There are two cases which must be handled.

©2017 Ambiq Micro, Inc.
All rights reserved.

The first is the case where another master initiates an I2C operation when the Apollo2 Blue Master is inactive. In this case the I2C/SPI Master will detect an I2C START operation on the interface and the START interrupt will be asserted, which tells the software not to generate any IO operations (which will not be executed in any case). Software then waits for the STOP interrupt, which reenables operation.

The second case is where another master initiates an operation at the same time as the Apollo2 Blue. In this case there will be a point where one master detects that it is not driving SDA low but the bus signal is low, and that master loses the arbitration to the other master. If the Apollo2 Blue I2C/SPI Master detects that it has lost arbitration, it will assert the ARB interrupt and immediately terminate its operation. Software must then wait for the STOP interrupt and re-execute the current Command.

5.6 SPI Operations

5.6.1 SPI Configuration

The I2C/SPI Master supports all combinations of the polarity (CPOL) and phase (CPHA) modes of SPI using the REG_IOMSTRn_IOMCFG_SPOL and REG_IOMSTRn_IOMCFG_SPHA bits. It also may be configured in either 3-wire or 4-wire mode. In 4-wire mode, the MOSI and MISO interface signals use separate IO pins. In 3-wire mode, MOSI and MISO are multiplexed on a single IO pin for more efficient pin utilization. The 3/4 wire configuration is selected in the mapping function of the PINCFG module.

SPI operations may transfer up to 4095 bytes in a single transfer, as the UPLNGTH field of the CMD Register is appended to the standard LENGTH field to provide a 12-bit length specification.

5.6.2 SPI Slave Addressing

In SPI mode, the Command specifies the slave channel to be used in the CHANNEL field. The I2C/SPI Master supports up to eight slaves, each of which has its own nCE signal which can be configured on an IO pin. Additional slaves may be supported using GPIO pins and external decoding.

5.6.3 SPI Normal Write

Figure 24 shows the case of a SPI Normal Write operation selected in the OPER field. The operation is initiated when the I2C/SPI Master pulls one of the eight nCE signals low. At that point the I2C/SPI Master begins generating the clock on SCK and an 8-bit Address byte is transmitted from the master on the MOSI line, with the upper RW bit indicating read (if 0) or write (if 1). In this example the RW bit is a one selecting a write operation. The entire Offset Address Byte, including the RW bit, is taken from the OFFSET field of the CMD. This means that OFFSET[7] should be set to 1 if the slave expects a RW bit. If the slave does not expect a RW bit, this allows the first byte of a write to be completely specified in the OFFSET field, and a single byte write in that case can be executed without requiring any data to be loaded in to the FIFO.

Each subsequent byte is read from the FIFO and transmitted. The operation is terminated when the I2C/SPI Master brings the nCE signal high. Note that the MISO line is not used in a write operation and is held in the high impedance state by the I2C/SPI Master.

©2017 Ambiq Micro, Inc.
All rights reserved.

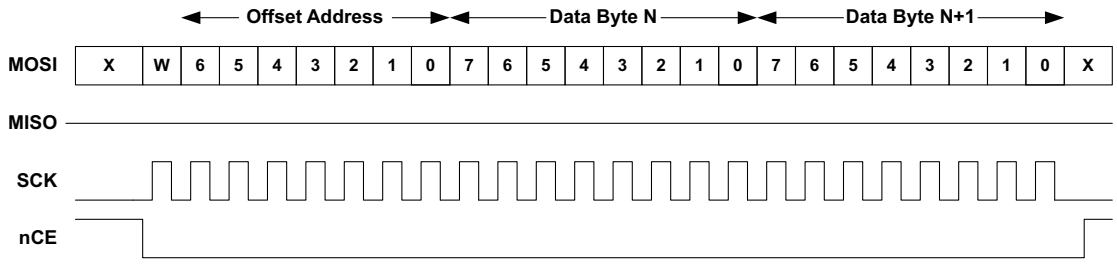


Figure 24. SPI Normal Write Operation

5.6.4 SPI Normal Read

Figure 25 shows the case of a Normal Read operation selected in the OPER field. The operation is initiated when the I^{2}C/SPI Master pulls one of the eight nCE signals low. At that point the I^{2}C/SPI Master begins driving the clock onto SCK and the address is transferred from the master to the slave just as it is in a write operation, but in this case the RW bit is a 0 indicating a read. After the transfer of the last address bit (bit 0), the I^{2}C/SPI Master stops driving the MOSI line and begins loading the FIFO with the data on the MISO line. The transfer continues until the I^{2}C/SPI Master brings the nCE line high.

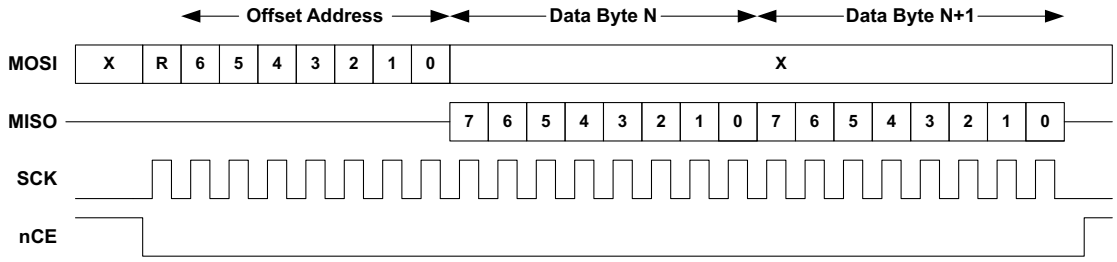
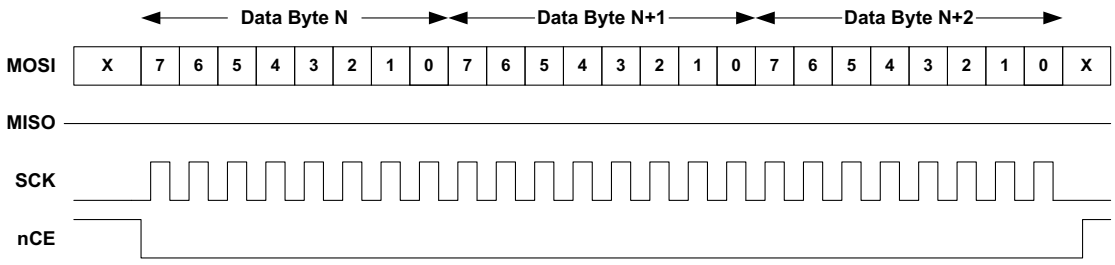


Figure 25. SPI Normal Read Operation

As with a Normal Write, the Offset Address byte including the RW bit is taken from the OFFSET field of CMD. If the slave expects an RW bit, OFFSET[7] must be set to 1. This allows reads from devices which have different formats for the address byte.

5.6.5 SPI Raw Write

If a Raw Write is selected in the OPER field, the operation is similar to a Normal Write but the Offset Address byte is not sent and all data comes directly from the FIFO as shown in Figure 26. The OFFSET field is not used in this case.



©2017 Ambiq Micro, Inc.
All rights reserved.

Figure 26. SPI Raw Write Operation

5.6.6 SPI Raw Read

If a Raw Read is selected in the OPER field, the operation is simply the data transfer portion of a Normal Read. All data goes directly to the FIFO as shown in Figure 27. The OFFSET field is not used in this case.

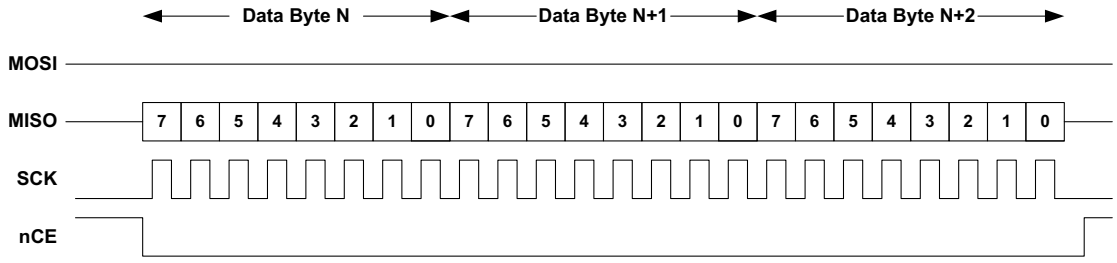


Figure 27. SPI Raw Read Operation

5.6.7 SPI 3-wire Mode

In 3-wire mode, the MOSI and MISO lines are shared on a single pin. As described in the previous sections, the MISO and MOSI lines are not driven at the same time, so 3-wire mode is equivalent to simply tying them together external to the Apollo2 Blue. 3-wire mode is configured by selecting the MxWIR3 alternative (x = 0 to 5 selecting the I2C/SPI Master) in the GPIO Pad Multiplexor rather than the MxMOSI and MxMISO alternatives. Detailed configuration information is supplied in the GPIO and Pad Configuration Module chapter.

5.6.8 Complex SPI Operations

In some cases peripheral devices require more complex transaction sequences than those supported by a single Command. In order to support these transactions, the CONT bit may be set in the Command. In this case, the nCE pin selected by the Channel will remain asserted low at the end of the transaction, so that the next SPI operation will be seen as part of the same transaction. For example, there are peripheral devices which require both a Function and an Address Offset to be transmitted at the beginning of a read. Implementing this can be done in several ways. One example as shown in Figure 28 is:

1. Execute a Raw SPI write of length 2, with the data bytes being the Function and Offset. Set the CONT bit in this Command so nCE remains asserted low.
2. Execute a Raw SPI Read of the desired transfer length. The data will then be read into the FIFO. The CONT bit is not set in this Command.

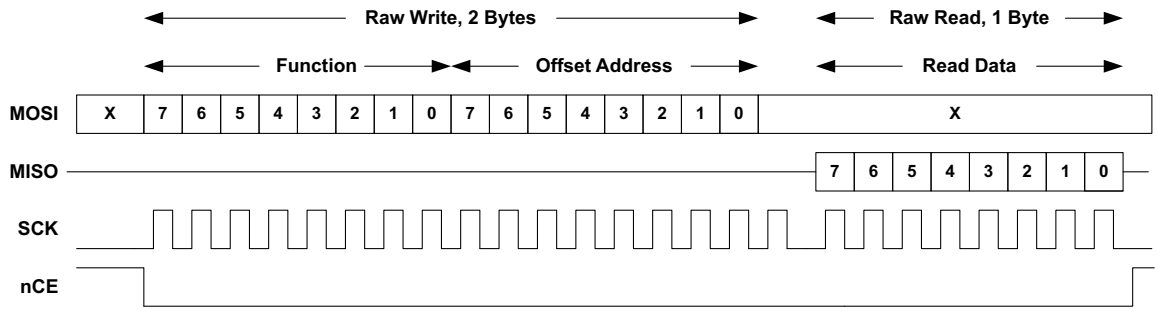


Figure 28. SPI Combined Operation

©2017 Ambiq Micro, Inc.
All rights reserved.

5.6.9 SPI Polarity and Phase

The Apollo2 Blue supports all combinations of CPOL (clock polarity) and CPHA (data phase) in SPI mode, as defined by the SPOL and SPHA bits. Figure 29 shows how these two bits affect the interface signal behavior.

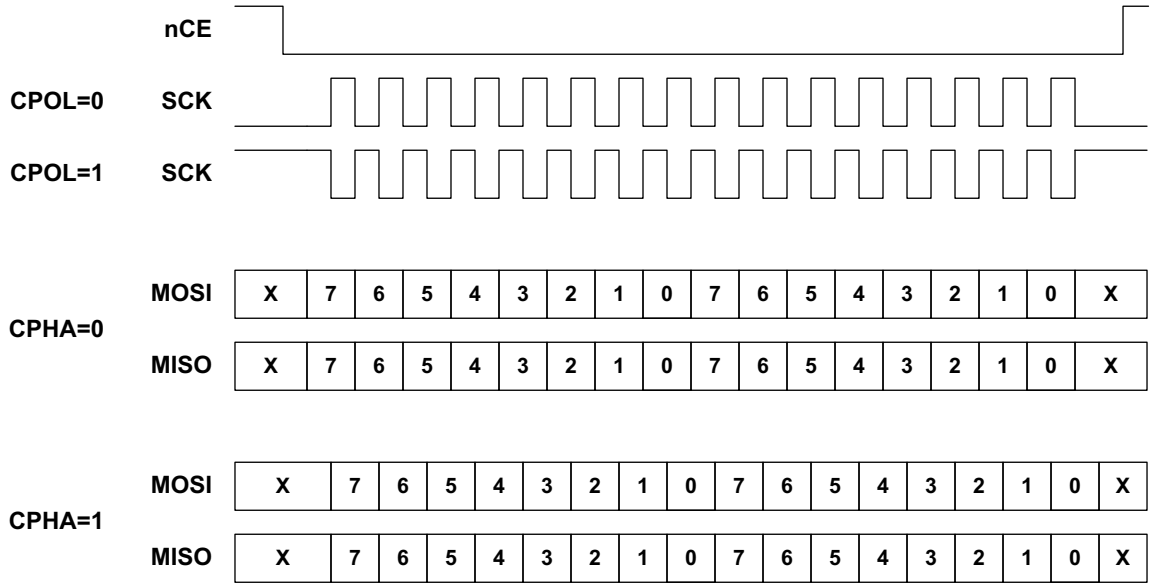


Figure 29. SPI CPOL and CPHA

If CPOL is 0, the clock SCK is normally low and positive pulses are generated during transfers. If CPOL is 1, SCK is normally high and negative pulses are generated during transfers.

If CPHA is 0, the data on the MOSI and MISO lines is sampled on the edge corresponding to the first SCK edge after nCE goes low (i.e. the rising edge if CPOL is 0 and the falling edge if CPOL is 1). Data on MISO and MOSI is driven on the opposite edge of SCK.

If CPHA is 1, the data on the MOSI and MISO lines is sampled on the edge corresponding to the second SCK edge after nCE goes low (i.e. the falling edge if CPOL is 0 and the rising edge if CPOL is 1). Data on MISO and MOSI is driven on the opposite edge of SCK.

The SPOL and SPHA bits may be changed between Commands if different slave devices have different requirements. In this case the IFCEN bit should be set to 0 either before or at the same time as SPHA and SPOL are changed, and then set back to 1 before CMD is written.

5.7 Repeating a Command

Some peripherals, particularly sensors such as accelerometers and gyroscopes, have multiple registers which hold sample data (2 bytes each of X, Y and Z are common), and FIFOs behind these registers which hold multiple samples. In order to allow software to retrieve several samples with a single operation, the Apollo2 Blue I^2C/SPI Master includes the capability to execute the same Command multiple times. If multiple Commands are desired, the REG_IOMSTRn_CMDRPT Register is loaded with the number of additional times to execute the next Command (e.g. loading CMDRPT with the value 3 will cause the next Command to be executed a total of 4 times). When a Command is written to the Command Register, the Command is then executed multiple times, filling or emptying the FIFO as appropriate. The series of repeated Commands behaves as if it was a single long Command, with a single CMDCMP interrupt occurring at the end and THR interrupts occurring if the FIFO crosses the relevant threshold. At the end of

©2017 Ambiq Micro, Inc.
All rights reserved.

any Command the CMDRPT Register has the value 0, so that single Commands may always be executed without requiring a write to CMDRPT.

As an example, assume the peripheral has 6 bytes of sensor sample data located at register offsets 10, 11, 12, 13, 14 and 15. Also assume the internal FIFO threshold of the peripheral has been set so that an interrupt occurs when the FIFO contains 8 samples. The CMDRPT register is set to 7, and a read Command is executed with an offset of 10 and a length of 6. This Command will be executed 8 times, each time bursting 6 bytes of data from registers 10-15 in the peripheral to the I^{2}C/SPI Master FIFO. When CMDCMP is received the FIFO in the I^{2}C/SPI Master will contain 48 bytes of data. The bytes of data are packed in the FIFO – there are no gaps between samples.

5.8 Bit Orientation

In both I^{2}C and SPI modes, the I^{2}C/SPI Master supports data transmission either LSB first or MSB first as configured by the LSB bit in the Command. If LSB is 0, data is transmitted and received MSB first. If LSB is 1, data is transmitted and received LSB first.

5.9 Full Duplex Operations

Some SPI slaves operate in full duplex mode, where data is transferred on both the MISO and MOSI wires at the same time. The I^{2}C/SPI Master supports this type of operation when the REG_IOMSTRn_IOMCFG_FULLDUP bit is set.

When FULLDUP is set, the I^{2}C/SPI Master splits the standard 128-byte transmit/receive FIFO into a 64-byte transmit FIFO and a 64-byte receive FIFO. A normal or raw write Command is executed, and proceeds just as a normal write transfer. FIFOREM will report the remaining FIFO area as the remainder from 64 bytes. Software must not attempt to load more than 64 bytes into the write FIFO or an IACC error will be generated. The primary difference from a normal write operation is that data received on the MISO line will be loaded into the read FIFO, with the bytes aligned to the corresponding byte in the write FIFO. Software may read the read FIFO at any time, and should use the FIFOSIZ and./or FIFOREM registers to determine when data should be read. The FIFORTHR threshold value does not generate an interrupt.

If more than 64 bytes of data are written into the read FIFO without being read by software, the read FIFO will simply wrap around and overwrite the earlier read data. This means that if a long full duplex operation only returns data at the end, software does not need to continuously empty the read FIFO but can simply drain the FIFO when the write operation is complete.

5.10 SPI Flow Control

The I^{2}C/SPI Master supports flow control from the slave, which is controlled by several configuration bits. Either read or write (or both) flow control may be implemented. Read flow control is enabled by setting the REG_IOMSTRn_IOMCFG_RDFC bit, in which case the I^{2}C/SPI Master will check the state of the Flow Control IRQ pin, and if it is inactive the SPI clock will stop at the completion of the current byte transfer until it becomes active. The Flow Control IRQ can be any of the 50 pins as selected by the REG_GPIO_IOMnIRQ register corresponding to the particular I^{2}C/SPI Master. The polarity of the active state of the Flow Control IRQ is selected by the REG_IOMSTRn_IOMCFG_RDFCPOL

Write flow control is enabled by setting the REG_IOMSTRn_IOMCFG_WTFC bit, but in this case either the Flow Control IRQ or the state of the MISO line may be used for flow control, as selected by the REG_IOMSTRn_IOMCFG_WTFCIRQ bit. If IRQ is selected by setting a one, the clock control is identical to that described for reads above and the IRQ polarity is set by the REG_IOMSTRn_IOMCFG_WTFCPOL bit. If MISO is selected by setting a zero in WTFCIRQ, the clock will be stopped if the MISO line is at the inactive polarity, which is set by the WTFCPOL bit.

©2017 Ambiq Micro, Inc.
All rights reserved.

Slave devices supporting flow control typically require specific states of the MOSI line prior to the start of a transfer. This state is controlled by the REG_IOMSTRn_IOMCFG_MOSIINV bit. If this bit is zero, MOSI will be driven to a 1 at the start of a write transaction and to a 0 at the start of a read transaction – this is the normal operation of devices with flow control support. If MOSIINV is set to one, these polarities will be inverted.

Flow control may be asserted either prior to the first byte transfer, which will delay the start of SCK, or within each byte transferred, which will pause SCK at the end of that byte. The examples below assume that WTFCPOL or RDFCPOL are set to 0.

Figure 30 shows the operation of flow control at the beginning of a write transfer or a normal read transfer which begins with an offset byte write. Either MISO or IRQ (selected by WTFCIRQ) must be deasserted low within ½ of the SCK period after nCE is asserted low in order to delay the clock. SCK will continue in its inactive state until MISO or IRQ is changed to the active state, and then will begin normal operation.

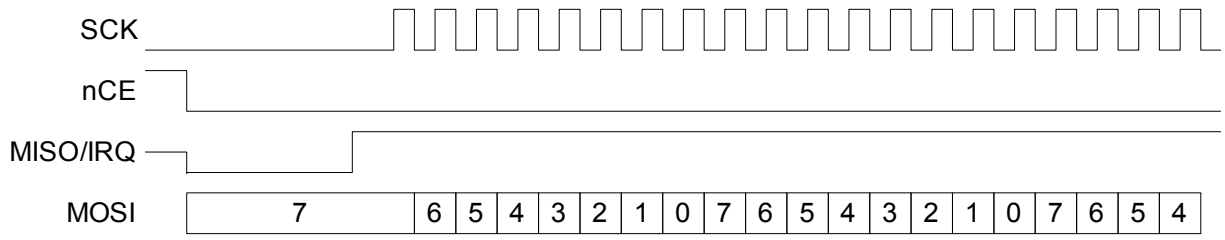


Figure 30. Flow Control at Beginning of a Write Transfer

Figure 31 shows the operation of flow control at the beginning of a raw read transfer. IRQ must be deasserted low within ½ of the SCK period after nCE is asserted low in order to delay the clock. SCK will continue in its inactive state until IRQ is changed to the active state, and then will begin normal operation.

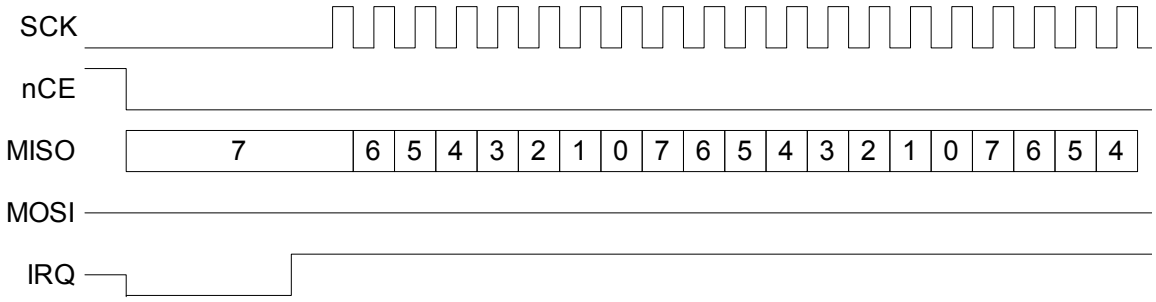


Figure 31. Flow Control at Beginning of a Raw Read Transfer

Figure 32 shows the operation of flow control in the middle of a write transfer. MISO or IRQ must be deasserted after the leading edge of SCK on the first bit of the byte (labelled 7) and before the falling edge of the 7th bit of the byte (labelled 1) in order to insure that SCK stops at the end of the byte.

©2017 Ambiq Micro, Inc.
All rights reserved.

Deasserting MISO or IRQ outside of that window can produce unpredictable results. SCK will resume at some point after the assertion of MISO or IRQ.

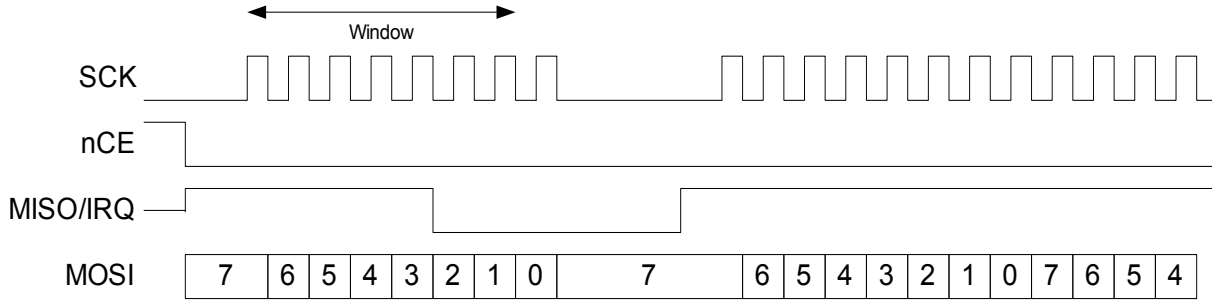


Figure 32. Flow Control in the Middle of a Write Transfer

Figure 33 shows the operation of flow control in the middle of a read transfer. IRQ must be deasserted after the leading edge of SCK on the first bit of the byte (labelled 7) and before the falling edge of the 7th bit of the byte (labelled 1) in order to insure that SCK stops at the end of the byte. Deasserting IRQ outside of that window can produce unpredictable results. SCK will resume at some point after the assertion of IRQ.

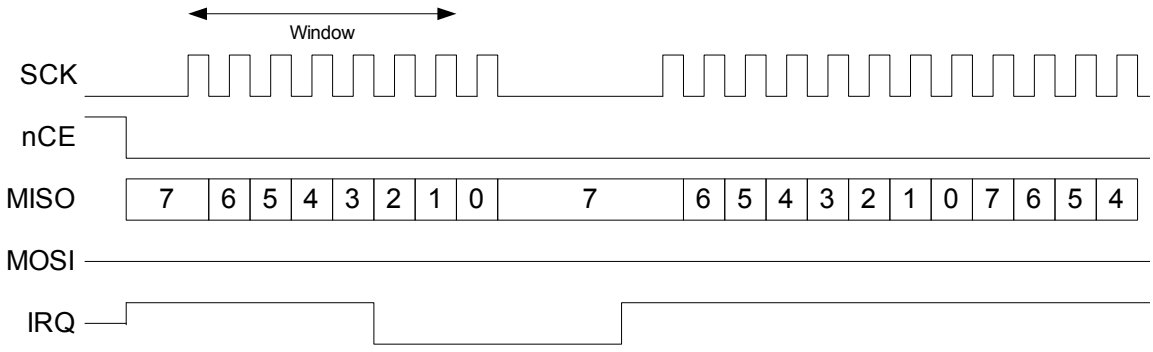


Figure 33. Flow Control in the Middle of a Read Transfer

5.11 Pre-read Control

The STARTRD field defines the number of bus clock cycles before the end of each byte where the IO read request occurs. For all I2C frequencies and SPI frequencies below 16 MHz, the STARTRD field should be set to 0 to minimize the potential of the IO transfer holding off a bus access to the FIFO. For SPI frequencies of 16 MHz or 24 MHz, the STARTRD field must be set to a value of 2 to insure enough time for the IO preread.

©2017 Ambiq Micro, Inc.
All rights reserved.

5.12 Minimizing Power

Each I^2C/SPI Master has a global interface enable bit REG_IOMSTRn_IOMCFG_IFCEN. This bit should be kept at 0 whenever the interface is not being used in order to minimize power consumption. The FIFO cannot be accessed if IFCEN is 0, although all of the other registers are accessible. When the module is not in use, the field should also be kept at 0 to minimize power. This is important even if IFCEN is a 0.

5.13 IOMSTR Registers

I2C/SPI Master

INSTANCE 0 BASE ADDRESS:0x50004000

INSTANCE 1 BASE ADDRESS:0x50005000

INSTANCE 2 BASE ADDRESS:0x50006000

INSTANCE 3 BASE ADDRESS:0x50007000

INSTANCE 4 BASE ADDRESS:0x50008000

INSTANCE 5 BASE ADDRESS:0x50009000

©2017 Ambiq Micro, Inc.
All rights reserved.

5.13.1 Register Memory Map

Table 213: IOMSTR Register Map

Address(s)	Register Name	Description
0x50004000 0x50005000 0x50006000 0x50007000 0x50008000 0x50009000	FIFO	FIFO Access Port
0x50004100 0x50005100 0x50006100 0x50007100 0x50008100 0x50009100	FIFOPTR	Current FIFO Pointers
0x50004104 0x50005104 0x50006104 0x50007104 0x50008104 0x50009104	TLNGTH	Transfer Length
0x50004108 0x50005108 0x50006108 0x50007108 0x50008108 0x50009108	FIFOTHR	FIFO Threshold Configuration
0x5000410C 0x5000510C 0x5000610C 0x5000710C 0x5000810C 0x5000910C	CLKCFG	I/O Clock Configuration
0x50004110 0x50005110 0x50006110 0x50007110 0x50008110 0x50009110	CMD	Command Register
0x50004114 0x50005114 0x50006114 0x50007114 0x50008114 0x50009114	CMDRPT	Command Repeat Register
0x50004118 0x50005118 0x50006118 0x50007118 0x50008118 0x50009118	STATUS	Status Register

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 213: IOMSTR Register Map

Address(s)	Register Name	Description
0x5000411C 0x5000511C 0x5000611C 0x5000711C 0x5000811C 0x5000911C	CFG	I/O Master Configuration
0x50004200 0x50005200 0x50006200 0x50007200 0x50008200 0x50009200	INTEN	IO Master Interrupts: Enable
0x50004204 0x50005204 0x50006204 0x50007204 0x50008204 0x50009204	INTSTAT	IO Master Interrupts: Status
0x50004208 0x50005208 0x50006208 0x50007208 0x50008208 0x50009208	INTCLR	IO Master Interrupts: Clear
0x5000420C 0x5000520C 0x5000620C 0x5000720C 0x5000820C 0x5000920C	INTSET	IO Master Interrupts: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

5.13.2 IOMSTR Registers

5.13.2.1 FIFO Register

FIFO Access Port

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x50004000

INSTANCE 1 ADDRESS: 0x50005000

INSTANCE 2 ADDRESS: 0x50006000

INSTANCE 3 ADDRESS: 0x50007000

INSTANCE 4 ADDRESS: 0x50008000

INSTANCE 5 ADDRESS: 0x50009000

FIFO Access Port

Table 214: FIFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO																															

Table 215: FIFO Register Bits

Bit	Name	Reset	RW	Description
31:0	FIFO	0x0	RW	FIFO access port.

5.13.2.2 FIFOPTR Register

Current FIFO Pointers

OFFSET: 0x00000100

INSTANCE 0 ADDRESS: 0x50004100

INSTANCE 1 ADDRESS: 0x50005100

INSTANCE 2 ADDRESS: 0x50006100

INSTANCE 3 ADDRESS: 0x50007100

INSTANCE 4 ADDRESS: 0x50008100

INSTANCE 5 ADDRESS: 0x50009100

Current FIFO Pointers

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 216: FIFOPTR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD								FIFOREM								RSVD								FIFOSIZ							

Table 217: FIFOPTR Register Bits

Bit	Name	Reset	RW	Description
31:24	RSVD	0x0	RO	RESERVED
23:16	FIFOREM	0x0	RO	The number of bytes remaining in the FIFO (i.e. 128-FIFOSIZ if FULLDUP = 0 or 64-FIFOSIZ if FULLDUP = 1)).
15:8	RSVD	0x0	RO	RESERVED
7:0	FIFOSIZ	0x0	RO	The number of bytes currently in the FIFO.

5.13.2.3 TLNGTH Register

Transfer Length

OFFSET: 0x00000104

INSTANCE 0 ADDRESS: 0x50004104

INSTANCE 1 ADDRESS: 0x50005104

INSTANCE 2 ADDRESS: 0x50006104

INSTANCE 3 ADDRESS: 0x50007104

INSTANCE 4 ADDRESS: 0x50008104

INSTANCE 5 ADDRESS: 0x50009104

Transfer Length

Table 218: TLNGTH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																				TLNGTH											

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 219: TLNGTH Register Bits

Bit	Name	Reset	RW	Description
31:12	RSVD	0x0	RO	RESERVED
11:0	TLNGTH	0x0	RO	Remaining transfer length.

5.13.2.4 FIFOTHR Register

FIFO Threshold Configuration

OFFSET: 0x00000108

INSTANCE 0 ADDRESS: 0x50004108

INSTANCE 1 ADDRESS: 0x50005108

INSTANCE 2 ADDRESS: 0x50006108

INSTANCE 3 ADDRESS: 0x50007108

INSTANCE 4 ADDRESS: 0x50008108

INSTANCE 5 ADDRESS: 0x50009108

FIFO Threshold Configuration

Table 220: FIFOTHR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																	FIFOWTHR							RSVD	FIFORTHR						

Table 221: FIFOTHR Register Bits

Bit	Name	Reset	RW	Description
31:15	RSVD	0x0	RO	RESERVED
14:8	FIFOWTHR	0x0	RW	FIFO write threshold.
7	RSVD	0x0	RO	RESERVED
6:0	FIFORTHR	0x0	RW	FIFO read threshold.

5.13.2.5 CLKCFG Register

I/O Clock Configuration

OFFSET: 0x0000010C

©2017 Ambiq Micro, Inc.
All rights reserved.

INSTANCE 0 ADDRESS: 0x5000410C

INSTANCE 1 ADDRESS: 0x5000510C

INSTANCE 2 ADDRESS: 0x5000610C

INSTANCE 3 ADDRESS: 0x5000710C

INSTANCE 4 ADDRESS: 0x5000810C

INSTANCE 5 ADDRESS: 0x5000910C

I/O Clock Configuration

Table 222: CLKCFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TOTPER								LOWPER								RSVD			DIVEN	DIV3	FSEL			RSVD							

Table 223: CLKCFG Register Bits

Bit	Name	Reset	RW	Description
31:24	TOTPER	0x0	RW	Clock total count minus 1.
23:16	LOWPER	0x0	RW	Clock low count minus 1.
15:13	RSVD	0x0	RO	RESERVED
12	DIVEN	0x0	RW	Enable clock division by TOTPER. DIS = 0x0 - Disable TOTPER division. EN = 0x1 - Enable TOTPER division.
11	DIV3	0x0	RW	Enable divide by 3. DIS = 0x0 - Select divide by 1. EN = 0x1 - Select divide by 3.
10:8	FSEL	0x0	RW	Select the input clock frequency. MIN_PWR = 0x0 - Selects the minimum power clock. This setting should be used whenever the IOMSTR is not active. HFRC = 0x1 - Selects the HFRC as the input clock. HFRC_DIV2 = 0x2 - Selects the HFRC / 2 as the input clock. HFRC_DIV4 = 0x3 - Selects the HFRC / 4 as the input clock. HFRC_DIV8 = 0x4 - Selects the HFRC / 8 as the input clock. HFRC_DIV16 = 0x5 - Selects the HFRC / 16 as the input clock. HFRC_DIV32 = 0x6 - Selects the HFRC / 32 as the input clock. HFRC_DIV64 = 0x7 - Selects the HFRC / 64 as the input clock.
7:0	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

5.13.2.6 CMD Register

Command Register

OFFSET: 0x00000110

INSTANCE 0 ADDRESS: 0x50004110

INSTANCE 1 ADDRESS: 0x50005110

INSTANCE 2 ADDRESS: 0x50006110

INSTANCE 3 ADDRESS: 0x50007110

INSTANCE 4 ADDRESS: 0x50008110

INSTANCE 5 ADDRESS: 0x50009110

Command Register

Table 224: CMD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMD																															

Table 225: CMD Register Bits

Bit	Name	Reset	RW	Description
31:0	CMD	0x0	RW	This register holds the I/O Command

5.13.2.7 CMDRPT Register

Command Repeat Register

OFFSET: 0x00000114

INSTANCE 0 ADDRESS: 0x50004114

INSTANCE 1 ADDRESS: 0x50005114

INSTANCE 2 ADDRESS: 0x50006114

INSTANCE 3 ADDRESS: 0x50007114

INSTANCE 4 ADDRESS: 0x50008114

INSTANCE 5 ADDRESS: 0x50009114

Command Repeat Register

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 226: CMDRPT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																											CMDRPT					

Table 227: CMDRPT Register Bits

Bit	Name	Reset	RW	Description
31:5	RSVD	0x0	RO	RESERVED
4:0	CMDRPT	0x0	RW	These bits hold the Command repeat count.

5.13.2.8 STATUS Register

Status Register

OFFSET: 0x00000118

INSTANCE 0 ADDRESS: 0x50004118

INSTANCE 1 ADDRESS: 0x50005118

INSTANCE 2 ADDRESS: 0x50006118

INSTANCE 3 ADDRESS: 0x50007118

INSTANCE 4 ADDRESS: 0x50008118

INSTANCE 5 ADDRESS: 0x50009118

Status Register

Table 228: STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													IDLEST	CMDACT	ERR

Table 229: STATUS Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 229: STATUS Register Bits

Bit	Name	Reset	RW	Description
2	IDLEST	0x0	RO	This bit indicates if the I/O state machine is IDLE. IDLE = 0x1 - The I/O state machine is in the idle state.
1	CMDACT	0x0	RO	This bit indicates if the I/O Command is active. ACTIVE = 0x1 - An I/O command is active.
0	ERR	0x0	RO	This bit indicates if an error interrupt has occurred. ERROR = 0x1 - An error has been indicated by the IOM.

5.13.2.9 CFG Register

I/O Master Configuration

OFFSET: 0x0000011C

INSTANCE 0 ADDRESS: 0x5000411C

INSTANCE 1 ADDRESS: 0x5000511C

INSTANCE 2 ADDRESS: 0x5000611C

INSTANCE 3 ADDRESS: 0x5000711C

INSTANCE 4 ADDRESS: 0x5000811C

INSTANCE 5 ADDRESS: 0x5000911C

I/O Master Configuration

Table 230: CFG Register

31	30:15	14	13	12	11	10	09	08	07:06	05:04	03	02	01	00
IFCEN	RSVD	RDFCPOL	WTFCPOL	WTFCIRQ	FCDEL	MOSIINV	RDFC	WTFC	RSVD	STARTRD	FULLDUP	SPHA	SPOL	IFCSEL

Table 231: CFG Register Bits

Bit	Name	Reset	RW	Description
31	IFCEN	0x0	RW	This bit enables the IO Master. DIS = 0x0 - Disable the IO Master. EN = 0x1 - Enable the IO Master.
30:15	RSVD	0x0	RO	RESERVED
14	RDFCPOL	0x0	RW	This bit selects the read flow control signal polarity. HIGH = 0x0 - Flow control signal high creates flow control. LOW = 0x1 - Flow control signal low creates flow control.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 231: CFG Register Bits

Bit	Name	Reset	RW	Description
13	WTFCPOL	0x1	RW	This bit selects the write flow control signal polarity. HIGH = 0x0 - Flow control signal high creates flow control. LOW = 0x1 - Flow control signal low creates flow control.
12	WTFCIRQ	0x0	RW	This bit selects the write mode flow control signal. MISO = 0x0 - MISO is used as the write mode flow control signal. IRQ = 0x1 - IRQ is used as the write mode flow control signal.
11	FCDEL	0x0	RW	This bit must be left at the default value of 0.
10	MOSIINV	0x0	RW	This bit invewrts MOSI when flow control is enabled. NORMAL = 0x0 - MOSI is set to 0 in read mode and 1 in write mode. INVERT = 0x1 - MOSI is set to 1 in read mode and 0 in write mode.
9	RDFC	0x0	RW	This bit enables read mode flow control. DIS = 0x0 - Read mode flow control disabled. EN = 0x1 - Read mode flow control enabled.
8	WTFC	0x0	RW	This bit enables write mode flow control. DIS = 0x0 - Write mode flow control disabled. EN = 0x1 - Write mode flow control enabled.
7:6	RSVD	0x0	RO	RESERVED
5:4	STARTRD	0x0	RW	This bit selects the preread timing. PRERD0 = 0x0 - 0 read delay cycles. PRERD1 = 0x1 - 1 read delay cycles. PRERD2 = 0x2 - 2 read delay cycles. PRERD3 = 0x3 - 3 read delay cycles.
3	FULLDUP	0x0	RW	This bit selects full duplex mode. NORMAL = 0x0 - 128 byte FIFO in half duplex mode. FULLDUP = 0x1 - 64 byte FIFO in full duplex mode.
2	SPHA	0x0	RW	This bit selects SPI phase. SAMPLE_LEADING_EDGE = 0x0 - Sample on the leading (first) clock edge. SAMPLE_TRAILING_EDGE = 0x1 - Sample on the trailing (second) clock edge.
1	SPOL	0x0	RW	This bit selects SPI polarity. CLK_BASE_0 = 0x0 - The base value of the clock is 0. CLK_BASE_1 = 0x1 - The base value of the clock is 1.
0	IFCSEL	0x0	RW	This bit selects the I/O interface. I2C = 0x0 - Selects I2C interface for the I/O Master. SPI = 0x1 - Selects SPI interface for the I/O Master.

5.13.2.10INTEN Register

IO Master Interrupts: Enable

OFFSET: 0x00000200

©2017 Ambiq Micro, Inc.
All rights reserved.

INSTANCE 0 ADDRESS: 0x50004200

INSTANCE 1 ADDRESS: 0x50005200

INSTANCE 2 ADDRESS: 0x50006200

INSTANCE 3 ADDRESS: 0x50007200

INSTANCE 4 ADDRESS: 0x50008200

INSTANCE 5 ADDRESS: 0x50009200

Set bits in this register to allow this module to generate the corresponding interrupt.

Table 232: INTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					ARB	STOP	START	ICMD	IACC	WTLEN	NAK	FOVFL	FUNDFL	THR	CMDCMP

Table 233: INTEN Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	RESERVED
10	ARB	0x0	RW	This is the arbitration loss interrupt. This error occurs if another master collides with an IO Master transfer. Generally, the IOM started an operation but found SDA already low.
9	STOP	0x0	RW	This is the STOP command interrupt. A STOP bit was detected by the IOM.
8	START	0x0	RW	This is the START command interrupt. A START from another master was detected. Software must wait for a STOP before proceeding.
7	ICMD	0x0	RW	This is the illegal command interrupt. Software attempted to issue a CMD while another CMD was already in progress. Or an attempt was made to issue a non-zero-length write CMD with an empty FIFO.
6	IACC	0x0	RW	This is the illegal FIFO access interrupt. An attempt was made to read the FIFO during a write CMD. Or an attempt was made to write the FIFO on a read CMD.
5	WTLEN	0x0	RW	This is the WTLEN interrupt.
4	NAK	0x0	RW	This is the I2C NAK interrupt. The expected ACK from the slave was not received by the IOM.
3	FOVFL	0x0	RW	This is the Write FIFO Overflow interrupt. An attempt was made to write the FIFO while it was full (i.e. while FIFOSIZ > 124).

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 233: INTEN Register Bits

Bit	Name	Reset	RW	Description
2	FUNDFL	0x0	RW	This is the Read FIFO Underflow interrupt. An attempt was made to read FIFO when empty (i.e. while FIFOSIZ < 4).
1	THR	0x0	RW	This is the FIFO Threshold interrupt.
0	CMDCMP	0x0	RW	This is the Command Complete interrupt.

5.13.2.11INTSTAT Register

IO Master Interrupts: Status

OFFSET: 0x00000204

INSTANCE 0 ADDRESS: 0x50004204

INSTANCE 1 ADDRESS: 0x50005204

INSTANCE 2 ADDRESS: 0x50006204

INSTANCE 3 ADDRESS: 0x50007204

INSTANCE 4 ADDRESS: 0x50008204

INSTANCE 5 ADDRESS: 0x50009204

Read bits from this register to discover the cause of a recent interrupt.

Table 234: INTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					ARB	STOP	START	ICMD	IACC	WTLEN	NAK	FOVFL	FUNDFL	THR	CMDCMP

Table 235: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	RESERVED
10	ARB	0x0	RW	This is the arbitration loss interrupt. This error occurs if another master collides with an IO Master transfer. Generally, the IOM started an operation but found SDA already low.
9	STOP	0x0	RW	This is the STOP command interrupt. A STOP bit was detected by the IOM.
8	START	0x0	RW	This is the START command interrupt. A START from another master was detected. Software must wait for a STOP before proceeding.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 235: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
7	ICMD	0x0	RW	This is the illegal command interrupt. Software attempted to issue a CMD while another CMD was already in progress. Or an attempt was made to issue a non-zero-length write CMD with an empty FIFO.
6	IACC	0x0	RW	This is the illegal FIFO access interrupt. An attempt was made to read the FIFO during a write CMD. Or an attempt was made to write the FIFO on a read CMD.
5	WTLEN	0x0	RW	This is the WTLEN interrupt.
4	NAK	0x0	RW	This is the I2C NAK interrupt. The expected ACK from the slave was not received by the IOM.
3	FOVFL	0x0	RW	This is the Write FIFO Overflow interrupt. An attempt was made to write the FIFO while it was full (i.e. while FIFOSIZ > 124).
2	FUNDFL	0x0	RW	This is the Read FIFO Underflow interrupt. An attempt was made to read FIFO when empty (i.e. while FIFOSIZ < 4).
1	THR	0x0	RW	This is the FIFO Threshold interrupt.
0	CMDCMP	0x0	RW	This is the Command Complete interrupt.

5.13.2.12INTCLR Register

IO Master Interrupts: Clear

OFFSET: 0x00000208

INSTANCE 0 ADDRESS: 0x50004208

INSTANCE 1 ADDRESS: 0x50005208

INSTANCE 2 ADDRESS: 0x50006208

INSTANCE 3 ADDRESS: 0x50007208

INSTANCE 4 ADDRESS: 0x50008208

INSTANCE 5 ADDRESS: 0x50009208

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 236: INTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					ARB	STOP	START	ICMD	IACC	WTLEN	NAK	FOVFL	FUNDFL	THR	CMDCMP

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 237: INTCLR Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	RESERVED
10	ARB	0x0	RW	This is the arbitration loss interrupt. This error occurs if another master collides with an IO Master transfer. Generally, the IOM started an operation but found SDA already low.
9	STOP	0x0	RW	This is the STOP command interrupt. A STOP bit was detected by the IOM.
8	START	0x0	RW	This is the START command interrupt. A START from another master was detected. Software must wait for a STOP before proceeding.
7	ICMD	0x0	RW	This is the illegal command interrupt. Software attempted to issue a CMD while another CMD was already in progress. Or an attempt was made to issue a non-zero-length write CMD with an empty FIFO.
6	IACC	0x0	RW	This is the illegal FIFO access interrupt. An attempt was made to read the FIFO during a write CMD. Or an attempt was made to write the FIFO on a read CMD.
5	WTLEN	0x0	RW	This is the WTLEN interrupt.
4	NAK	0x0	RW	This is the I2C NAK interrupt. The expected ACK from the slave was not received by the IOM.
3	FOVFL	0x0	RW	This is the Write FIFO Overflow interrupt. An attempt was made to write the FIFO while it was full (i.e. while FIFOSIZ > 124).
2	FUNDFL	0x0	RW	This is the Read FIFO Underflow interrupt. An attempt was made to read FIFO when empty (i.e. while FIFOSIZ < 4).
1	THR	0x0	RW	This is the FIFO Threshold interrupt.
0	CMDCMP	0x0	RW	This is the Command Complete interrupt.

5.13.2.13INTSET Register

IO Master Interrupts: Set

OFFSET: 0x0000020C

INSTANCE 0 ADDRESS: 0x5000420C

INSTANCE 1 ADDRESS: 0x5000520C

INSTANCE 2 ADDRESS: 0x5000620C

INSTANCE 3 ADDRESS: 0x5000720C

INSTANCE 4 ADDRESS: 0x5000820C

INSTANCE 5 ADDRESS: 0x5000920C

©2017 Ambiq Micro, Inc.
All rights reserved.

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 238: INTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					ARB	STOP	START	ICMD	IACC	WTLEN	NAK	FOVFL	FUNDFL	THR	CMDCMP

Table 239: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	RESERVED
10	ARB	0x0	RW	This is the arbitration loss interrupt. This error occurs if another master collides with an IO Master transfer. Generally, the IOM started an operation but found SDA already low.
9	STOP	0x0	RW	This is the STOP command interrupt. A STOP bit was detected by the IOM.
8	START	0x0	RW	This is the START command interrupt. A START from another master was detected. Software must wait for a STOP before proceeding.
7	ICMD	0x0	RW	This is the illegal command interrupt. Software attempted to issue a CMD while another CMD was already in progress. Or an attempt was made to issue a non-zero-length write CMD with an empty FIFO.
6	IACC	0x0	RW	This is the illegal FIFO access interrupt. An attempt was made to read the FIFO during a write CMD. Or an attempt was made to write the FIFO on a read CMD.
5	WTLEN	0x0	RW	This is the WTLEN interrupt.
4	NAK	0x0	RW	This is the I2C NAK interrupt. The expected ACK from the slave was not received by the IOM.
3	FOVFL	0x0	RW	This is the Write FIFO Overflow interrupt. An attempt was made to write the FIFO while it was full (i.e. while FIFOSIZ > 124).
2	FUNDFL	0x0	RW	This is the Read FIFO Underflow interrupt. An attempt was made to read FIFO when empty (i.e. while FIFOSIZ < 4).
1	THR	0x0	RW	This is the FIFO Threshold interrupt.
0	CMDCMP	0x0	RW	This is the Command Complete interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

©2017 Ambiq Micro, Inc.
All rights reserved.

6. I²C/SPI Slave Module

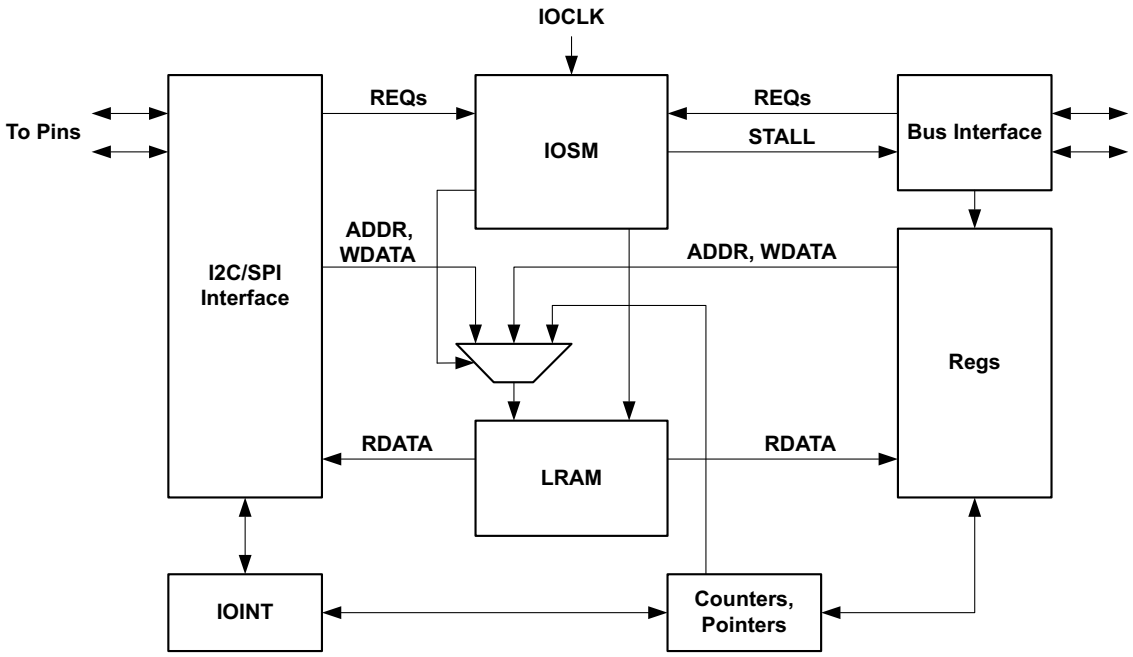


Figure 34. Block diagram for the I²C/SPI Slave Module

6.1 Functional Overview

The I²C/SPI Slave Module, shown in Figure 34, allows the Apollo2 Blue to function as a Slave in an I²C or SPI system. The I²C/SPI Slave operates in an independent fashion, so that the Apollo2 Blue may be placed in a sleep mode and still receive operations over the I/O interface. The Slave may be configured to generate an interrupt on specific references.

The I²C/SPI Slave contains 256 bytes of RAM which is only accessible when the module is enabled. This RAM may be flexibly configured into three spaces: a block directly accessible via the I/O interface, a block which functions as a FIFO for read operations on the interface, and a block of generally accessible RAM used to store parameters during deep sleep mode.

In I²C mode the Slave supports fully configurable 7 and 10-bit addressing with interface timing limits as specified in Table 781. In SPI mode, the Slave supports all polarity/phase combinations and interface frequencies as specified in Table 784.

6.2 Local RAM Allocation

The I²C/SPI Slave is built around a 256-byte local RAM (LRAM), through which all data flows between the CPU AHB and the IO interface. The I²C/SPI Slave supports a 128-byte offset space when accessed from the I/O interface.

The LRAM is divided into three separate areas on 8-byte boundaries. These areas are:

©2017 Ambiq Micro, Inc.
All rights reserved.

1. A Direct Area for direct communication between the host and the MCU, which is mapped between the AHB address space and the I/O address space. This area is from LRAM address 0x00 to the address calculated from the 5-bit FIFOBASE field in the FIFO configuration register (FIFOCFG), minus 1. This 5-bit field (REG_IOSLAVE_FIFOCFG_FIFOBASE) should contain a value that represents the start of the FIFO Area and, in so doing, defines the size of the Direct Area in 8-byte segments. Part of this area can be defined as IO Slave Read-only starting at any 8-byte segment defined by REG_IOSLAVE_FIFOCFG_ROBASE and extending through the end of the Direct Area at FIFOBASE*8-1.
2. A FIFO Area which is used to stream data from the Apollo2 MCU. This memory is directly addressed from the AHB, but accessed from the I/O Interface using a single I/O address 0x7F as a streaming port. The FIFO area is from the LRAM address calculated from the value in the FIFOBASE field, FIFOBASE*8, to the LRAM address calculated from the value in the FIFOMAX field of the FIFOCFG register, REG_IOSLAVE_FIFOCFG_FIFOMAX.The upper FIFO Area address is FIFOMAX*8-1. The maximum value for FIFOMAX is 0x20, which would result in an upper FIFO Area address of 0xFF.
3. A RAM Area which is accessible only from the AHB Slave. The RAM area is from the LRAM address calculated from the value in the FIFOMAX field of the FIFOCFG register, REG_IOSLAVE_FIFOCFG_FIFOMAX, to address 0xFF. Setting FIFOMAX to 0x20 would result in a RAM area of zero size.

The data in the LRAM is maintained in Deep Sleep Mode.

Figure 35 below shows the LRAM address mapping between the I/O interface and the AHB.

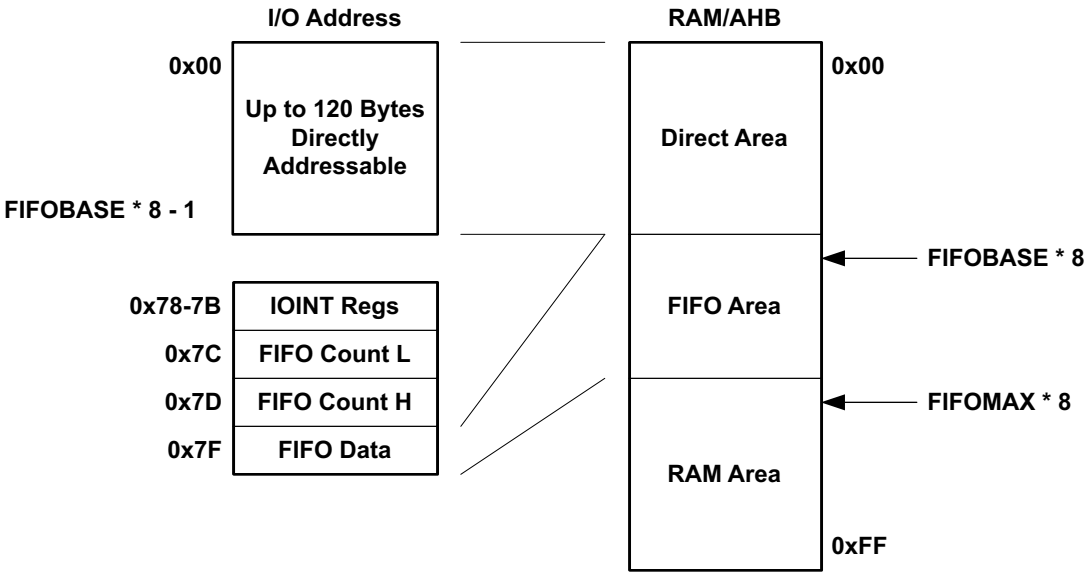


Figure 35. I²C/SPI Slave Module LRAM Addressing

6.3 Direct Area Functions

The Direct Area is used for direct communications between the interface Host and the Apollo2 Blue. The Host may write a register in this Register Access space, called REGACC, and read it back without

©2017 Ambiq Micro, Inc.
All rights reserved.

requiring the CPU to wake up, so that very low power interactions are supported. In some cases, however, accesses require interaction with the CPU.

REGACC interrupts are mapped in the Direct Area and operate as follows. Each REGACC interrupt status bit will be set whenever there is a read or write over the I2C or SPI interface in the Direct Area with an offset address which corresponds to a particular REGACC interrupt. Table 240 below lists the offsets to memory locations within the Direct Area and corresponding interrupt bit settings in the REGACCINTSTAT register.

I/O writes to locations 0x0-0xF will set a corresponding interrupt flag in the REGACCINTSTAT register. These locations are typically used for specific commands to the . Note that not all flags need generate an actual interrupt, so small multi-byte commands may be transmitted in this area. For example, a write to location 0x0 will set bit 31 of the REGACCINTSTAT register, a write to location 0x1 will set bit 30 of REGACCINTSTAT, and a write to location 0xF will set bit 16 of the REGACCINTSTAT register.

The upper 16 REGACC interrupts are each generated on an access to the last byte of a 32-bit word, starting at 0x10. I/O writes to locations 0x10 to 0x4F will set a corresponding interrupt flag in the REGACCINTSTAT register if the I/O address modulo 4 is 3 (i.e. addresses 0x13, 0x17, 0x1B, etc.). This allows larger transfers to be sent in a burst with a trigger being generated on the last write, and it also allows specifying a data buffer of any whole word size and have an interrupt generated on access to the last byte of the buffer. For example, a write to location 0x13 will set bit 15 of the REGACCINTSTAT register, a write to location 0x17 will set bit 14 of REGACCINTSTAT, and a write to location 0x4F will set bit 0 of the REGACCINTSTAT register.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 240: Mapping of Direct Area Access Interrupts and Corresponding REGACCINTSTAT Bits

REGACCINTSTAT Bit	Direct Area Offset Address
31	0x0
30	0x1
29	0x2
28	0x3
27	0x4
26	0x5
25	0x6
24	0x7
23	0x8
22	0x9
21	0xA
20	0xB
19	0xC
18	0xD
17	0xE
16	0xF
15	0x13
14	0x17
13	0x1B
12	0x1F
11	0x23
10	0x27
9	0x2B
8	0x2F
7	0x33
6	0x37
5	0x3B
4	0x3F
3	0x43
2	0x47
1	0x4B
0	0x4F

The REGACCINTSTAT register provides status of the 32 individual write interrupts. If an interrupt is enabled and set, it shows as a high bit in this register. The highest priority REGACC bit is bit 31 (set on access to address 0x00), and the lowest priority is bit 0 (set on access to address 0x4F). The 5-bit REG_IOSLAVE_PRENC register provides an encoded value of the highest priority of these interrupts to

©2017 Ambiq Micro, Inc.
All rights reserved.

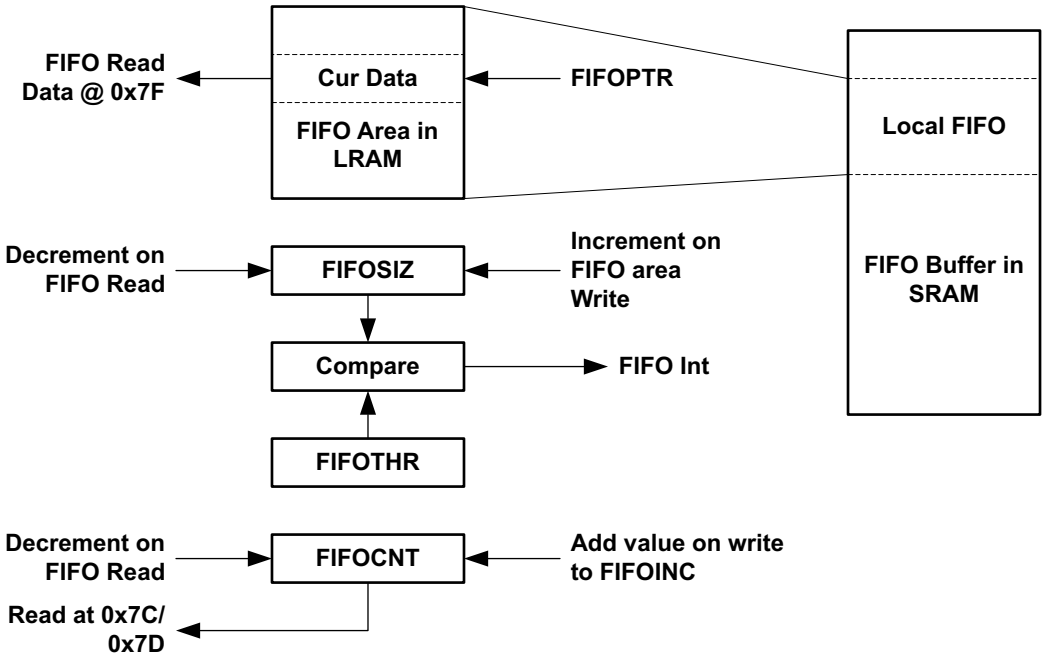
speed software decoding, and is therefore very useful for quickly servicing the highest priority REGACC interrupt (i.e. the one at the lowest offset address). The encoding works such that if interrupt 31 is set, PRENC will be 0. If interrupt 31 is not set and bit 30 is set, PRENC will be 1, and so on to the point where if bits 31-1 are not set and bit 0 is set PRENC will be 31. If no interrupts are set the value in PRENC is indeterminate.

The final special memory space within the Direct Area is a read-only area for the I/O Host, which is from I/O address (REG_IOSLAVE_FIFOCFG_ROBASE * 8) to (FIFOBASE * 8 – 1). I/O writes to this address space will not change the LRAM, which allows the space to be used for returning status to the I/O Host. ROBASE should have a minimum value of 0x0A, representing a start address of 0x50 to allow space for special commands and burst writes in lower Direct Area space.

6.4 FIFO Area Functions

The FIFO is used to provide very efficient flow of data from the Apollo2 Blue to the I/O Host processor with minimal CPU interaction. A FIFO of up to 1023 bytes can be easily maintained by software, with the oldest bytes residing in the LRAM FIFO Area and the newer data being held in system SRAM and transferred to the I^2C/SPI Slave on demand. Several hardware features support this operation.

Figure 36 shows the basic FIFO operation. The main FIFO is held in a buffer in SRAM, and the oldest data in that FIFO has been transferred to the FIFO Area of the I/O Slave. The REG_IOSLAVE_FIFOPTR_FIFOPTR register points to the next byte to be read on the I/O interface. REG_IOSLAVE_FIFOPTR_FIFOSIZ holds the current number of valid bytes in the FIFO on the I^2C/SPI Slave, and FIFOCTR holds the total number of bytes in the FIFO. The value in REG_IOSLAVE_FIFOCTR may be read indirectly at any time by the Host processor via the FIFOCTRUP_FIFOCTRLO registers to determine if there is FIFO data available (and how much is currently in the FIFO). I/O Host access to the FIFO counter is at offset 0x7C/D.



©2017 Ambiq Micro, Inc.
All rights reserved.

Figure 36. I2C/SPI Slave Module FIFO

When the host reads a byte from the FIFO, the data retrieved is pointed to by FIFOPTR, FIFOPTR is incremented and wraps around in the FIFO Area if it reaches FIFOMAX. FIFOSIZ and FIFOCTR are each decremented by one. The Host can read FIFOCTR and then read that many bytes without further checking. Note that this process can continue without requiring a CPU wakeup. If the Host attempts to read the FIFO when FIFOSIZ is 0, the FUNDFL interrupt flag is set in both the I2C Slave interrupt block and in the Host interrupt block.

When FIFOSIZ drops below the configured threshold REG_IOSLAVE_FIFOTHR the FSIZE interrupt flag is set and if enabled an interrupt is sent to the CPU which will wake it up. At that point, the CPU can move as much data from the SRAM FIFO to the I2C/SPI Slave FIFO as possible in a single operation and then go back to sleep. Since the FIFO Area can be quite large, CPU wake-ups will be very infrequent. If a write to the FIFOCTR which would increment the value beyond 1023 occurs, the FOVFL interrupt flag is set.

When some other process, such as a sensor read, produces new data for the FIFO, the CPU will add that data to the FIFO in SRAM, wrapping around as necessary. The REG_IOSLAVE_FIFOINC register is then written with the number of bytes added to the FIFO, which is added to the FIFOCTR register in an atomic fashion. In this way the Host processor can always determine how much read data is available.

The FIFO interface offset 0x7F is treated uniquely by the I2C/SPI Slave, in that an access to this address does not increment the Address Pointer. This allows the Host to initiate a burst read from address 0x7F of any length, and each read will supply the next byte in the FIFO.

6.5 Rearranging the FIFO

In normal operation the Host reads the oldest data from the FIFO, and the CPU writes new data onto the FIFO. In some cases it is desirable to modify this process, in particular for the FIFO to provide the newest data. The Apollo2 Blue supports such operation using a special control function.

If software desires to write the current sample to the front of the FIFO, it first checks the REG_IOSLAVE_FUPD_IOREAD status bit to ensure that there is not a Host read operation from the FIFO underway. Once IOREAD is clear, software sets the REG_IOSLAVE_FUPD_FIFOUPD bit, writes the new sample data to the front of the FIFO and modifies the FIFOPTR to point to the new data. At that point the FIFOUPD bit is cleared.

If the Host attempts a FIFO read operation while the FIFOUPD is set, a RDERR interrupt will be generated to the Host and the FRDERR interrupt flag will be set. The Host must either poll the RDERR interrupt bit at the end of each operation or configure a hardware interrupt. Note that if the software does not support alternate FIFO ordering, the Host does not have to check the RDERR function.

6.6 Interface Interrupts

The CPU may also signal the Host via the IOINT interrupt, which may be connected to an Apollo2 Blue pin and driven to the Host. Eight interrupts are available to be combined into the IOINT interrupt, and the Host can enable, read, clear and set these interrupts via the I/O interface. Software on the CPU can set 6 of the interrupts (SWINT0 through SWINT5) to communicate a variety of situations to the Host, and the other two interrupts indicate errors such as an attempt by the Host to read the FIFO when it is empty. A CPU interrupt is generated whenever the Host writes any IOINT registers (for example, to clear an interrupt) so the CPU can manage the interrupt interaction.The I2C/SPI Slave includes a mechanism to allow the Host CPU and the Apollo2 Blue to each interrupt the other via a set of eight interrupts. The Host CPU accesses these interrupts via interface locations 0x78-0x7B, and the Apollo2 Blue accesses these interrupts in the IOINTCTL Register.

The Host CPU may enable or disable any of the eight interrupts by writing the corresponding bit in the IOINTEN field of the IOINTCTL Register, which is accessed by the Host at interface location 0x78. The

©2017 Ambiq Micro, Inc.
All rights reserved.

Host CPU may then clear or set any of the interrupts by writing a 1 to the corresponding bit of the clear (at location 0x7A) or set (at location 0x7B) registers. The current state of all eight interrupts may be read in the IOINT field at location 0x79. Note that this structure is identical to the standard Apollo2 Blue interrupts in all modules. The Apollo2 Blue can read the value of the eight interrupt enables in the IOINTEN field of IOINTCTL, and can read the values of the eight interrupt status bits in the IOINT field of the IOINTCTL register. These two fields are read only. Table 241 summarizes these I/O interface interrupts and how they can be controlled and read.

Table 241: I/O Interface Interrupt Control

RAM Location	IOINT Register[1]	Function	MCU Register_Field	Description
0x78	IOINTEN	I/O Interrupt Enable	IOINTCTL_IOINTEN (R/O)	Each interrupt can be individually enabled by I/O Host, but can only be read by the MCU
0x79	IOINT	I/O Interrupt State	IOINTCTL_IOINT (R/O)	State of each interrupt, set or cleared, can be read by either the I/O Host or by the MCU
0x7A	IOINTCLR	I/O Interrupt Clear	IOINTCTL_IOINTCLR (W/O	Each interrupt can be individually cleared by the I/O Host, but the MCU can (only) clear all of them at once
0x7B	IOINTSET	I/O Interrupt Set	IOINTCTL_IOINTSET (W/O)	Each interrupt can be individually set by either the I/O Host or the MCU

1. Readable by the I/O Host

The Apollo2 Blue software may set any of the eight interrupt status register bits by writing a 1 to the corresponding bit of the IOINTSET field of the IOINTCTL Register, and may clear all of the interrupts by writing a 1 to the IOINTCLR bit of the IOINTCTL register. This allows the Apollo2 Blue to generate a software interrupt to the Host device. In addition, a FIFO underflow interrupt FUNDFL in the I2C/SPI Slave will set interrupt bit 7, and a FIFO read error interrupt FRDERR will set interrupt bit 6 of the IO interrupt status register IOINT. Note that the Apollo2 Blue software cannot write the IOINTEN register, so that IO interrupts are controlled completely by the Host processor.

If any of the IOINT interrupt bits are set and the corresponding bit in IOINTEN is set, an IOINT interrupt will be generated. If the GPIO configuration registers have configured PAD4 as IOINT, that interrupt will be driven directly onto PAD_IO[4]. This pin should be connected to an interrupt input pin of the Host interface device so that it can receive the interrupt and service it.

If the Host device writes to any of the interrupt register access locations (any location in 0x78-0x7B) the IOINTW interrupt will be set in the I2C/SPI INTSTAT Register. This allows Apollo2 Blue software to receive a software interrupt from the Host device. Note that this interrupt will occur for all writes by the Host, including a write to clear an interrupt.

6.7 Command Completion Interrupts

Four interrupts in the I2C/SPI Slave module are generated when the Host interface device completes a transfer. This allows Apollo2 Blue to be easily awakened for any transfer from the Host while maximizing the time Apollo2 Blue is in sleep mode. The XCMPWR interrupt is generated at the completion of a Host write transfer which includes addresses in the currently configured Direct Register space, and the XCMPRR interrupt is generated on the completion of a Host read transfer to that space. The XCMPWF interrupt is generated at the completion of a Host write transfer which includes the FIFO address 0x7F (although that is an invalid access), and the XCMPRF interrupt is generated at the completion of a Host read transfer which includes the FIFO address 0x7F.

©2017 Ambiq Micro, Inc.
All rights reserved.

NOTE: A write to 0x7F, which is the FIFO address, uses the address 0xFF, since this includes the R/W bit in the upper (first) bit followed by the 7-bit Direct Register address (offset). The prescribed usage of IOS FIFO is only for READ from the host, and hence writing to the FIFO is generally an invalid operation. So, even though XCMPWF flag/interrupt is defined, it is likely never going to be used.

NOTE: A burst transfer which begins in the Direct Register address space and is long enough to cause the Address Pointer to be 0x7F can set both the Direct Register and FIFO interrupts, although that would in general be an invalid operation.

6.8 Host Address Space and Registers

The Host of the I/O interface can access 128 bytes in the I^{2}C/SPI Slave in either I^{2}C or SPI mode. Offsets 0x00 to 0x77 may be directly mapped to the Direct RAM Area. The remaining eight offset locations access hardware functions within the I^{2}C/SPI Slave. The R/W indicator is referring to accesses from the Host.

6.9 I^{2}C Interface

The Apollo2 Blue I^{2}C Slave interface operates as a standard slave. The device is accessed at an address configured in the REG_IOSLAVE_IOSCFG_I2CADDR field, and supports Fast Mode Plus (up to 1 MHz). Both 7-bit and 10-bit address modes are supported, as selected by REG_IOSLAVE_IOSCFG_10BIT. The I^{2}C interface consists of two lines: one bi-directional data line (SDA) and one clock line (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor. By definition, a device that sends a message is called the “transmitter”, and the device that accepts the message is called the “receiver”. The device that controls the message transfer by driving SCL is called “master”. The devices that are controlled by the master are called “slaves”. The Apollo2 Blue I^{2}C Slave is always a slave device.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

A number of bus conditions have been defined (see Figure 37) and are described in the following sections.

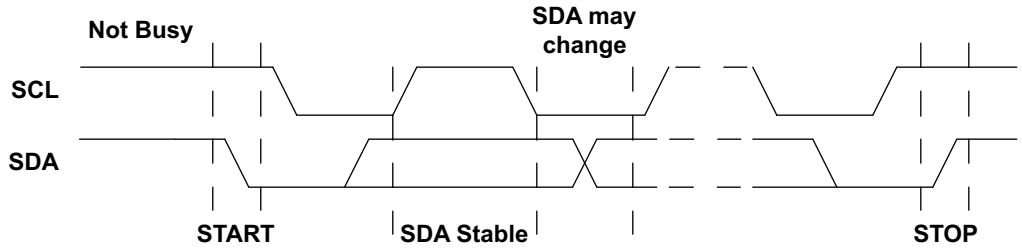


Figure 37. Basic I^{2}C Conditions

6.9.1 Bus Not Busy

Both SDA and SCL remain high.

©2017 Ambiq Micro, Inc.
All rights reserved.

6.9.2 Start Data Transfer

A change in the state of SDA from high to low, while SCL is high, defines the START condition. A START condition which occurs after a previous START but before a STOP is called a RESTART condition, and functions exactly like a normal STOP followed by a normal START.

6.9.3 Stop Data Transfer

A change in the state of SDA from low to high, while SCL is high, defines the STOP condition.

6.9.4 Data Valid

After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

6.9.5 Acknowledge

Each byte of eight bits is followed by one Acknowledge (ACK) bit as shown in Figure 38. This Acknowledge bit is a low level driven onto SDA by the receiver, whereas the master generates an extra ACK related SCL pulse. A slave receiver which is addressed is obliged to generate an Acknowledge after the reception of each byte. Also, on a read transfer a master receiver must generate an Acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the Acknowledge related SCL pulse. A master receiver must signal an end-of-data to the slave transmitter by not generating an Acknowledge (a NAK) on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

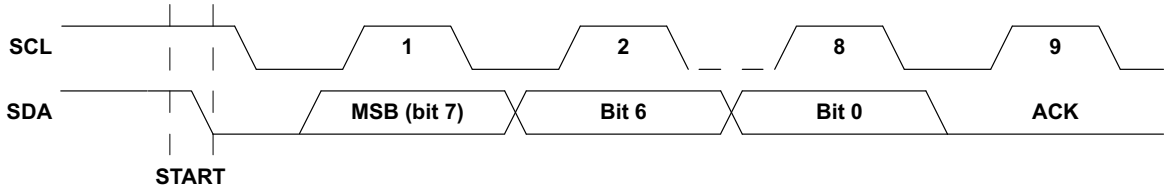
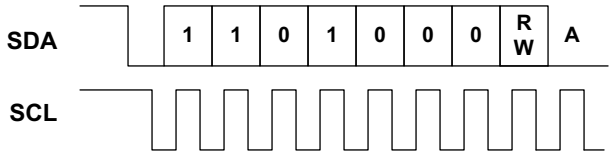


Figure 38. I2C Acknowledge

6.9.6 Address Operation

In I2C mode, the I2C/SPI Slave supports either 7-bit or 10-bit addressing, selected by the 10BIT bit in the IOSCFG Register. Figure 39 shows the operation in 7-bit mode in which the master addresses the Apollo2 Blue with a 7-bit address configured as 0xD2 in the I2CADDR field. After the START condition, the 7-bit address is transmitted MSB first. If this address matches the lower 7 bits of the I2CADDR field, the Apollo2 Blue is selected, the eighth bit indicate a write (RW = 0) or a read (RW = 1) operation and the Apollo2 Blue supplies the ACK. The Apollo2 Blue ignores all other address values and does not respond with an ACK.



©2017 Ambiq Micro, Inc.
All rights reserved.

Figure 39. I2C 7-bit Address Operation

Figure 40 shows the operation with which the master addresses the Apollo2 Blue with a 10-bit address configured at 0x536. After the START condition, the 10-bit preamble 0b11110 is transmitted first, followed by the first two address bits and the eighth bit indicating a write (RW = 0) or a read (RW = 1) operation. If the upper two bits match the I2CADDR value, the I2C/SPI Slave supplies the ACK. The next transfer includes the lower 8 bits of the address, and if these bits also match I2CADDR the Apollo2 Blue again supplies the ACK. The I2C/SPI Slave ignores all other address values and does not respond with an ACK.

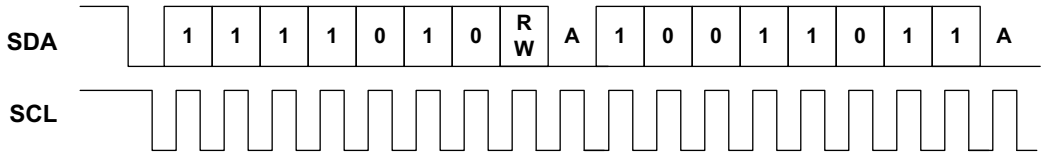


Figure 40. I2C 10-bit Address Operation

6.9.7 Offset Address Transmission

If the RW bit of the Address Operation indicates a write, the next byte transmitted from the master is the Offset Address as shown in Figure 41. This value is loaded into the Address Pointer of the I2C/SPI Slave.

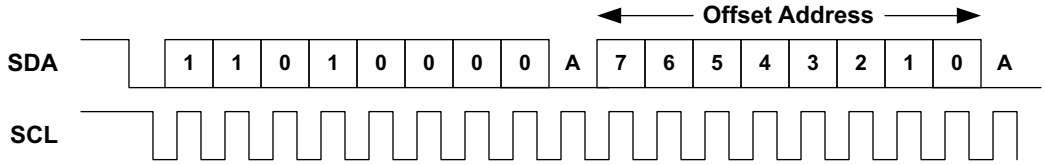


Figure 41. I2C Offset Address Transmission

6.9.8 Write Operation

In a write operation the master transmitter transmits to the Apollo2 Blue slave receiver. The Address Operation has a RW value of 0, and the second byte contains the Offset Address as in Figure 41. The next byte is written to the register selected by the Address Pointer (which was loaded with the Offset Address) and the Address Pointer is incremented. Subsequent transfers write bytes into successive registers until a STOP condition is received, as shown in Figure 42. Note that if the Address Pointer is at 0x7F, it will not increment on the write.

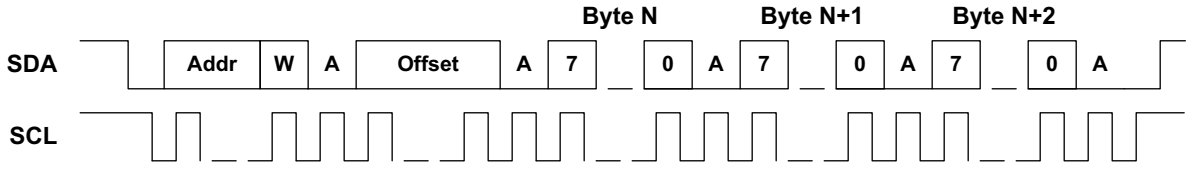


Figure 42. I2C Write Operation

©2017 Ambiq Micro, Inc.
All rights reserved.

6.9.9 Read Operation

In a read operation, the master first executes an Offset Address Transmission to load the Address Pointer with the desired Offset Address. A subsequent operation will again issue the address of the Apollo2 Blue but with the RW bit as a 1 indicating a read operation. Figure 43 shows this transaction beginning with a RESTART condition, although a STOP followed by a START may also be used. After the address operation, the slave becomes the transmitter and sends the register value from the location pointed to by the Address Pointer, and the Address Pointer is incremented. Subsequent transactions produce successive register values, until the master receiver responds with a NAK and a STOP to complete the operation. Because the Address Pointer holds a valid register address, the master may initiate another read sequence at this point without performing another Offset Address operation. Note that if the Address Pointer is at 0x7F, it will not increment on the read.

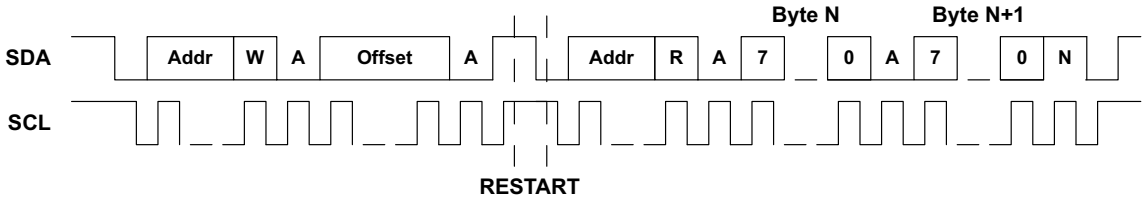


Figure 43. I2C Read Operation

6.9.10 General Address Detection

The I2C/SPI Slave may be configured to detect an I2C General Address (0x00) write. If this address is detected, the first data byte written is stored in the REG_IOSLAVE_GADATA Register and the GENAD interrupt flag is set. This allows software to create the appropriate response, which is typically to reset the I2C/SPI Slave.

6.10 SPI Interface

The I2C/SPI Slave includes a standard 3-wire or 4-wire SPI interface. The serial peripheral interface (SPI) bus is intended for synchronous communication between different ICs. 4-wire SPI consists of four signal lines: serial data input (MOSI), serial data output (MISO), serial clock (SCL) and an active low chip enable (nCE). The I2C/SPI Slave may be connected to a master with a 3-wire SPI interface by configuring 3-wire mode in the pin configuration block of the GPIO module, which will tie MOSI and MISO together. By definition, a device that sends a message is called the “transmitter”, and the device that accepts the message is called the “receiver”. The device that controls the message transfer by driving SCL is called “master”. The devices that are controlled by the master are called “slaves”. The I2C/SPI Slave SPI Slave is always a slave device.

The nCE input is used to initiate and terminate a data transfer. The SCL input is used to synchronize data transfer between the master and the slave devices via the MOSI (master to slave) and MISO (slave to master) lines. The SCL input, which is generated by the master, is active only during address and data transfer to any device on the SPI bus.

The I2C/SPI Slave supports clock frequencies up to 12 MHz, and responds to all SPI configurations of CPOL and CPHA using the SPOL configuration bit. There is one clock for each bit transferred. Address and data bits are transferred in groups of eight bits.

©2017 Ambiq Micro, Inc.
All rights reserved.

6.10.1 Write Operation

Figure 44 shows a SPI write operation. The operation is initiated when the nCE signal to the Apollo2 Blue goes low. At that point an 8-bit Address byte is transmitted from the master on the MOSI line, with the upper RW bit indicating read (if 0) or write (if 1). In this example the RW bit is a one selecting a write operation, and the lower 7 bits of the Address byte contain the Offset Address, which is loaded into the Address Pointer of the I2C/SPI Slave.

Each subsequent byte is loaded into the register selected by the Address Pointer, and the Address Pointer is incremented. The operation is terminated by the master by bringing the nCE signal high. Note that the MISO line is not used in a write operation and is held in the high impedance state by the I2C/SPI Slave. Note also that if the Address Pointer is 0x7F, it does not increment on the read.

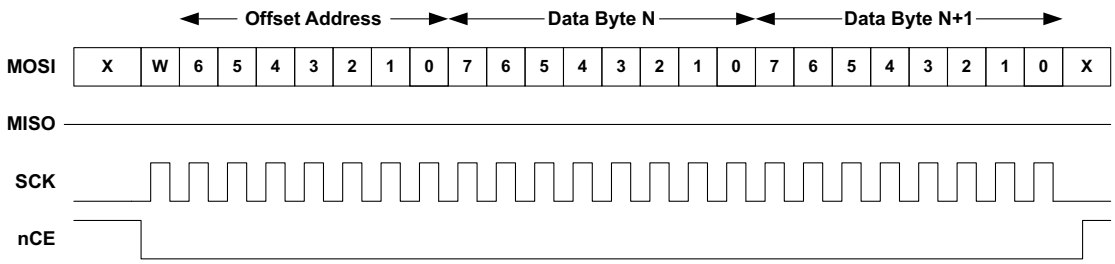


Figure 44. SPI Write Operation

6.10.2 Read Operation

Figure 45 shows a read operation. The address is transferred from the master to the slave just as it is in a write operation, but in this case the RW bit is a 0 indicating a read. After the transfer of the last address bit (bit 0), the I2C/SPI Slave begins driving data from the register selected by the Address Pointer onto the MISO line, bit 7 first, and the Address Pointer is incremented. The transfer continues until the master brings the nCE line high. Note that if the Address Pointer is 0x7F, it does not increment on the read.

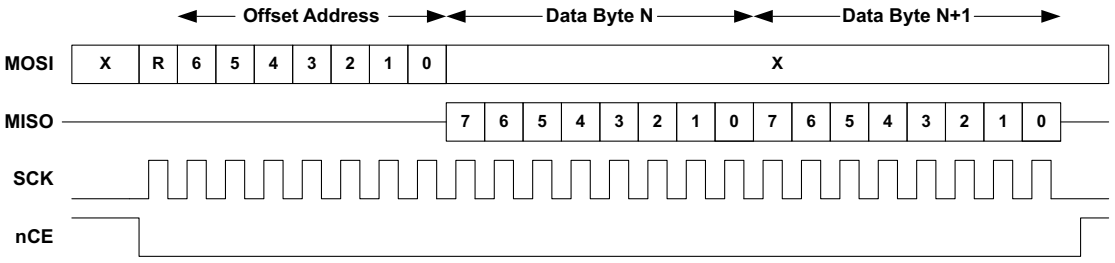


Figure 45. SPI Read Operation

6.10.3 Configuring 3-wire vs. 4-wire SPI Mode

The I2C/SPI Slave can operate in either 4-wire SPI mode, where the MISO and MOSI signals are on separate wires, or in 3-wire SPI mode where MISO and MOSI share a wire. This configuration is performed in the Pin Configuration module, and no configuration is necessary in the I2C/SPI Slave itself.

©2017 Ambiq Micro, Inc.
All rights reserved.

6.10.4 SPI Polarity and Phase

The I2C/SPI Slave supports all combinations of CPOL (clock polarity) and CPHA (data phase) in SPI mode. Figure 46 shows how these two bits affect the interface signal behavior.

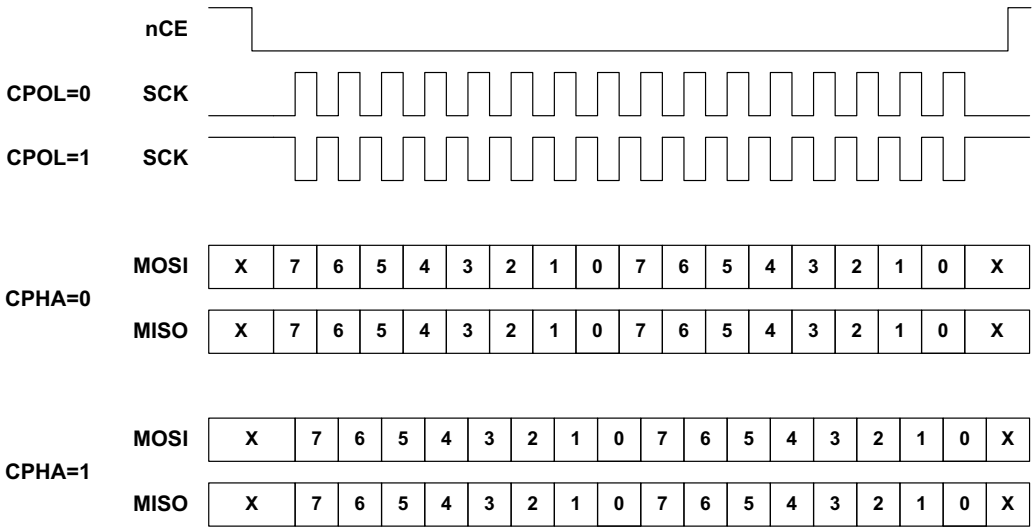


Figure 46. SPI CPOL and CPHA

If CPOL is 0, the clock SCK is normally low and positive pulses are generated during transfers. If CPOL is 1, SCK is normally high and negative pulses are generated during transfers.

If CPHA is 0, the data on the MOSI and MISO lines is sampled on the edge corresponding to the first SCK edge after nCE goes low (i.e. the rising edge if CPOL is 0 and the falling edge if CPOL is 1). Data on MISO and MOSI is driven on the opposite edge of SCK.

If CPHA is 1, the data on the MOSI and MISO lines is sampled on the edge corresponding to the second SCK edge after nCE goes low (i.e. the falling edge if CPOL is 0 and the rising edge if CPOL is 1). Data on MISO and MOSI is driven on the opposite edge of SCK.

The I2C/SPI Slave has only a single SPOL bit to control the polarity. If CPOL = CPHA, REG_IOSLAVE_IOSCFG_SPOL must be set to 0. If CPOL ≠ CPHA, SPOL must be set to 1.

6.11 Bit Orientation

In both I2C and SPI modes, the I2C/SPI Slave supports data transmission either LSB first or MSB first as configured by the REG_IOSLAVE_IOSCFG_LSB bit. If LSB is 0, data is transmitted and received MSB first. If LSB is 1, data is transmitted and received LSB first.

6.12 Wakeup Using the I2C/SPI Slave

The I2C/SPI Slave can continue to operate even if the Apollo2 Blue CPU is in Sleep or Deep Sleep mode. The hardware will enable and disable the I2C/SPI Slave clock and oscillators as necessary. The only consideration in this environment is when the MCU is in a deep sleep mode, such that the HFRC Oscillator is powered down, and a master attempts to access the I2C/SPI Slave. In this case the HFRC Oscillator must be powered up before any is transferred to or from the internal RAM. This process takes roughly 5-10 us, and is initiated by nCE going low in SPI mode or by the detection of a START in I2C mode.

©2017 Ambiq Micro, Inc.
All rights reserved.

For I^2C applications, the time delay is typically not relevant. At the fastest system clock of 1 MHz, the master must transfer 9 bits of address plus 9 bits of offset before any FIFO access can occur, and that is a minimum of 18 us. The clocks will have started prior to that point in every case.

For SPI applications with fast interface clocks (faster than 1 MHz), the master must be programmed to pull nCE low at least 10 us prior to sending the first clock. If a master is unable to control the timing of nCE in this way, then a GPIO interrupt can be configured to wake the Apollo2 Blue prior to initiating any SPI transfers.

There is no delay restriction if the MCU is in normal Sleep mode. In that case the HFRC is not powered down and the I^2C/SPI Slave clock will start immediately when nCE goes low. Alternatively, the FRCHFRC bit may be set in the FRCHFRC Register in the CLK_GEN module. If this bit is set, the HFRC will continue to be active even if the Apollo2 Blue CPU is in deep sleep mode, so that the I2C/SPI Slave can immediately begin transferring data independent of the SPI transfer rate. This will result in higher power because the HFRC remains active, so the FRCHFRC bit should only be set if it is known that a transfer is likely to begin prior to another interrupt.

6.13 IOSLAVE Registers

I2C/SPI Slave

INSTANCE 0 BASE ADDRESS:0x50000000

©2017 Ambiq Micro, Inc.
All rights reserved.

6.13.1 Register Memory Map

Table 242: IOSLAVE Register Map

Address(s)	Register Name	Description
0x50000100	FIFOPTR	Current FIFO Pointer
0x50000104	FIFOCFG	FIFO Configuration
0x50000108	FIFOTHR	FIFO Threshold Configuration
0x5000010C	FUPD	FIFO Update Status
0x50000110	FIFOCTR	Overall FIFO Counter
0x50000114	FIFOINC	Overall FIFO Counter Increment
0x50000118	CFG	I/O Slave Configuration
0x5000011C	PRENC	I/O Slave Interrupt Priority Encode
0x50000120	IOINTCTL	I/O Interrupt Control
0x50000124	GENADD	General Address Data
0x50000200	INTEN	IO Slave Interrupts: Enable
0x50000204	INTSTAT	IO Slave Interrupts: Status
0x50000208	INTCLR	IO Slave Interrupts: Clear
0x5000020C	INTSET	IO Slave Interrupts: Set
0x50000210	REGACCINTEN	Register Access Interrupts: Enable
0x50000214	REGACCINTSTAT	Register Access Interrupts: Status
0x50000218	REGACCINTCLR	Register Access Interrupts: Clear
0x5000021C	REGACCINTSET	Register Access Interrupts: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

6.13.2 IOSLAVE Registers

6.13.2.1 FIFOPTR Register

Current FIFO Pointer

OFFSET: 0x00000100

INSTANCE 0 ADDRESS: 0x50000100

Current FIFO Pointer

Table 243: FIFOPTR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																FIFOSIZ								FIFOPTR							

Table 244: FIFOPTR Register Bits

Bit	Name	Reset	RW	Description
31:16	RSVD	0x0	RO	RESERVED
15:8	FIFOSIZ	0x0	RW	The number of bytes currently in the hardware FIFO.
7:0	FIFOPTR	0x0	RW	Current FIFO pointer.

6.13.2.2 FIFOCFG Register

FIFO Configuration

OFFSET: 0x00000104

INSTANCE 0 ADDRESS: 0x50000104

FIFO Configuration

Table 245: FIFOCFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		ROBASE						RSVD								RSVD		FIFOMAX						RSVD				FIFOBASE			

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 246: FIFOCFG Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:24	ROBASE	0x20	RW	Defines the read-only area. The IO Slave read-only area is situated in LRAM at (ROBASE*8) to (FIFOOBASE*8-1)
23:16	RSVD	0x0	RO	RESERVED
15:14	RSVD	0x0	RO	RESERVED
13:8	FIFOMAX	0x0	RW	These bits hold the maximum FIFO address in 8 byte segments. It is also the beginning of the RAM area of the LRAM. Note that no RAM area is configured if FIFOMAX is set to 0x1F.
7:5	RSVD	0x0	RO	RESERVED
4:0	FIFOBASE	0x0	RW	These bits hold the base address of the I/O FIFO in 8 byte segments.The IO Slave FIFO is situated in LRAM at (FIFOBASE*8) to (FIFOMAX*8-1).

6.13.2.3 FIFOTHR Register

FIFO Threshold Configuration

OFFSET: 0x00000108

INSTANCE 0 ADDRESS: 0x50000108

FIFO Threshold Configuration

Table 247: FIFOTHR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								FIFOTHR							

Table 248: FIFOTHR Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	RESERVED
7:0	FIFOTHR	0x0	RW	FIFO size interrupt threshold.

©2017 Ambiq Micro, Inc.
All rights reserved.

6.13.2.4 FUPD Register

FIFO Update Status

OFFSET: 0x0000010C

INSTANCE 0 ADDRESS: 0x5000010C

FIFO Update Status

Table 249: FUPD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														IOREAD	FIFOUPD

Table 250: FUPD Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	RESERVED
1	IOREAD	0x0	RO	This bitfield indicates an IO read is active.
0	FIFOUPD	0x0	RW	This bit indicates that a FIFO update is underway.

6.13.2.5 FIFOCTR Register

Overall FIFO Counter

OFFSET: 0x00000110

INSTANCE 0 ADDRESS: 0x50000110

Overall FIFO Counter

Table 251: FIFOCTR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																						FIFOCTR									

Table 252: FIFOCTR Register Bits

Bit	Name	Reset	RW	Description
31:10	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 252: FIFOCTR Register Bits

Bit	Name	Reset	RW	Description
9:0	FIFOCTR	0x0	RW	Virtual FIFO byte count

6.13.2.6 FIFOINC Register

Overall FIFO Counter Increment

OFFSET: 0x00000114

INSTANCE 0 ADDRESS: 0x50000114

Overall FIFO Counter Increment

Table 253: FIFOINC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																						FIFOINC									

Table 254: FIFOINC Register Bits

Bit	Name	Reset	RW	Description
31:10	RSVD	0x0	RO	RESERVED
9:0	FIFOINC	0x0	WO	Increment the Overall FIFO Counter by this value on a write

6.13.2.7 CFG Register

I/O Slave Configuration

OFFSET: 0x00000118

INSTANCE 0 ADDRESS: 0x50000118

I/O Slave Configuration

Table 255: CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IFCEN	RSVD											I2CADDR												RSVD			STARTRD	RSVD	LSB	SPOL	IFCSEL

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 256: CFG Register Bits

Bit	Name	Reset	RW	Description
31	IFCEN	0x0	RW	IOSLAVE interface enable. DIS = 0x0 - Disable the IOSLAVE EN = 0x1 - Enable the IOSLAVE
30:20	RSVD	0x0	RO	RESERVED
19:8	I2CADDR	0x0	RW	7-bit or 10-bit I2C device address. Bit 19 Selects 7-bit/10-bit address: 7BIT = 0x0, 10BIT = 0x1 Bit 18:16 Upper 3 bits for 10-bit address; not used for 7-bit address Bit 15:9 7-bit address or lower 7 bits of 10-bit address Bit 8 Not used for either address mode
7:5	RSVD	0x0	RO	RESERVED
4	STARTRD	0x0	RW	This bit holds the cycle to initiate an I/O RAM read. LATE = 0x0 - Initiate I/O RAM read late in each transferred byte. EARLY = 0x1 - Initiate I/O RAM read early in each transferred byte.
3	RSVD	0x0	RO	RESERVED
2	LSB	0x0	RW	This bit selects the transfer bit ordering. MSB_FIRST = 0x0 - Data is assumed to be sent and received with MSB first. LSB_FIRST = 0x1 - Data is assumed to be sent and received with LSB first.
1	SPOL	0x0	RW	This bit selects SPI polarity. SPI_MODES_0_3 = 0x0 - Polarity 0, handles SPI modes 0 and 3. SPI_MODES_1_2 = 0x1 - Polarity 1, handles SPI modes 1 and 2.
0	IFCSEL	0x0	RW	This bit selects the I/O interface. I2C = 0x0 - Selects I2C interface for the IO Slave. SPI = 0x1 - Selects SPI interface for the IO Slave.

6.13.2.8 PRENC Register

I/O Slave Interrupt Priority Encode

OFFSET: 0x0000011C

INSTANCE 0 ADDRESS: 0x5000011C

I/O Slave Interrupt Priority Encode

Table 257: PRENC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																											PRENC				

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 258: PRENC Register Bits

Bit	Name	Reset	RW	Description
31:5	RSVD	0x0	RO	RESERVED
4:0	PRENC	0x0	RO	These bits hold the priority encode of the REGACC interrupts.

6.13.2.9 IOINTCTL Register

I/O Interrupt Control

OFFSET: 0x00000120

INSTANCE 0 ADDRESS: 0x50000120

I/O Interrupt Control

Table 259: IOINTCTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IOINTSET								RSVD							IOINTCLR	IOINT								IOINTEN							

Table 260: IOINTCTL Register Bits

Bit	Name	Reset	RW	Description
31:24	IOINTSET	0x0	WO	These bits set the IOINT interrupts when written with a 1.
23:17	RSVD	0x0	RO	RESERVED
16	IOINTCLR	0x0	WO	This bit clears all of the IOINT interrupts when written with a 1.
15:8	IOINT	0x0	RO	These bits read the IOINT interrupts.
7:0	IOINTEN	0x0	RO	These read-only bits indicate whether the IOINT interrupts are enabled.

6.13.2.10GENADD Register

General Address Data

OFFSET: 0x00000124

INSTANCE 0 ADDRESS: 0x50000124

General Address Data

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 261: GENADD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								GADATA							

Table 262: GENADD Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	RESERVED
7:0	GADATA	0x0	RO	The data supplied on the last General Address reference.

6.13.2.11INTEN Register

IO Slave Interrupts: Enable

OFFSET: 0x00000200

INSTANCE 0 ADDRESS: 0x50000200

Set bits in this register to allow this module to generate the corresponding interrupt.

Table 263: INTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																						XCMPWR	XCMPWF	XCMPRR	XCMPRF	IOINTW	GENAD	FRDERR	FUNDFL	FOVFL	FSIZE

Table 264: INTEN Register Bits

Bit	Name	Reset	RW	Description
31:10	RSVD	0x0	RO	RESERVED
9	XCMPWR	0x0	RW	Transfer complete interrupt, write to register space.
8	XCMPWF	0x0	RW	Transfer complete interrupt, write to FIFO space.
7	XCMPRR	0x0	RW	Transfer complete interrupt, read from register space.
6	XCMPRF	0x0	RW	Transfer complete interrupt, read from FIFO space.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 264: INTEN Register Bits

Bit	Name	Reset	RW	Description
5	IOINTW	0x0	RW	I2C Interrupt Write interrupt.
4	GENAD	0x0	RW	I2C General Address interrupt.
3	FRDERR	0x0	RW	FIFO Read Error interrupt.
2	FUNDFL	0x0	RW	FIFO Underflow interrupt.
1	FOVFL	0x0	RW	FIFO Overflow interrupt.
0	FSIZE	0x0	RW	FIFO Size interrupt.

6.13.2.12INTSTAT Register

IO Slave Interrupts: Status

OFFSET: 0x00000204

INSTANCE 0 ADDRESS: 0x50000204

Read bits from this register to discover the cause of a recent interrupt.

Table 265: INTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																						XCMPWR	XCMPWF	XCMPRR	XCMPRF	IOINTW	GENAD	FRDERR	FUNDFL	FOVFL	FSIZE

Table 266: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:10	RSVD	0x0	RO	RESERVED
9	XCMPWR	0x0	RW	Transfer complete interrupt, write to register space.
8	XCMPWF	0x0	RW	Transfer complete interrupt, write to FIFO space.
7	XCMPRR	0x0	RW	Transfer complete interrupt, read from register space.
6	XCMPRF	0x0	RW	Transfer complete interrupt, read from FIFO space.
5	IOINTW	0x0	RW	I2C Interrupt Write interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 266: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
4	GENAD	0x0	RW	I2C General Address interrupt.
3	FRDERR	0x0	RW	FIFO Read Error interrupt.
2	FUNDFL	0x0	RW	FIFO Underflow interrupt.
1	FOVFL	0x0	RW	FIFO Overflow interrupt.
0	FSIZE	0x0	RW	FIFO Size interrupt.

6.13.2.13INTCLR Register

IO Slave Interrupts: Clear

OFFSET: 0x00000208

INSTANCE 0 ADDRESS: 0x50000208

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 267: INTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																						XCMPWR	XCMPWF	XCMPRR	XCMPRF	IOINTW	GENAD	FRDERR	FUNDFL	FOVFL	FSIZE

Table 268: INTCLR Register Bits

Bit	Name	Reset	RW	Description
31:10	RSVD	0x0	RO	RESERVED
9	XCMPWR	0x0	RW	Transfer complete interrupt, write to register space.
8	XCMPWF	0x0	RW	Transfer complete interrupt, write to FIFO space.
7	XCMPRR	0x0	RW	Transfer complete interrupt, read from register space.
6	XCMPRF	0x0	RW	Transfer complete interrupt, read from FIFO space.
5	IOINTW	0x0	RW	I2C Interrupt Write interrupt.
4	GENAD	0x0	RW	I2C General Address interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 268: INTCLR Register Bits

Bit	Name	Reset	RW	Description
3	FRDERR	0x0	RW	FIFO Read Error interrupt.
2	FUNDFL	0x0	RW	FIFO Underflow interrupt.
1	FOVFL	0x0	RW	FIFO Overflow interrupt.
0	FSIZE	0x0	RW	FIFO Size interrupt.

6.13.2.14INTSET Register

IO Slave Interrupts: Set

OFFSET: 0x0000020C

INSTANCE 0 ADDRESS: 0x5000020C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 269: INTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																						XCMPWR	XCMPWF	XCMPRR	XCMPRF	IOINTW	GENAD	FRDERR	FUNDFL	FOVFL	FSIZE

Table 270: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:10	RSVD	0x0	RO	RESERVED
9	XCMPWR	0x0	RW	Transfer complete interrupt, write to register space.
8	XCMPWF	0x0	RW	Transfer complete interrupt, write to FIFO space.
7	XCMPRR	0x0	RW	Transfer complete interrupt, read from register space.
6	XCMPRF	0x0	RW	Transfer complete interrupt, read from FIFO space.
5	IOINTW	0x0	RW	I2C Interrupt Write interrupt.
4	GENAD	0x0	RW	I2C General Address interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 270: INTSET Register Bits

Bit	Name	Reset	RW	Description
3	FRDERR	0x0	RW	FIFO Read Error interrupt.
2	FUNDFL	0x0	RW	FIFO Underflow interrupt.
1	FOVFL	0x0	RW	FIFO Overflow interrupt.
0	FSIZE	0x0	RW	FIFO Size interrupt.

6.13.2.15REGACCINTEN Register

Register Access Interrupts: Enable

OFFSET: 0x00000210

INSTANCE 0 ADDRESS: 0x50000210

Set bits in this register to allow this module to generate the corresponding interrupt.

Table 271: REGACCINTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
REGACC																															

Table 272: REGACCINTEN Register Bits

Bit	Name	Reset	RW	Description
31:0	REGACC	0x0	RW	Register access interrupts.

6.13.2.16REGACCINTSTAT Register

Register Access Interrupts: Status

OFFSET: 0x00000214

INSTANCE 0 ADDRESS: 0x50000214

Read bits from this register to discover the cause of a recent interrupt.

Table 273: REGACCINTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
REGACC																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 274: REGACCINTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:0	REGACC	0x0	RW	Register access interrupts.

6.13.2.17REGACCINTCLR Register

Register Access Interrupts: Clear

OFFSET: 0x00000218

INSTANCE 0 ADDRESS: 0x50000218

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 275: REGACCINTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
REGACC																															

Table 276: REGACCINTCLR Register Bits

Bit	Name	Reset	RW	Description
31:0	REGACC	0x0	RW	Register access interrupts.

6.13.2.18REGACCINTSET Register

Register Access Interrupts: Set

OFFSET: 0x0000021C

INSTANCE 0 ADDRESS: 0x5000021C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 277: REGACCINTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
REGACC																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 278: REGACCINTSET Register Bits

Bit	Name	Reset	RW	Description
31:0	REGACC	0x0	RW	Register access interrupts.

6.14 Host Side Address Space and Register

6.14.1 Host Address Space and Registers

The Host of the I/O interface can access 128 bytes in the I^{2}C/SPI Slave in either I^{2}C or SPI mode. Offsets 0x00 to 0x77 may be directly mapped to the Direct RAM Area. The remaining eight offset locations access hardware functions within the I^{2}C/SPI Slave. The R/W indicator refers to accesses from the Host.

6.14.1.1 HOST_IER Register

Host Interrupt Enable

OFFSET: 0x78

This register enables the FIFO read interrupts.

Table 279: HOST_IER Register

07	06	05	04	03	02	01	00
FUNDFLEN	RDERREN	SWINT5EN	SWINT4EN	SWINT3EN	SWINT2EN	SWINT1EN	SWINT0EN

Table 280: HOST_IER Register Bits

Bit	Name	Reset	RW	Description
7	FUNDFLEN	0x0	RW	If 1, enable an interrupt that triggers when the FIFO underflows
6	RDERREN	0x0	RW	If 1, enable the interrupt which occurs when the Host attempts to access the FIFO when read access is locked
5	SWINT5EN	0x0	RW	If 1, enable software interrupt 5
4	SWINT4EN	0x0	RW	If 1, enable software interrupt 4
3	SWINT3EN	0x0	RW	If 1, enable software interrupt 3
2	SWINT2EN	0x0	RW	If 1, enable software interrupt 2
1	SWINT1EN	0x0	RW	If 1, enable software interrupt 1
0	SWINT0EN	0x0	RW	If 1, enable software interrupt 0

©2017 Ambiq Micro, Inc.
All rights reserved.

6.14.1.2 HOST_ISR Register

Host Interrupt Status Register

OFFSET: 0x79

The host uses this register to read interrupt status.

Table 281: HOST_ISR Register

07	06	05	04	03	02	01	00
FUNDFLSTAT	RDERRSTAT	SWINT5STAT	SWINT4STAT	SWINT3STAT	SWINT2STAT	SWINT1STAT	SWINT0STAT

Table 282: HOST_ISR Register Bits

Bit	Name	Reset	RW	Description
7	FUNDFLSTAT	0x0	RO	This bit is set by writing a 1 to bit 31 of the IOINTCTL Register, or if the Host attempts a FIFO read when FIFOCTR is 0.
6	RDERRSTAT	0x0	RO	This bit is set by writing a 1 to bit 30 of the IOINTCTL Register, or if the Host attempts a FIFO read when the FIFOUPD bit is a 1.
5	SWINT5STAT	0x0	RO	This bit is set by writing a 1 to bit 29 of the IOINTCTL Register.
4	SWINT4STAT	0x0	RO	This bit is set by writing a 1 to bit 28 of the IOINTCTL Register.
3	SWINT3STAT	0x0	RO	This bit is set by writing a 1 to bit 27 of the IOINTCTL Register.
2	SWINT2STAT	0x0	RO	This bit is set by writing a 1 to bit 26 of the IOINTCTL Register.
1	SWINT1STAT	0x0	RO	This bit is set by writing a 1 to bit 25 of the IOINTCTL Register.
0	SWINT0STAT	0x0	RO	This bit is set by writing a 1 to bit 24 of the IOINTCTL Register.

NOTE: All bits are cleared by a write to the IOINTCLR bit of the IOINTCTL Register.

6.14.1.3 HOST_WCR Register

Host Interrupt Write-to-Clear Register

OFFSET: 0x7A

Write a 1 to a bit in this register to clear a pending interrupt.

Table 283: HOST_WCR Register

07	06	05	04	03	02	01	00
FUNDFLWC	RDERRWC	SWINT5WC	SWINT4WC	SWINT3WC	SWINT2WC	SWINT1WC	SWINT0WC

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 284: HOST_WCR Register Bits

Bit	Name	Reset	RW	Description
7	FUNDFLWC	0x0	WO	Writing a 1 to this bit will clear the pending interrupt status bit FUNDFLSTAT
6	RDERRWC	0x0	WO	Writing a 1 to this bit will clear the pending interrupt status bit RDERRSTAT
5	SWINT5WC	0x0	WO	Writing a 1 to this bit will clear the pending interrupt status bit SWINT5STAT
4	SWINT4WC	0x0	WO	Writing a 1 to this bit will clear the pending interrupt status bit SWINT4STAT
3	SWINT3WC	0x0	WO	Writing a 1 to this bit will clear the pending interrupt status bit SWINT3STAT
2	SWINT2WC	0x0	WO	Writing a 1 to this bit will clear the pending interrupt status bit SWINT2STAT
1	SWINT1WC	0x0	WO	Writing a 1 to this bit will clear the pending interrupt status bit SWINT1STAT
0	SWINT0WC	0x0	WO	Writing a 1 to this bit will clear the pending interrupt status bit SWINT0STAT

6.14.1.4 HOST_WCS Register

Host Interrupt Write-to-Set Register

OFFSET: 0x7B

Write a 1 to a bit in this register to set the status bit of a pending interrupt.

Table 285: HOST_WCS Register

07	06	05	04	03	02	01	00
FUNDFLWS	RDERRWS	SWINT5WS	SWINT4WS	SWINT3WS	SWINT2WS	SWINT1WS	SWINT0WS

Table 286: HOST_WCS Register Bits

Bit	Name	Reset	RW	Description
7	FUNDFLWS	0x0	WO	Writing a 1 to this bit will set the pending interrupt status bit FUNDFLSTAT
6	RDERRWS	0x0	WO	Writing a 1 to this bit will set the pending interrupt status bit RDERRSTAT
5	SWINT5WS	0x0	WO	Writing a 1 to this bit will set the pending interrupt status bit SWINT5STAT
4	SWINT4WS	0x0	WO	Writing a 1 to this bit will set the pending interrupt status bit SWINT4STAT
3	SWINT3WS	0x0	WO	Writing a 1 to this bit will set the pending interrupt status bit SWINT3STAT
2	SWINT2WS	0x0	WO	Writing a 1 to this bit will set the pending interrupt status bit SWINT2STAT
1	SWINT1WS	0x0	WO	Writing a 1 to this bit will set the pending interrupt status bit SWINT1STAT
0	SWINT0WS	0x0	WO	Writing a 1 to this bit will set the pending interrupt status bit SWINT0STAT

©2017 Ambiq Micro, Inc.
All rights reserved.

6.14.1.5 FIFOCTRLO Register

FIFOCTR Low Byte

OFFSET: 0x7C

This register allows the host to read the lower eight bits of the FIFOCTR register.

Table 287: FIFOCTRLO Register

07	06	05	04	03	02	01	00
FIFOCTRLO							

Table 288: FIFOCTRLO Register Bits

Bit	Name	Reset	RW	Description
7:0	FIFOCTRLO	0x0	RO	Reads the lower eight bits of FIFOCTR

6.14.1.6 FIFOCTRUP Register

FIFOCTR Upper Byte

OFFSET: 0x7D

This register allows the host to read the upper two bits of the FIFOCTR register.

Table 289: FIFOCTRUP Register

07	06	05	04	03	02	01	00
RSVD						FIFOCTRUP	

Table 290: FIFOCTRUP Register Bits

Bit	Name	Reset	RW	Description
1:0	FIFOCTRUP	0x0	RO	Reads the upper two bits of FIFOCTR

©2017 Ambiq Micro, Inc.
All rights reserved.

6.14.1.7 FIFO Register

FIFO Read Data

OFFSET: 0x7F

Read this register for FIFO data.

Table 291: FIFO Register

07	06	05	04	03	02	01	00
FIFO							

Table 292: FIFO Register Bits

Bit	Name	Reset	RW	Description
7:0	FIFO	0x0	RO	Reads the top byte of the FIFO

©2017 Ambiq Micro, Inc.
All rights reserved.

7. PDM/I2S Module

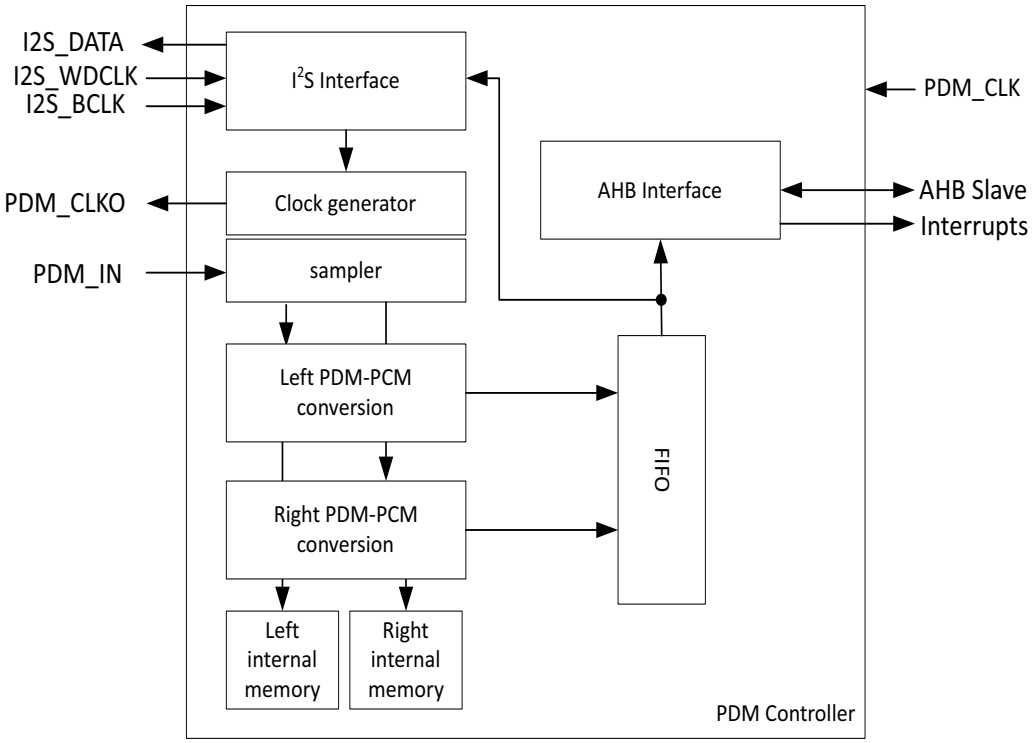


Figure 47. Block Diagram for PDM Module

7.1 Features

The PDM module provides support for low power Pulse-Density Modulated (PDM) to Pulse-Code Modulated (PCM) conversion and optional I2S slave interface for external host processor communication.

The PDM controller generates the clock output to interface to 1 (mono) or 2 (stereo) PDM-based digital microphones. The PDM input data is sampled on the rising (left/mono) and falling (right/stereo) edges of PDM clock. The controller supports 16-bit PCM output sampling at 8/16kHz. The single bit pulse-density modulated (PDM) bit stream data is converted into pulse-code modulated (PCM) data and provides an optional I^2S serial audio/voice data format. The converted PCM data is stored in an asynchronous FIFO where is can then be retrieved by the MCU CPU via the AHB slave interface.

The PDM controller includes the following features:

- Stereo or mono PDM input
- 16bit PCM digital output
- I^2S slave interface output (optional)
- Support for variable PDM output clock rates (750-768kHz, 1.5-1.536MHz, 3-3.072MHz: output clock depends on source clock from I^2S or MCU)
- 64x Decimation of PDM bit stream input to PCM output
- Sampling rate: 8kHz, 16kHz (additional sample rates are supported as needed)
- AHB slave interface for register control, status programming and PCM FIFO data access

©2017 Ambiq Micro, Inc.
All rights reserved.

7.2 Functional Overview

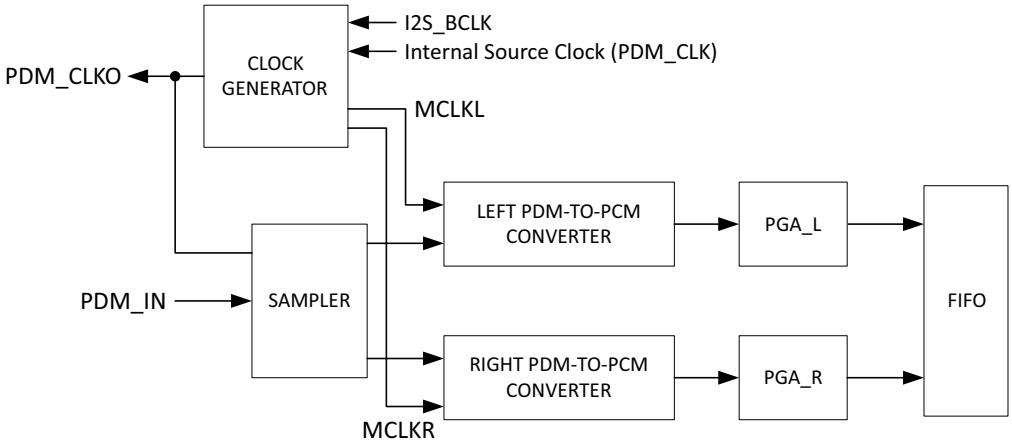
The Apollo2 Blue integrates a PDM controller which has two modes of operation: low power mode and normal mode. The low power mode is intended for wake-on-voice/keyword detect operation. A low frequency PDM clock is generated to the microphone (requires digital microphone that supports low power operation). Once a keyword is detected, the MCU generates a wake event to enter normal mode. In normal mode, higher PDM frequencies are supported to process audio/voice as needed for voice recording, voice calls, etc.

7.2.1 PDM-to-PCM Conversion

The PDM-to-PCM core IP converts PDM bit stream data into 16-bit PCM data through internal data sampling, filtering, and PGA amplification. The controller may be operated at stereo or mono mode in normal operation, system reset or power down mode when not in use. Each mode can be programmed through registers.

The basic PCM conversion flow is shown in Figure 48.

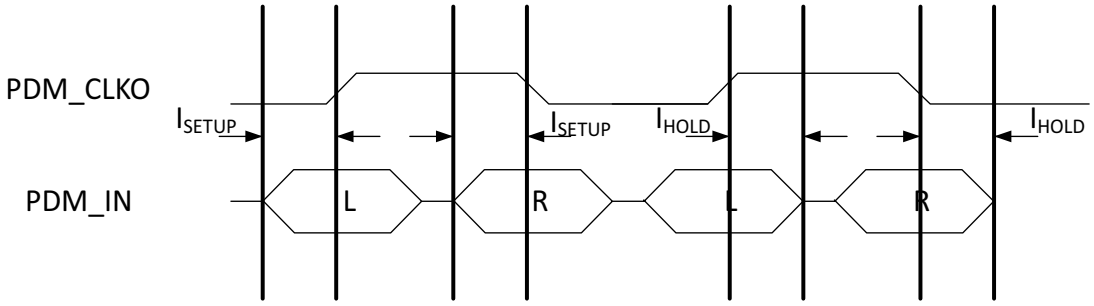
Figure 48. Stereo PDM to PCM Conversion Path



7.2.2 Clock Generation

The PDM module generates the clock which is supplied on the PDM_CLKO pin to the PDM source, and is shown in Figure 49 below.

Figure 49. PDM Clock Timing Diagram



There are two sources for this clock, which are selected by the VCFG_SELAP register bit. If SELAP is 0, this clock is an internally generated clock which is selected by the VCFG_PDMCLKSEL field and can

©2017 Ambiq Micro, Inc.
All rights reserved.

range from 12 MHz to 187.5 KHz, and is enabled by setting the PCFG_PDMCLK bit. These clock selections are derived from the internal 48 MHz HFRC oscillator and therefore will have some frequency variation. If SELAP is 1, this clock is supplied externally on the I2S_BCLK pin. The input clock is used as the clock of the internal PDM logic, and therefore the lowest acceptable frequency should be selected to minimize power. The PDM logic includes separately clocked sections for each of the left and right channels.

The input clock is divided by 1, 2, 3 or 4 as selected by the PCFG_MCLKDIV field to produce the PDM_CLKO output.

NOTE: If achieving a nominal 50% duty cycle PDM output clock is important, then using a clock divider of divide-by-3 (MCKDIV3) for PCFG_MCLKDIV should be avoided as the resulting divided clock has a duty cycle of 67%, not the expected 50%. The other PCFG_MCLKDIV settings, MCKDIV1, MCKDIV2 and MCKDIV4 can be used to generate an output clock close to 50% duty cycle. See Table 293 for reference.

The following equations are for reference showing the relationship between SINC_RATE, MCLKDIV, sample rate and OSR.

$F_{PDM_CLK} = F_S \times 2 \times SINC_RATE \times MCLKDIV$

$F_{PDM_CLKO} = F_S \times 2 \times SINC_RATE$

$OSR = F_{PDM_CLKO} / F_S = 2 \times SINC_RATE$

The PDM module also requires a system clock to operate, which is enabled by the VCFG_IOCLKEN register bit. This bit should be kept at 0 whenever the PDM is not capturing input data to minimize power consumption.

The serial PDM input data is oversampled by a value specified in the PCFG_SINCRATE register field to produce the PCM data. The resulting PCM data rate is the PDM_CLKO frequency divided by the SINCRATE value and divided by 2. The table below shows some examples of frequency selection.

Table 293: PDM Clock Output Reference Table

F_S (kHz)	Duty Cycle (%)	F_{PDM_CLKO}(kHz)	OSR	MCLKDIV	SYNC_ RATE	Clock Source
7.8125	50	750	96	MCKDIV1	48	750kHz (MCU HFRC)
15.625	50	750	48	MCKDIV1	24	750kHz (MCU HFRC)
15.625	50	1500	96	MCKDIV1	48	1.5MHz (MCU HFRC)
7.8125	67	1000	128	MCKDIV3	64	3MHz (MCU HFRC)
8	50	768	96	MCKDIV1	48	768kHz (external I2S_BCLK)
16	50	768	48	MCKDIV1	24	768kHz (external I2S_BCLK)
16	50	3072	192	MCKDIV4	96	12.288MHz (external I2S BCLK)

The PDM controller also includes separate clock gates for left and right channel. This allows for lower power operation in mono microphone configuration.

7.2.3 Clock Switching

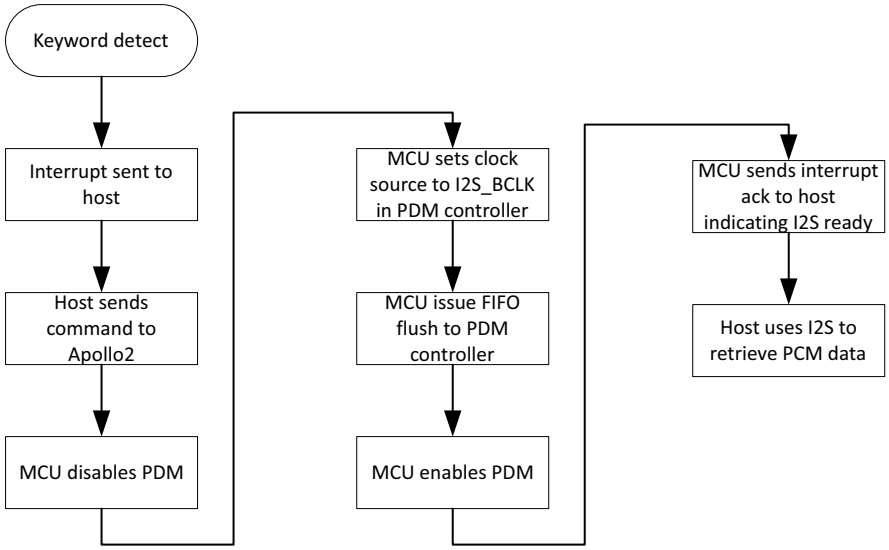
The Apollo2 Blue supports dual-mode clock sourcing for PDM microphone operation. The first mode is clock sourcing from the MCU directly (via divided down HFRC reference). The second mode is clock sourcing from an external host via the I2S_BCLK.

©2017 Ambiq Micro, Inc.
All rights reserved.

The scenario for switching clock sources is if a higher accuracy clock is required based on the audio sampling requirements. The MCU clock source is based off of an RC oscillator which has intrinsic jitter that affects the quality of the resulting clock. For general voice command processing, the quality of the clock is sufficient. However, for voice recording/playback scenarios, this could manifest as pitch/noise problems. In a scenario where the Apollo2 Blue is used for voice/keyword detect, upon detection, the Apollo2 Blue can generate notification to the external host. The external host can then send a command to the Apollo2 Blue to switch clock source.

Clock switching requires careful orchestration since the PDM controller will continue to collect/process samples during this transition. The flow below is an example of how this transition can be handled.

Figure 50. PDM Clock Source Switching Flow



7.2.4 Operating Modes

The PDM module can operate in a variety of modes selected by the CHSET, PCMPACK and LRSWAP register fields, as shown in Table 294 below. The FIFO Data Format column shows the PCM data that will be presented on each 32-bit read from the FIFO, in two 16-bit segments. “L0” indicates the first 16-bit sample from the left channel, “L1” indicates the second left channel sample, “R0” indicates the first 16-bit sample from the right channel, etc.

Table 294: PDM Operating Modes and Data Formats

Mode	CHSET	PCMPACK	LRSWAP	31 - FIFO Data Format - 0		MCLKL	MCLKR
Mono Left Packed	01	1	N/A	L1	L0	En	Dis
				L3	L2		
Mono Right Packed	10	1	N/A	R1	R0	Dis	En
				R3	R2		
Stereo Packed	11	1	0	R0	L0	En	En
				R1	L1		
Stereo Packed Swapped	11	1	1	L0	R0	En	En
				L1	R1		

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 294: PDM Operating Modes and Data Formats

Mode	CHSET	PCMPACK	LRSWAP	31 - FIFO Data Format - 0		MCLKL	MCLKR
Mono Left Unpacked	01	0	N/A	0000	L0	En	Dis
				0000	L1		
Mono Right Unpacked	10	0	N/A	0000	R0	Dis	En
				0000	R1		
Stereo Unpacked	11	0	0	0000	L0	En	En
				0000	R0		
Stereo Unpacked Swapped	11	0	1	0000	R0	En	En
				0000	L0		
Disabled	00	N/A	N/A	0000	0000	Dis	Dis
				0000	0000		

The MCLKL and MCLKR columns indicate whether the left and right channel clocks are enabled or disabled.

7.2.5 FIFO Control and Interrupts

The PCM data is retrieved from the PDM module through a 256-word FIFO, read at the FRD Register. The number of words currently in the FIFO (0 to 256) is read in the FR_FIFOCNT field. If the FLUSH Register is written (with any value) FIFOCNT is set to 0 and any data in the FIFO is discarded. Each read from the FRD Register will decrement the FIFOCNT value, and FIFOCNT will be incremented each time new PCM data is written into the FIFO.

There are three interrupts which are generated based on the number of words in the FIFO. The UNDFL interrupt is generated if software reads from the FRD register when FIFOCNT is 0. The OVF interrupt is generated if PCM data is received when FIFOCNT is 256. The THR interrupt is set if PCM data is received and FIFOCNT is greater than or equal to the value in the FTHR_FIFOTHR Register field.

7.2.6 Digital Volume Gain

The PDM controller supports digital volume control with a range from -12dB to +10.5 dB in steps of 1.5 dB. It is programmed by register PGA_L and PGA_R for both left and right channels.

Table 295: Digital Volume Control

Port Name	Default	Description
PGA_L[3:0]	0000	Left Channel PGA Gain: +1.5dB/step 7→ +10.5dB; 6→ +9.0dB; 5→ +7.5dB; 4→ +6.0dB; 3→ +4.5dB; 2→ +3.0dB; 1→ +1.5dB; 0→ 0.0dB; 15→ -1.5dB; 14→ -3.0dB; 13→ -4.5dB; 12→ -6.0dB; 11→ -7.5dB; 10→ -9.0dB; 9→ -10.5dB; 8→ -12dB

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 295: Digital Volume Control

Port Name	Default	Description
PGA_R[3:0]	0000	Right Channel PGA Gain: +1.5dB/step 7→ +10.5dB; 6→ +9.0dB; 5→ +7.5dB; 4→ +6.0dB; 3→ +4.5dB; 2→ +3.0dB; 1→ +1.5dB; 0→ 0.0dB; 15→ -1.5dB; 14→ -3.0dB; 13→ -4.5dB; 12→ -6.0dB; 11→ -7.5dB; 10→ -9.0dB; 9→ -10.5dB; 8→ -12dB

7.2.7 Low Pass Filter (LPF)

The controller's internal low pass filters attenuate the out-of-band noise at predefined bandwidth and corners.

Table 296: LPF Digital Filter Parameters

Parameter	Min	Typ	Max	Units
Pass band corner frequency		0.41		Fs
Pass band ripple	-1		1	dB
Stop band corner frequency	0.59			Fs
Stop band rejection		-60		dB

7.2.8 High Pass Filter

The filter response for high pass filter is characterized as:

$$H(Z) = (1 - Z^{1}) / [1 - (1 - 2^{-HPGAIN}) Z^{-1}]$$

In default mode, HPGAIN = 1011, so the high pass filter can be formulated by the polynomial:

$$H(Z) = (1 - Z^{1}) / [1 - 0.99951Z^{-1}]$$

7.3 I2S Slave Interface

The PDM controller supports an optional I^2S slave interface for PCM serial data output. This enables support for an external host controller to receive the serial output data from the converted PDM stream. In I^2S slave mode, the MSB of I2S_DAT PCM data is available on the second rising edge of I2S_BCLK following an I2S_WDCLK transition. The other bits up to the LSB are sent in order. The word length is 16 bits so there will be 16 bits of unused I2S_BCLK cycles between the LSB of one sample data and the MSB of the next one. The I2S_WDCLK is always 32 clock cycles/phase.

©2017 Ambiq Micro, Inc.
All rights reserved.

Figure 51. I2S Interface Data Format Timing

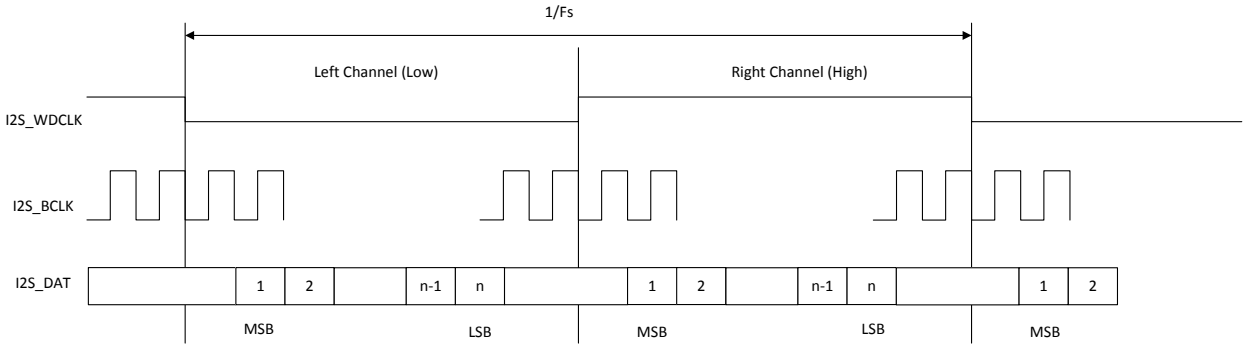
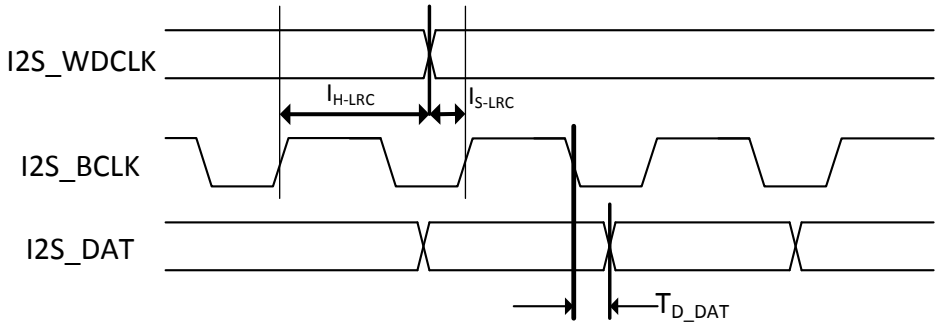


Figure 52. I2S Interface Setup and Hold Timing Diagram



7.4 PDM Registers

PDM Audio

INSTANCE 0 BASE ADDRESS:0x50011000

©2017 Ambiq Micro, Inc.
All rights reserved.

7.4.1 Register Memory Map

Table 297: PDM Register Map

Address(s)	Register Name	Description
0x50011000	PCFG	PDM Configuration Register
0x50011004	VCFG	Voice Configuration Register
0x50011008	FR	Voice Status Register
0x5001100C	FRD	FIFO Read
0x50011010	FLUSH	FIFO Flush
0x50011014	FTHR	FIFO Threshold
0x50011200	INTEN	IO Master Interrupts: Enable
0x50011204	INTSTAT	IO Master Interrupts: Status
0x50011208	INTCLR	IO Master Interrupts: Clear
0x5001120C	INTSET	IO Master Interrupts: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

7.4.2 PDM Registers

7.4.2.1 PCFG Register

PDM Configuration Register

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x50011000

PDM Configuration Register

Table 298: PCFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LRSWAP	PGARIGHT				PGALEFT				RSVD				MCLKDIV		SINCRATE							ADCHPD	HPCUTOFF				CYCLES			SOFTMUTE	PDMCORE

Table 299: PCFG Register Bits

Bit	Name	Reset	RW	Description
31	LRSWAP	0x0	RW	Left/right channel swap. EN = 0x1 - Swap left and right channels (FIFO Read RIGHT_LEFT). NOSWAP = 0x0 - No channel swapping (IFO Read LEFT_RIGHT).
30:27	PGARIGHT	0x0	RW	Right channel PGA gain. M15DB = 0xF - -1.5 db gain. M300DB = 0xE - -3.0 db gain. M45DB = 0xD - -4.5 db gain. M60DB = 0xC - -6.0 db gain. M75DB = 0xB - -7.5 db gain. M90DB = 0xA - -9.0 db gain. M105DB = 0x9 - -10.5 db gain. M120DB = 0x8 - -12.0 db gain. P105DB = 0x7 - 10.5 db gain. P90DB = 0x6 - 9.0 db gain. P75DB = 0x5 - 7.5 db gain. P60DB = 0x4 - 6.0 db gain. P45DB = 0x3 - 4.5 db gain. P30DB = 0x2 - 3.0 db gain. P15DB = 0x1 - 1.5 db gain. 0DB = 0x0 - 0.0 db gain.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 299: PCFG Register Bits

Bit	Name	Reset	RW	Description
26:23	PGALEFT	0x0	RW	Left channel PGA gain. M15DB = 0xF - -1.5 db gain. M300DB = 0xE - -3.0 db gain. M45DB = 0xD - -4.5 db gain. M60DB = 0xC - -6.0 db gain. M75DB = 0xB - -7.5 db gain. M90DB = 0xA - -9.0 db gain. M105DB = 0x9 - -10.5 db gain. M120DB = 0x8 - -12.0 db gain. P105DB = 0x7 - 10.5 db gain. P90DB = 0x6 - 9.0 db gain. P75DB = 0x5 - 7.5 db gain. P60DB = 0x4 - 6.0 db gain. P45DB = 0x3 - 4.5 db gain. P30DB = 0x2 - 3.0 db gain. P15DB = 0x1 - 1.5 db gain. 0DB = 0x0 - 0.0 db gain.
22:19	RSVD	0x0	RO	This bitfield is reserved for future use.
18:17	MCLKDIV	0x0	RW	PDM_CLK frequency divisor. MCKDIV4 = 0x3 - Divide input clock by 4 MCKDIV3 = 0x2 - Divide input clock by 3 MCKDIV2 = 0x1 - Divide input clock by 2 MCKDIV1 = 0x0 - Divide input clock by 1
16:10	SINCRATE	0x30	RW	SINC decimation rate.
9	ADCHPD	0x1	RW	High pass filter control. EN = 0x1 - Enable high pass filter. DIS = 0x0 - Disable high pass filter.
8:5	HPCUTOFF	0xb	RW	High pass filter coefficients.
4:2	CYCLES	0x1	RW	Number of clocks during gain-setting changes.
1	SOFTMUTE	0x0	RW	Soft mute control. EN = 0x1 - Enable Soft Mute. DIS = 0x0 - Disable Soft Mute.
0	PDMCORE	0x1	RW	Data Streaming Control. EN = 0x1 - Enable Data Streaming. DIS = 0x0 - Disable Data Streaming.

7.4.2.2 VCFG Register

Voice Configuration Register

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x50011004

Voice Configuration Register

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 300: VCFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IOCLKEN	RSTB	PDMCLKSEL			PDMCLK	RSVD					I2SMODE	BCLKINV	RSVD	DMICKDEL	SELAP	RSVD							PCMPACK	RSVD			CHSET	RSVD			

Table 301: VCFG Register Bits

Bit	Name	Reset	RW	Description
31	IOCLKEN	0x0	RW	Enable the IO clock. DIS = 0x0 - Disable FIFO read. EN = 0x1 - Enable FIFO read.
30	RSTB	0x0	RW	Reset the IP core. RESET = 0x0 - Reset the core. NORM = 0x1 - Enable the core.
29:27	PDMCLKSEL	0x0	RW	Select the PDM input clock. DISABLE = 0x0 - Static value. 12MHz = 0x1 - PDM clock is 12 MHz. 6MHz = 0x2 - PDM clock is 6 MHz. 3MHz = 0x3 - PDM clock is 3 MHz. 1_5MHz = 0x4 - PDM clock is 1.5 MHz. 750KHz = 0x5 - PDM clock is 750 KHz. 375KHz = 0x6 - PDM clock is 375 KHz. 187KHz = 0x7 - PDM clock is 187.5 KHz.
26	PDMCLK	0x0	RW	Enable the serial clock. DIS = 0x0 - Disable serial clock. EN = 0x1 - Enable serial clock.
25:21	RSVD	0x0	RO	This bitfield is reserved for future use.
20	I2SMODE	0x0	RW	I2S interface enable. DIS = 0x0 - Disable I2S interface. EN = 0x1 - Enable I2S interface.
19	BCLKINV	0x0	RW	I2S BCLK input inversion. INV = 0x0 - BCLK inverted. NORM = 0x1 - BCLK not inverted.
18	RSVD	0x0	RO	This bitfield is reserved for future use.
17	DMICKDEL	0x0	RW	PDM clock sampling delay. 0CYC = 0x0 - No delay. 1CYC = 0x1 - 1 cycle delay.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 301: VCFG Register Bits

Bit	Name	Reset	RW	Description
16	SELAP	0x0	RW	Select PDM input clock source. I2S = 0x1 - Clock source from I2S BCLK. INTERNAL = 0x0 - Clock source from internal clock generator.
15:9	RSVD	0x0	RO	This bitfield is reserved for future use.
8	PCMPACK	0x0	RW	PCM data packing enable. DIS = 0x0 - Disable PCM packing. EN = 0x1 - Enable PCM packing.
7:5	RSVD	0x0	RO	This bitfield is reserved for future use.
4:3	CHSET	0x1	RW	Set PCM channels. DIS = 0x0 - Channel disabled. LEFT = 0x1 - Mono left channel. RIGHT = 0x2 - Mono right channel. STEREO = 0x3 - Stereo channels.
2:0	RSVD	0x0	RO	This bitfield is reserved for future use.

7.4.2.3 FR Register

Voice Status Register

OFFSET: 0x00000008

INSTANCE 0 ADDRESS: 0x50011008

Voice Status Register

Table 302: FR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																							FIFOCNT								

Table 303: FR Register Bits

Bit	Name	Reset	RW	Description
31:9	RSVD	0x0	RO	This bitfield is reserved for future use.
8:0	FIFOCNT	0x0	RO	Valid 32-bit entries currently in the FIFO.

©2017 Ambiq Micro, Inc.
All rights reserved.

7.4.2.4 FRD Register

FIFO Read

OFFSET: 0x0000000C

INSTANCE 0 ADDRESS: 0x5001100C

FIFO Read

Table 304: FRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFOREAD																															

Table 305: FRD Register Bits

Bit	Name	Reset	RW	Description
31:0	FIFOREAD	0x0	RO	FIFO read data.

7.4.2.5 FLUSH Register

FIFO Flush

OFFSET: 0x00000010

INSTANCE 0 ADDRESS: 0x50011010

FIFO Flush

Table 306: FLUSH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															FIFOFLUSH

Table 307: FLUSH Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	This bitfield is reserved for future use.
0	FIFOFLUSH	0x0	WO	FIFO FLUSH.

©2017 Ambiq Micro, Inc.
All rights reserved.

7.4.2.6 FTHR Register

FIFO Threshold

OFFSET: 0x00000014

INSTANCE 0 ADDRESS: 0x50011014

FIFO Threshold

Table 308: FTHR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								FIFOTHR							

Table 309: FTHR Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	This bitfield is reserved for future use.
7:0	FIFOTHR	0xc0	RW	FIFO interrupt threshold.

7.4.2.7 INTEN Register

IO Master Interrupts: Enable

OFFSET: 0x00000200

INSTANCE 0 ADDRESS: 0x50011200

Set bits in this register to allow this module to generate the corresponding interrupt.

Table 310: INTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													UNDFL	OVF	THR

Table 311: INTEN Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	RESERVED
2	UNDFL	0x0	RW	This is the FIFO underflow interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 311: INTEN Register Bits

Bit	Name	Reset	RW	Description
1	OVF	0x0	RW	This is the FIFO overflow interrupt.
0	THR	0x0	RW	This is the FIFO threshold interrupt.

7.4.2.8 INTSTAT Register

IO Master Interrupts: Status

OFFSET: 0x00000204

INSTANCE 0 ADDRESS: 0x50011204

Read bits from this register to discover the cause of a recent interrupt.

Table 312: INTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													UNDFL	OVF	THR

Table 313: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	RESERVED
2	UNDFL	0x0	RW	This is the FIFO underflow interrupt.
1	OVF	0x0	RW	This is the FIFO overflow interrupt.
0	THR	0x0	RW	This is the FIFO threshold interrupt.

7.4.2.9 INTCLR Register

IO Master Interrupts: Clear

OFFSET: 0x00000208

INSTANCE 0 ADDRESS: 0x50011208

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 314: INTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													UNDFL	OVF	THR

Table 315: INTCLR Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	RESERVED
2	UNDFL	0x0	RW	This is the FIFO underflow interrupt.
1	OVF	0x0	RW	This is the FIFO overflow interrupt.
0	THR	0x0	RW	This is the FIFO threshold interrupt.

7.4.2.10 INTSET Register

IO Master Interrupts: Set

OFFSET: 0x0000020C

INSTANCE 0 ADDRESS: 0x5001120C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 316: INTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													UNDFL	OVF	THR

Table 317: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	RESERVED
2	UNDFL	0x0	RW	This is the FIFO underflow interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 317: INTSET Register Bits

Bit	Name	Reset	RW	Description
1	OVF	0x0	RW	This is the FIFO overflow interrupt.
0	THR	0x0	RW	This is the FIFO threshold interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

8. GPIO and Pad Configuration Module

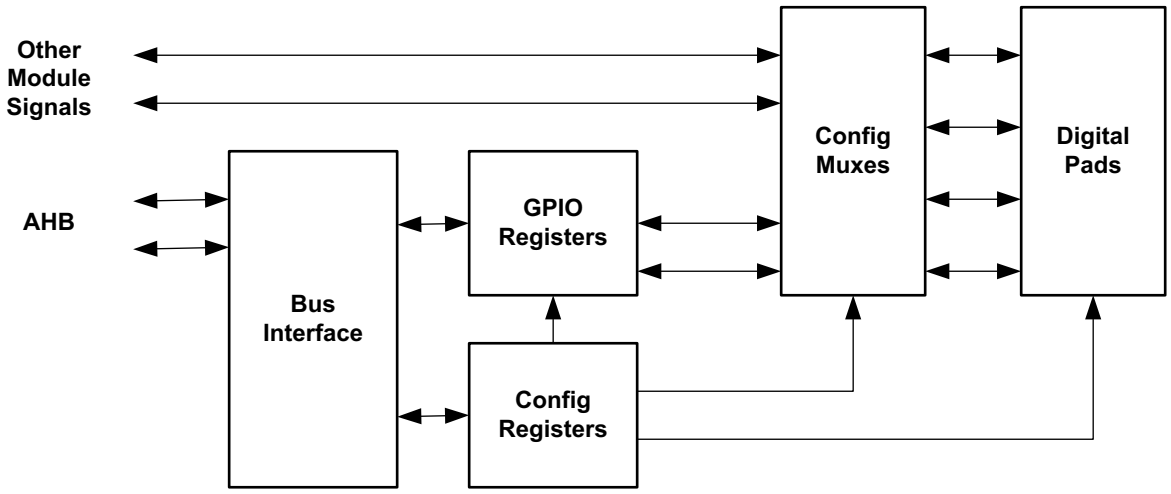


Figure 53. Block diagram for the General Purpose I/O (GPIO) Module

8.1 Functional Overview

The General Purpose I/O and Pad Configuration (GPIO) Module, shown in Figure 53, controls connections to up to 50 digital/analog pads. Each pad may be connected to a variety of module interface signals, with all pad input and output selection and control managed by the GPIO module. In addition, any pad may function as a general purpose input and/or output pad which may be configured for a variety of external functions. Each GPIO may be configured to generate an interrupt when a transition occurs on the input.

Note: Once the PADKEY is written, it should be explicitly cleared (with a non-key value) after GPIO configuration register updates are complete.

8.2 Pad Configuration Functions

The REG_GPIO_PADREGy (y = A to M) registers are used to control the function of each pad. Note that the REG_GPIO_PADKEY Register must be set to the value 0x73 in order to write the PADREGn Registers. The REG_GPIO_PADREGy_PADnFNCSEL (n = 0 to 49) field selects one of up to eight signals to be used for each pad, as shown in Table 319. Functions are grouped by module, with the color coding shown in Table 320. This table also defines the pad type for each configuration. The Special pad types are defined in Table 321. Note that the CSP package only supports pads 0 through 23, 26, 28-29, 39-41, 44 and 47-49, which are indicated by an ‘X’ in the CSP PKG column of Table 319.

The REG_GPIO_PADREGy_PADnSTRNG bit and the REG_GPIO_ALTPADCFGy_PADn_DS1 bit control the drive strength of the pad. Nominal drive strengths of 2, 4, 8 or 12 mA can be selected with the setting of these two bits according to Table 318.

Table 318: Drive Strength Control Bits

ALTPADCFGy_ PADn_DS1	ADREGy_ PADnSTRNG	Nominal Drive Strength (mA)
0	0	2
0	1	4
1	0	8

©2017 Ambiq Micro, Inc.
All rights reserved.

ALTPADCFGy_PADn_DS1	ADREGy_PADnSTRNG	Nominal Drive Strength (mA)
1	1	12

For all pads except for pad 20, REG_GPIO_PADREGy_PADnPULL bit enables a weak pull-up on the pad when set to one. For pad 20, the REG_GPIO_PADREGy_PAD20PULL bit enables a weak pull-down on the pad when set to one. The REG_GPIO_PADREGy_PADnINPEN bit must be set to enable the pad input, and should be left clear whenever the pad is not used in order to eliminate any leakage current in the pad.

Pads 22 and 41 have selectable high side power switch transistors to provide ~1 Ω switches to VDDH. Pad 4 has a selectable low side power switch transistor to provide a ~1 Ω switch to VSS. The high side power switches are enabled by setting the REG_GPIO_PADREGF_PAD22PWRUP or REG_GPIO_PADREGK_PAD41PWRUP bits, and the low side switch is enabled by setting the REG_GPIO_PADREGB_PAD4PWRDN bit. Once enabled, the switches operate in parallel with the normal pad function.

Pads 0, 1, 5, 6, 8, 9, 25, 27, 39, 40, 42, 43, 48 and 49 include optional pull-up resistors for use in I^2C mode, to eliminate the need for external resistors. If the pull-up is enabled by the PADnPULL bit, the REG_GPIO_PADREGy_PADnRSEL field selects the size of the pull-up resistor as shown in Table 322.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 319: Apollo2 Blue Pad Function Mapping

GPIO/Pad	0	1	2	3	4	5	6	7
0	SLSCL	SLSCK	CLKOUT	GPIO00	MxSCKLB	M2SCK	MxSCLLB	M2SCL
1	SLSDA	SLMISO	UART0TX	GPIO01	MxMISOLB	M2MISO	MxSDALB	M2SDA
2	SLWIR3	SLMOSI	UART0RX	GPIO02	MxMOSILB	M2MOSI	MxWIR3LB	M2WIR3
3	UA0RTS	SLnCE	M1nCE4	GPIO03	MxnCELB	M2nCE0	TRIG1	I2S _WCLK
4	UA0CTS	SLINT	M0nCE5	GPIO04	SLINTGP	M2nCE5	CLKOUT	32KHz_XT
5	M0SCL	M0SCK	UA0RTS	GPIO05	M0SCKLB	-	M0SCLLB	M1nCE2
6	M0SDA	M0MISO	UA0CTS	GPIO06	SLMISOLB	M1nCE0	SLSDALB	I2S _DAT
7	M0WIR3	M0MOSI	CLKOUT	GPIO07	TRIG0	UART0TX	SLWIR3LB	M1nCE1
8	M1SCL	M1SCK	M0nCE4	GPIO08	M2nCE4	M1SCKLB	UART1TX	M1SCLLB
9	M1SDA	M1MISO	M0nCE5	GPIO09	M4nCE5	SLMISOLB	UART1RX	SLSDALB
10	M1WIR3	M1MOSI	M0nCE6	GPIO10	M2nCE6	UA1RTS	M4nCE4	SLWIR3LB
11	ADCSE2	M0nCE0	CLKOUT	GPIO11	M2nCE7	UA1CTS	UART0RX	PDM_DATA
12	ADCD0NSE9	M1nCE0	TCTA0	GPIO12	CLKOUT	PDM_CLK	UA0CTS	UART1TX
13	ADCD0PSE8	M1nCE1	TCTB0	GPIO13	M2nCE3	-	UA0RTS	UART1RX
14	ADCD1P	M1nCE2	UART1TX	GPIO14	M2nCE1	-	SWDCK	32KHz_XT
15	ADCD1N	M1nCE3	UART1RX	GPIO15	M2nCE2	-	SWDIO	SWO
16	ADCSE0	M0nCE4	TRIG0	GPIO16	M2nCE3	CMPIN0	UART0TX	UA1RTS
17	CMPRF1	M0nCE1	TRIG1	GPIO17	M4nCE3	-	UART0RX	UA1CTS
18	CMPIN1	M0nCE2	TCTA1	GPIO18	M4nCE1	-	UART1TX	32KHz_XT
19	CMPRF0	M0nCE3	TCTB1	GPIO19	TCTA1	-	UART1RX	I2S_BCLK
20	SWDCK	M1nCE5	TCTA2	GPIO20	UART0TX	UART1TX	-	-
21	SWDIO	M1nCE6	TCTB2	GPIO21	UART0RX	UART1RX	-	-
22	UART0TX	M1nCE7	TCTA3	GPIO22	PDM_CLK	-	TCTB1	SWO
24	-	-	CLKOUT	-	-	-	-	-
29	ADCSE1	M1nCE6	TCTA2	GPIO29	UA0CTS	UA1CTS	M4nCE0	PDM_DATA
30	-	M1nCE7	TCTB2	GPIO30	UART0TX	UA1RTS	-	I2S _DAT
35	ADCSE7	M1nCE0	UART1TX	GPIO35	M4nCE6	TCTA1	UA0RTS	M3nCE2
36	TRIG1	M1nCE1	UART1RX	GPIO36	32KHz_XT	M2nCE0	UA0CTS	M3nCE3
39	UART0TX	UART1TX	CLKOUT	GPIO39	M4SCL	M4SCK	M4SCKLB	M4SCLLB
40	UART0RX	UART1RX	TRIG0	GPIO40	M4SDA	M4MISO	SLMISOLB	SLSDALB
41	M2nCE1	CLKOUT	SWO	GPIO41	M3nCE5	M5nCE7	M4nCE2	UA0RTS
42	M2nCE2	-	-	-	-	-	-	-
44	UA1RTS	M0nCE2	TCTA1	GPIO44	M4WIR3	M4MOSI	M5nCE6	SLWIR3LB
45	-	-	-	-	-	-	M5nCE5	-
46	-	-	-	-	-	M5nCE4	-	-
47	-	-	-	-	-	M5MOSI	-	-
48	-	-	-	-	-	M5SCK	-	-
49	-	-	-	-	-	M5MISO	-	-

NOTE: Pads 24, 42, and 45-48 are internally connected to the BLE sub-system, and these pins must be “no connects” externally. These pads must be configured to the functions specified in this table for proper connection to the BLE. See Internal Die-to-Die Connections section in the Bluetooth Low-Energy Sub-system chapter for more information.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 320: Pad Function Color and Symbol Code

Color/ Symbol	Function	Pad Type
	ADC Signals	Analog or Input
	I2C/SPI Slave Signals	Input, Special or Push-pull output
	I2C/SPI Master 0 Signals	Input, Special or Push-pull output
	I2C/SPI Master 1 Signals	Input, Special or Push-pull output
	I2C/SPI Master 2 Signals	Input, Special or Push-pull output
	I2C/SPI Master 3 Signals	Input, Special or Push-pull output
	I2C/SPI Master 4 Signals	Input, Special or Push-pull output
	I2C/SPI Master 5 Signals	Input, Special or Push-pull output
	GPIO Signals	Controlled by GPIO Configuration
	Counter/Timer Signals	Controlled by CTIMER Configuration
	UART0 Signals	Input or Push-pull output
	UART1 Signals	Input or Push-pull output
	Audio Signals	Input or Push-pull output
	CLKOUT Signals	Push-pull Output
	Loopback Connections	Tri-state
	Miscellaneous Signals	Input Special or Push-pull output

Table 321: Special Pad Types

Pad	PADnFNCSEL	Name	Pad Type
0	7	M2SCL	Open Drain*
1	0	SLSDA	Bidirectional Open Drain
1	7	M2SDA	Bidirectional Open Drain*
2	0	SLWIR3	Bidirectional Tri-state*
2	7	M2WIR3	Bidirectional Tri-state*
5	0	M0SCL	Open Drain
6	0	M0SDA	Bidirectional Open Drain
7	0	M0WIR3	Bidirectional Tri-state
8	0	M1SCL	Open Drain
9	0	M1SDA	Bidirectional Open Drain
10	0	M1WIR3	Bidirectional Tri-state
15	6	SWDIO	Bidirectional Tri-state
21	0	SWDIO	Bidirectional Tri-state

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 321: Special Pad Types

Pad	PADnFNCSEL	Name	Pad Type
25	4	M2SDA	Bidirectional Open Drain
27	4	M2SCL	Open Drain
28	4	M2WIR3	Bidirectional Tri-state
38	4	M3WIR3	Bidirectional Tri-state
39	4	M4SCL	Open Drain
40	4	M4SDA	Bidirectional Open Drain
42	4	M3SCL	Open Drain
43	4	M3SDA	Bidirectional Open Drain
44	4	M4WIR3	Bidirectional Tri-state
47	4	M5WIR3	Bidirectional Tri-state
48	4	M5SCL	Open Drain
49	4	M5SDA	Bidirectional Open Drain

Table 322: I^2C Pullup Resistor Selection

RSEL[1:0]	Pullup Resistor
00	1.5 kΩ
01	6 kΩ
10	12 kΩ
11	24 kΩ

8.3 General Purpose I/O (GPIO) Functions

For each pad, if the PADnFNCSEL field is set to 0x3 the pad is connected to the corresponding GPIO signal. This section describes the configuration functions specific to GPIO pads.

8.3.1 Configuring the GPIO Functions

Each GPIO must be configured in the REG_GPIO_CFGy (y = A to G) Registers as an input and/or output. Note that the PADKEY Register must be set to the value 0x73 in order to write the REG_GPIO_CFGy Registers. Each output may be push-pull, open drain, disabled, or tri-stated as selected by the REG_GPIO_CFGy_GPIOnOUTCFG field. If the output is configured as push-pull, the pad will be driven with the corresponding bit in the REG_GPIO_WTy (y = A or B) Register. If the output is configured as open drain, the pad will be pulled low if the corresponding bit in the WTy Register is a 0, and will be floating if the corresponding bit in the WTy Register is a 1. If the output is configured as tri-state, the pad will be driven with the corresponding bit in the WTy Register if the corresponding bit in the REG_GPIO_ENy Register is a 1. If the bit in ENy is a 0, the output will be floating.

8.3.2 Reading from a GPIO Pad

All GPIO inputs are readable at all times, even if the pad is not configured as a GPIO. The current values of pads 0 to 31 are read in the REG_GPIO_RDA Register, and the current values of pads 32 to 49 are read in the REG_GPIO_RDB Register. If the REG_GPIO_CFGy_GPIOnINCFG bit is set for a GPIO, it will always read as zero.

©2017 Ambiq Micro, Inc.
All rights reserved.

8.3.3 Writing to a GPIO Pad

The GPIO pad outputs are controlled by the REG_GPIO_WTA/B Registers and the REG_GPIO_ENA/B Registers. Each of these registers may be directly written and read. Because each GPIO is often an independent function, the capability also exists to set or clear one or more bits without having to perform a read-modify-write operation. If the REG_GPIO_WTSA or REG_GPIO_WTSB Register is written, the corresponding bit in WTA/B will be set if the write data is 1, otherwise the WTA/B bit will not be changed. If the REG_GPIO_WTCA or REG_GPIO_WTCB Register is written, the corresponding bit in WTA/B will be cleared if the write data is 1, otherwise the WTA/B bit will not be changed.

If a GPIO pad is configured for tri-state output mode, the ENA/B Register controls the enabling of each bit. ENA and ENB may be directly written, and individual bits may be set or cleared by writing the ENSA/B or ENCA/B Registers with a 1 in the desired bit position.

8.3.4 GPIO Interrupts

Each GPIO pad can be configured to generate an interrupt on a high-to-low transition or a low-to-high transition, as selected by the REG_GPIO_CFGy_GPIOnINTD bit. This interrupt will be generated even if the pad is not configured as a GPIO in the Pad Configuration logic. Each interrupt is enabled, disabled, cleared or set with a standard set of Interrupt Registers GPIOA_IER, GPIOA_ISR, GPIOA_WCR and GPIOB_WSR for GPIO pads 0 to 31, and Registers GPIOB_IER, GPIOB_ISR, GPIOB_WCR and GPIOB_WSR for GPIO pads 32 to 49.

8.4 Pad Connection Summary

Figure 54 shows the detailed implementation of each pad. Each element will be described in detail.

8.4.1 Output Selection

There is multiplexer which selects the module signal to be driven to the output based on REG_GPIO_PADREGy_PADnFNCSEL field. This implements the multiplexing shown in Table 319 for output pads. For all pads, a PADnFNCSEL value of 0x3 selects the value in the corresponding GPIO_WTy register bit.

8.4.2 Output Control

The pad driver for each pad has a data input and an output enable input. Each of these controls is selected from among several alternatives based on the OUTDATSEL and OUTENSEL signals which are controlled by the selection of the output type as shown in Table 321 and Table 322.

OUTDATSEL normally selects the data from the output multiplexer, but if the pad is configured as Open Drain the data input is selected to be low.

©2017 Ambiq Micro, Inc.
All rights reserved.

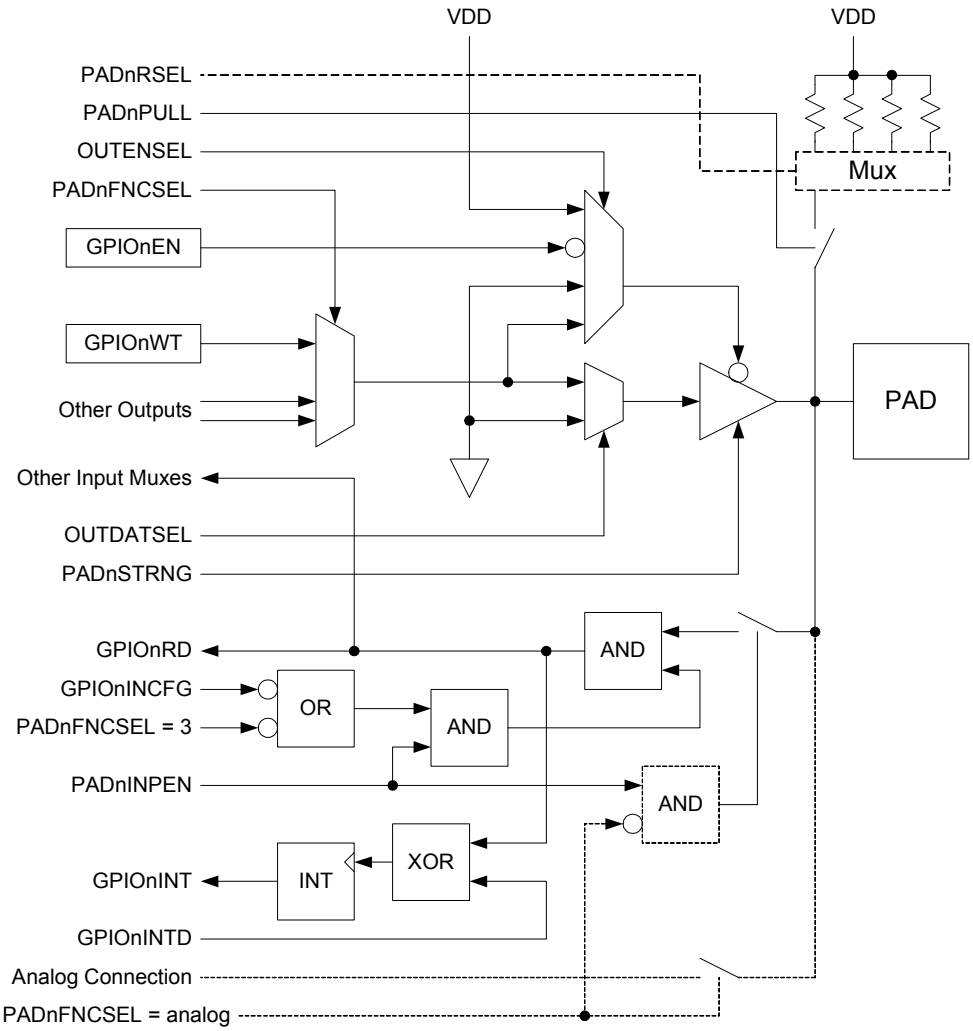


Figure 54. Pad Connection Details

OUTENSEL normally selects a ground signal to keep the pad driver enabled. If the pad is configured to be Open Drain, the pad enable is driven with the data from the output multiplexer. If the pad is configured as a GPIO (PADnFNCSEL = 0x3) and the GPIO drive type is tri-state (GPIOnOUTCFG = 0x3), the pad enable is driven with the inverse of the corresponding GPIOEN bit. If the pad is not configured as an output, the pad enable is forced high to turn the driver off.

The drive strength of each pad driver is configured as described in Section 8.2 on page 225.

©2017 Ambiq Micro, Inc.
All rights reserved.

8.4.3 Input Control

The input circuitry of the pad may be disabled by clearing the PADnINPEN bit. This configuration should always be set if the pad input is not being used, as it prevents unnecessary current consumption if the pad voltage happens to float to a level between VDD and Ground. If PADnINPEN is 0, the pad will always read as a 0.

If PADnINPEN is set, the pad input then goes to two places. It is driven to the selected module signal as selected in Table 319. In addition, the pad input can always be read from the GPIORD register unless the pad is configured as a GPIO (PADnFNCSEL = 0x3) and GPIOnINCFG is high, which will force the GPIORD input to be a zero. The ability to always read the pad value is very useful in some diagnostic cases.

The pad input is always sent to the GPIO interrupt logic, and a pad transition in the direction selected by GPIOnINTD will set the corresponding GPIOn_INT flip-flop. Note that this interrupt will be set even if the pad is not configured as a GPIO, which may be useful in detecting functions. As an example, this could be used to generate an interrupt when the I^2C/SPI Slave nCE signal is driven low by the Interface Host.

8.4.4 Pull-up Control

If PADnPULL is high, a pullup resistor is connected between the pad and VDDH, except for pad 20, where PADnPULL connects the resistor to VSS rather than VDDH.

The fourteen pads which can be I^2C/SPI Master output drivers (pads 0, 1, 5, 6, 8, 9, 25, 27, 39, 40, 42, 43 48 and 49) contain the additional circuitry shown with the dashed lines. In this case four different pullup resistors are selected by the PADnRSEL field.

8.4.5 Analog Pad Configuration

Pads which may have analog connections (pads 11-19, 29 and 31-35) include the circuitry shown with the dotted lines. If the pad is configured in analog mode (reference the analog input function selections in Table 1: Pin List and Function Table, the pad is connected directly to the particular analog module signal. In addition, OUTENSEL is forced high to disable the pad output, and the input of the pad is disabled independent of the value of PADnINPEN.

8.5 Module-specific Pad Configuration

The following sections describe in detail how to configure the pads for each module function.

8.5.1 Implementing IO Master Connections

The six IO Master modules must be correctly connected to the appropriate pads in order to operate.

8.5.1.1 IO Master 0 I^2C Connection

I^2C mode of IO Master 0 uses pad 5 as SCL and pad 6 as SDA. This mode is configured by setting the PADnFNCSEL fields as shown in Table 323. The PAD5INPEN and PAD6INPEN bits must be set. If the internal I^2C pullup resistors are to be used, PAD5PULL and PAD6PULL should be set, and the PAD5RSEL and PAD6RSEL fields should be set to select the desired pullup resistor size as shown in Table 322. If external pullup resistors are used, PAD5PULL and PAD6PULL should be cleared.

Table 323: IO Master 0 I^2C Configuration

Field	Value
PAD5FNCSEL	0

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 323: IO Master 0 I2C Configuration

Field	Value
PAD6FNCSEL	0

8.5.1.2 IO Master 1 I2C Connection

I2C mode of IO Master 1 uses pad 8 as SCL and pad 9 as SDA. This mode is configured by setting the PADnFNCSEL fields as shown in Table 324. The PAD8INPEN and PAD9INPEN bits must be set. If the internal I2C pullup resistors are to be used, PAD8PULL and PAD9PULL should be set, and the PAD8RSEL and PAD9RSEL fields should be set to select the desired pullup resistor size as shown in Table 322. If external pullup resistors are used, PAD8PULL and PAD9PULL should be cleared.

Table 324: IO Master 1 I2C Configuration

Field	Value
PAD8FNCSEL	0
PAD9FNCSEL	0

8.5.1.3 IO Master 2 I2C Connection

I2C mode of IO Master 2 uses pad 0 (or pad 27) as SCL and pad 1 (or pad 25) as SDA. This mode is configured by setting the PADnFNCSEL fields as shown in Table 325. The PAD0INPEN (or PAD27INPEN) and PAD1INPEN (or PAD25INPEN) bits must be set. If the internal I2C pullup resistors are to be used, PAD0PULL (or PAD27PULL) and PAD1PULL (or PAD25PULL) should be set, and the PAD0RSEL (or PAD27RSEL) and PAD1RSEL (or PAD25RSEL) fields should be set to select the desired pullup resistor size as shown in Table 322. If external pullup resistors are used, PAD0PULL (or PAD27PULL) and PAD1PULL (or PAD25PULL) should be cleared.

Table 325: IO Master 2 I2C Configuration

Field	Value
PAD0FNCSEL	7
PAD1FNCSEL	7
PAD27FNCSEL	4
PAD25FNCSEL	4

8.5.1.4 IO Master 3 I2C Connection

I2C mode of IO Master 3 uses pad 42 as SCL and pad 43 as SDA. This mode is configured by setting the PADnFNCSEL fields as shown in Table 326. The PAD42INPEN and PAD43INPEN bits must be set. If the internal I2C pullup resistors are to be used, PAD42PULL and PAD43PULL should be set, and the

©2017 Ambiq Micro, Inc.
All rights reserved.

PAD42RSEL and PAD43RSEL fields should be set to select the desired pullup resistor size as shown in Table 322. If external pullup resistors are used, PAD42PULL and PAD43PULL should be cleared.

Table 326: IO Master 3 I2C Configuration

Field	Value
PAD42FNCSEL	4
PAD43FNCSEL	4

8.5.1.5 IO Master 4 I2C Connection

I2C mode of IO Master 4 uses pad 39 as SCL and pad 40 as SDA. This mode is configured by setting the PADnFNCSEL fields as shown in Table 327. The PAD39INPEN and PAD40INPEN bits must be set. If the internal I2C pullup resistors are to be used, PAD39PULL and PAD40PULL should be set, and the PAD39RSEL and PAD40RSEL fields should be set to select the desired pullup resistor size as shown in Table 322. If external pullup resistors are used, PAD39PULL and PAD40PULL should be cleared.

Table 327: IO Master 4 I2C Configuration

Field	Value
PAD39FNCSEL	4
PAD40FNCSEL	4

8.5.1.6 IO Master 5 I2C Connection

I2C mode of IO Master 5 uses pad 48 as SCL and pad 49 as SDA. This mode is configured by setting the PADnFNCSEL fields as shown in Table 328. The PAD48INPEN and PAD49INPEN bits must be set. If the internal I2C pullup resistors are to be used, PAD48PULL and PAD49PULL should be set, and the PAD48RSEL and PAD49RSEL fields should be set to select the desired pullup resistor size as shown in Table 322. If external pullup resistors are used, PAD48PULL and PAD49PULL should be cleared.

Table 328: IO Master 5 I2C Configuration

Field	Value
PAD48FNCSEL	4
PAD49FNCSEL	4

8.5.1.7 High Speed IO Master 0 4-wire SPI Connection

Four-wire SPI mode of IO Master 0 uses pad 5 as SCK, pad 6 as MISO and pad 7 as MOSI. This mode is configured by setting the PADnFNCSEL fields as shown in Table 329. The PAD5INPEN and PAD6INPEN bits must be set. PAD5PULL, PAD6PULL and PAD7PULL should be cleared.

Table 329: IO Master 0 4-wire SPI Configuration

Field	Value
PAD5FNCSEL	1
PAD6FNCSEL	1
PAD7FNCSEL	1

©2017 Ambiq Micro, Inc.
All rights reserved.

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 330. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 330: IO Master 0 4-wire SPI nCE Configuration

Field	Value	nCE Selection	Pad Used
PAD11FNCSEL	1	0	11
PAD42FNCSEL	1	0	42
PAD17FNCSEL	1	1	17
PAD24FNCSEL	1	1	24
PAD18FNCSEL	1	2	18
PAD44FNCSEL	1	2	44
PAD19FNCSEL	1	3	19
PAD45FNCSEL	1	3	45
PAD8FNCSEL	2	4	8
PAD16FNCSEL	1	4	16
PAD46FNCSEL	1	4	46
PAD4FNCSEL	2	5	4
PAD9FNCSEL	2	5	9
PAD47FNCSEL	1	5	47
PAD10FNCSEL	2	6	10
PAD48FNCSEL	1	6	48
PAD49FNCSEL	1	7	49

8.5.1.8 IO Master 1 4-wire SPI Connection

Four-wire SPI mode of IO Master 1 uses pad 8 as SCK, pad 9 as MISO and pad 10 as MOSI. This mode is configured by setting the PADnFNCSEL fields as shown in Table 331. The PAD8INPEN and PAD9INPEN bits must be set. PAD8PULL, PAD9PULL and PAD10PULL should be cleared.

Table 331: IO Master 1 4-wire SPI Configuration

Field	Value
PAD8FNCSEL	1
PAD9FNCSEL	1
PAD10FNCSEL	1

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 332. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

Table 332: IO Master 1 4-wire SPI nCE Configuration

Field	Value	nCE Selection	Pad Used
PAD6FNCSEL	5	0	6
PAD12FNCSEL	1	0	12
PAD35FNCSEL	1	0	35
PAD7FNCSEL	7	1	7
PAD13FNCSEL	1	1	13

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 332: IO Master 1 4-wire SPI nCE Configuration

Field	Value	nCE Selection	Pad Used
PAD36FNCSEL	1	1	36
PAD5FNCSEL	7	2	5
PAD14FNCSEL	1	2	14
PAD15FNCSEL	1	3	15
PAD3FNCSEL	2	4	3
PAD20FNCSEL	1	5	20
PAD21FNCSEL	1	6	21
PAD29FNCSEL	1	6	29
PAD22FNCSEL	1	7	22
PAD30FNCSEL	1	7	30

8.5.1.9 IO Master 2 4-wire SPI Connection

Four-wire SPI mode of IO Master 2 uses pad 0 (or pad 27) as SCK, pad 2 (or pad 28) as MISO and pad 1 (pad 25) as MOSI. This mode is configured by setting the PADnFNCSEL fields as shown in Table 333. The PAD0INPEN and PAD2INPEN bits must be set. PAD0PULL, PAD2PULL and PAD1PULL should be cleared.

Table 333: IO Master 2 4-wire SPI Configuration

Field	Value
PAD0FNCSEL	5
PAD27FNCSEL	5
PAD2FNCSEL	5
PAD28FNCSEL	5
PAD1FNCSEL	5
PAD25FNCSEL	5

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 334. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

Table 334: IO Master 2 4-wire SPI nCE Configuration

Field	Value	nCE Selection	Pad Used
PAD3FNCSEL	5	0	3
PAD14FNCSEL	4	1	14
PAD24FNCSEL	0	1	24
PAD41FNCSEL	0	1	41
PAD15FNCSEL	4	2	15
PAD42FNCSEL	0	2	42
PAD13FNCSEL	4	3	13
PAD16FNCSEL	4	3	16

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 334: IO Master 2 4-wire SPI nCE Configuration

Field	Value	nCE Selection	Pad Used
PAD8FNCSEL	4	4	8
PAD4FNCSEL	5	5	4
PAD47FNCSEL	0	5	47
PAD10FNCSEL	4	6	10
PAD48FNCSEL	0	6	48
PAD11FNCSEL	4	7	11
PAD49FNCSEL	0	7	49

8.5.1.10 High Speed IO Master 4 4-wire SPI Connection

Four-wire SPI mode of IO Master 4 uses pad 39 as SCK, pad 40 as MISO and pad 44 as MOSI. This mode is configured by setting the PADnFNCSEL fields as shown in Table 335. The PAD39INPEN and PAD44INPEN bits must be set. PAD39PULL, PAD40PULL and PAD44PULL should be cleared.

Table 335: IO Master 4 4-wire SPI Configuration

Field	Value
PAD39FNCSEL	5
PAD40FNCSEL	5
PAD44FNCSEL	5

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 336. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

Table 336: IO Master 4 4-wire SPI nCE Configuration

Field	Value	nCE Selection	Pad Used
PAD29FNCSEL	6	0	29
PAD18FNCSEL	4	1	18
PAD41FNCSEL	6	2	41
PAD17FNCSEL	4	3	17
PAD45FNCSEL	4	3	45
PAD10FNCSEL	6	4	10
PAD46FNCSEL	6	4	46
PAD9FNCSEL	4	5	9
PAD47FNCSEL	6	5	47
PAD35FNCSEL	4	6	35

©2017 Ambiq Micro, Inc.
All rights reserved.

8.5.1.11 IO Master 5 4-wire SPI Connection

Four-wire SPI mode of IO Master 5 uses pad 48 as SCK, pad 49 as MISO and pad 47 as MOSI. This mode is configured by setting the PADnFNCSEL fields as shown in Table 337. The PAD48INPEN and PAD47INPEN bits must be set. PAD48PULL, PAD49PULL and PAD47PULL should be cleared.

Table 337: IO Master 5 4-wire SPI Configuration

Field	Value
PAD48FNCSEL	5
PAD49FNCSEL	5
PAD47FNCSEL	5

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 338. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

Table 338: IO Master 5 4-wire SPI nCE Configuration

Field	Value	nCE Selection	Pad Used
PAD24FNCSEL	4	0	24
PAD46FNCSEL	5	4	46
PAD45FNCSEL	6	5	45
PAD44FNCSEL	6	6	44
PAD41FNCSEL	5	7	41

8.5.1.12 High Speed IO Master 0 3-wire SPI Connection

Three-wire SPI mode of IO Master 0 uses pad 5 as SCK and pad 7 as MOSI/MISO. This mode is configured by setting the PADnFNCSEL fields as shown in Table 339. The PAD5INPEN and PAD7INPEN bits must be set. PAD5PULL and PAD7PULL should be cleared. Pad 6 may be used for other functions.

Table 339: IO Master 0 3-wire SPI Configuration

Field	Value
PAD5FNCSEL	1
PAD7FNCSEL	0

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 330. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

8.5.1.13 IO Master 1 3-wire SPI Connection

Three-wire SPI mode of IO Master 1 uses pad 8 as SCK and pad 10 as MOSI/MISO. This mode is configured by setting the PADnFNCSEL fields as shown in Table 340. The PAD8INPEN and PAD10INPEN bits must be set. PAD8PULL and PAD10PULL should be cleared. Pad 9 may be used for other functions.

Table 340: IO Master 1 3-wire SPI Configuration

Field	Value
PAD8FNCSEL	1

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 340: IO Master 1 3-wire SPI Configuration

Field	Value
PAD10FNCSEL	0

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 332. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

8.5.1.14 IO Master 2 3-wire SPI Connection

Three-wire SPI mode of IO Master 2 uses pad 0 (or pad 27) as SCK and pad 2 (or pad 28) as MOSI/MISO. This mode is configured by setting the PADnFNCSEL fields as shown in Table 341. The PAD0INPEN (or PAD27INPEN) and PAD2INPEN (or PAD28INPEN) bits must be set. PAD0PULL (or PAD27PULL) and PAD2PULL (or PAD28PULL) should be cleared. Pad 1 or Pad 25 may be used for other functions.

Table 341: IO Master 2 3-wire SPI Configuration

Field	Value
PAD0FNCSEL	5
PAD27FNCSEL	5
PAD2FNCSEL	7
PAD28FNCSEL	4

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 334. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

8.5.1.15 IO Master 3 3-wire SPI Connection

Three-wire SPI mode of IO Master 3 uses pad 42 as SCK and pad 38 as MOSI/MISO. This mode is configured by setting the PADnFNCSEL fields as shown in Table 342. The PAD42INPEN and PAD38INPEN bits must be set. PAD42PULL and PAD38PULL should be cleared. Pad 43 may be used for other functions.

Table 342: IO Master 3 3-wire SPI Configuration

Field	Value
PAD42FNCSEL	5
PAD38FNCSEL	4

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 340. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

8.5.1.16 High Speed IO Master 4 3-wire SPI Connection

Three-wire SPI mode of IO Master 4 uses pad 39 as SCK and pad 44 as MOSI/MISO. This mode is configured by setting the PADnFNCSEL fields as shown in Table 343. The PAD39INPEN and

©2017 Ambiq Micro, Inc.
All rights reserved.

PAD44INPEN bits must be set. PAD39PULL and PAD44PULL should be cleared. Pad 40 may be used for other functions.

Table 343: IO Master 4 3-wire SPI Configuration

Field	Value
PAD39FNCSEL	5
PAD44FNCSEL	4

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 336. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

8.5.1.17 IO Master 5 3-wire SPI Connection

Three-wire SPI mode of IO Master 5 uses pad 48 as SCK and pad 47 as MOSI/MISO. This mode is configured by setting the PADnFNCSEL fields as shown in Table 344. The PAD48INPEN and PAD47INPEN bits must be set. PAD48PULL and PAD47PULL should be cleared. Pad 49 may be used for other functions.

Table 344: IO Master 5 3-wire SPI Configuration

Field	Value
PAD48FNCSEL	5
PAD47FNCSEL	4

A variety of pads may be used for up to eight nCE signals to select up to eight separate slaves, as shown in Table 338. The PADnINPEN and PADnPULL bits of any pad used for nCE should be cleared.

8.5.1.18 SPI Flow Control Connections

SPI Flow Control in interrupt mode requires an external pin to be specified as the interrupt pin. This is accomplished by configuring the desired pin in the IOMxIRQ register (x = 0 to 5).

8.5.2 Implementing IO Slave Connections

The IO Master module must be correctly connected to the appropriate pads in order to operate.

8.5.2.1 IO Slave I^2C Connection

I^2C mode of the IO Slave uses pad 0 as SCL and pad 1 as SDA. This mode is configured by setting the PADnFNCSEL fields as shown in Table 345. The PAD0INPEN and PAD1INPEN bits must be set. PAD0PULL and PAD1PULL should be cleared.

Table 345: IO Slave I^2C Configuration

Field	Value
PAD0FNCSEL	0
PAD1FNCSEL	0

©2017 Ambiq Micro, Inc.
All rights reserved.

8.5.2.2 IO Slave 4-wire SPI Connection

Four-wire SPI mode of the IO Slave uses pad 0 as SCK, pad 1 as MISO, pad 2 as MOSI and pad 3 as nCE. This mode is configured by setting the PADnFNCSEL fields as shown in Table 346. The PAD0INPEN, PAD2INPEN and PAD3INPEN bits must be set. PAD0PULL, PAD1PULL, PAD2PULL and PAD3PULL should be cleared.

Table 346: IO Slave 4-wire SPI Configuration

Field	Value
PAD0FNCSEL	1
PAD1FNCSEL	1
PAD2FNCSEL	1
PAD3FNCSEL	1

8.5.2.3 IO Slave 3-wire SPI Connection

Three-wire SPI mode of the IO Slave uses pad 0 as SCK, pad 2 as MISO/MOSI and pad 3 as nCE. This mode is configured by setting the PADnFNCSEL fields as shown in Table 347. The PAD0INPEN, PAD2INPEN and PAD3INPEN bits must be set. PAD0PULL, PAD2PULL and PAD3PULL should be cleared. Pad 1 may be used for other functions.

Table 347: IO Slave 3-wire SPI Configuration

Field	Value
PAD0FNCSEL	1
PAD2FNCSEL	0
PAD3FNCSEL	1

8.5.2.4 IO Slave Interrupt Connection

The IO Slave can be configured to generate an interrupt output under a variety of internal conditions. If this function is used, the interrupt will be generated on pad 4. PAD4FNCSEL must be set to 1, and PAD4INPEN and PAD4PULL should be cleared.

8.5.2.5 Implementing Internal I^2C and SPI Loopback

Loopback involves connecting one of the 6 I2C/SPI Masters to the I2C/SPI Slave. In order to make this connection, two configurations are required, some of which are specific to the functional mode selected (I2C, 3-wire SPI or 4-wire SPI). In all cases, the LOOPBACK register must be loaded with the value to select the desired I2C/SPI Master (0 through 5).

8.5.2.5.1 I^2C Loopback

The Slave is configured in I2C loopback mode by setting PAD0FNCSEL to 6 (MxSCLLB) and by setting PAD1FNCSEL to 6 (MxSDALB). The selected Master is configured as shown in the table below.

Table 348: I^2C Loopback

Master	PADxFNCSEL	Value	PADxFNCSEL	Value
0	PAD5FNCSEL	6	PAD6FNCSEL	6

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 348: I²C Loopback

Master	PADxFNCSEL	Value	PADxFNCSEL	Value
1	PAD8FNCSEL	7	PAD9FNCSEL	7
2	PAD27FNCSEL	7	PAD25FNCSEL	7
4	PAD39FNCSEL	7	PAD40FNCSEL	7
5	PAD48FNCSEL	7	PAD49FNCSEL	7

8.5.2.5.2 3-wire SPI Loopback

The Slave is configured in 3-wire SPI loopback mode by setting PAD0FNCSEL to 4 (MxSCKLB), setting PAD2FNCSEL to 6 (MxWIR3LB) and setting PAD3FNCSEL to 4 (MxnCELB). The selected Master is configured as shown in the table below. Note that the SPI Channel selection is not relevant, as any of the eight Channels will loop nCE back to the Slave.

Table 349: 3-wire SPI Loopback

Master	PADxFNCSEL	Value	PADxFNCSEL	Value
0	PAD5FNCSEL	4	PAD7FNCSEL	6
1	PAD8FNCSEL	5	PAD10FNCSEL	7
2	PAD27FNCSEL	6	PAD28FNCSEL	7
4	PAD39FNCSEL	6	PAD44FNCSEL	7
5	PAD48FNCSEL	6	PAD47FNCSEL	7

8.5.2.5.3 4-wire SPI Loopback

The Slave is configured in 4-wire SPI loopback mode by setting PAD0FNCSEL to 4 (MxSCKLB), setting PAD1FNCSEL to 4 (MxMISOLB)), setting PAD2FNCSEL to 4 (MxMOSILB) and setting PAD3FNCSEL to 4 (MxnCELB). The selected Master is configured as shown in the table below. Note that the SPI Channel selection is not relevant, as any of the eight Channels will loop nCE back to the Slave.

Table 350: 4-wire SPI Loopback

Master	PADxFNCSEL	Value	PADxFNCSEL	Value
0	**PAD5FNCSEL**	4	PAD6FNCSEL	4
1	**PAD8FNCSEL**	5	PAD9FNCSEL	5
2	**PAD27FNCSEL**	6	PAD25FNC-SEL	6
4	**PAD39FNCSEL**	6	PAD40FNC-SEL	6
5	**PAD48FNCSEL**	6	PAD49FNC-SEL	6

8.5.2.6 Loopback of the I2C/SPI Slave Interrupt

The I2C/SPI Slave interrupt can be exercised in loopback mode by setting PAD4FNCSEL to 4. This will cause the slave interrupt to be driven into the GPIO4 pin where it can be checked by software.

©2017 Ambiq Micro, Inc.
All rights reserved.

8.5.3 Implementing Counter/Timer Connections

Each Counter/Timer can optionally count pulses from an input pad, or generate pulses on an output pad. Table 351 shows the PADnFNCSEL settings to connect each Counter/Timer to the appropriate pad. If the pad is used as an input, the PADnINPEN bit should be set, otherwise it should be cleared. The PADnPULL bit may be set if the input signal is open drain.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 351: Counter/Timer Pad Configuration

Field	Value	Ctr/Timer	Pad
PAD12FNCSEL	2	A0	12
PAD42FNCSEL	2	A0	42
PAD13FNCSEL	2	B0	13
PAD18FNCSEL	2	A1	18
PAD19FNCSEL	4	A1	19
PAD24FNCSEL	5	A1	24
PAD35FNCSEL	5	A1	35
PAD44FNCSEL	2	A1	44
PAD45FNCSEL	7	A1	45
PAD46FNCSEL	4	A1	46
PAD19FNCSEL	2	B1	19
PAD22FNCSEL	6	B1	22
PAD23FNCSEL	6	B1	22
PAD45FNCSEL	2	B1	45
PAD20FNCSEL	2	A2	20
PAD29FNCSEL	2	A2	29
PAD46FNCSEL	2	A2	46
PAD21FNCSEL	2	B2	21
PAD30FNCSEL	2	B2	30
PAD47FNCSEL	2	B2	47
PAD22FNCSEL	2	A3	22
PAD48FNCSEL	2	A3	48
PAD49FNCSEL	2	B3	49

8.5.4 Implementing UART Connections

The UART signals can be connected to a variety of pads.

8.5.4.1 UART0 TX/RX Connections

The UART data signals TX and RX may each be connected to several pads. Note that TX and RX are selected independently. Table 352 shows the connections for TX, which should have the corresponding PADnINPEN and PADnPULL bits clear. Table 353 shows the connections for RX, which must have the corresponding PADnINPEN bit set and should have the corresponding PADnPULL bit clear.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 352: UART0 TX Configuration

Field	Value	Pad
PAD1FNCSEL	2	1
PAD7FNCSEL	5	7
PAD16FNCSEL	6	16
PAD20FNCSEL	4	20
PAD22FNCSEL	0	22
PAD30FNCSEL	4	30
PAD39FNCSEL	0	39

Table 353: UART0 RX Configuration

Field	Value	Pad
PAD2FNCSEL	2	2
PAD11FNCSEL	6	11
PAD17FNCSEL	6	17
PAD21FNCSEL	4	21
PAD40FNCSEL	0	40

8.5.4.2 UART0 RTS/CTS Connections

The UART modem control signals RTS and CTS may each be connected to one of two pads. Note that RTS and CTS are selected independently. Table 354 shows the connections for RTS, which should have the corresponding PADnINPEN and PADnPULL bits clear. Table 355 shows the connections for CTS, which must have the corresponding PADnINPEN bit set and should have the corresponding PADnPULL bit clear.

Table 354: UART0 RTS Configuration

Field	Value	Pad
PAD3FNCSEL	0	3
PAD5FNCSEL	2	5
PAD13FNCSEL	6	13
PAD35FNCSEL	6	35
PAD41FNCSEL	7	41

Table 355: UART0 CTS Configuration

Field	Value	Pad
PAD4FNCSEL	0	4
PAD6FNCSEL	2	6
PAD12FNCSEL	6	12

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 355: UART0 CTS Configuration

Field	Value	Pad
PAD29FNCSEL	4	29
PAD36FNCSEL	6	36

8.5.4.3 UART1 TX/RX Connections

The UART data signals TX and RX may each be connected to several pads. Note that TX and RX are selected independently. Table 352 shows the connections for TX, which should have the corresponding PADnINPEN and PADnPULL bits clear. Table 353 shows the connections for RX, which must have the corresponding PADnINPEN bit set and should have the corresponding PADnPULL bit clear.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 356: UART1 TX Configuration

Field	Value	Pad
PAD8FNCSEL	6	8
PAD12FNCSEL	7	12
PAD14FNCSEL	2	14
PAD18FNCSEL	6	18
PAD20FNCSEL	5	20
PAD35FNCSEL	2	35
PAD39FNCSEL	1	39

Table 357: UART1 RX Configuration

Field	Value	Pad
PAD9FNCSEL	6	9
PAD13FNCSEL	7	13
PAD15FNCSEL	2	15
PAD19FNCSEL	6	19
PAD21FNCSEL	5	21
PAD36FNCSEL	2	36
PAD40FNCSEL	1	40

8.5.4.4 UART1 RTS/CTS Connections

The UART modem control signals RTS and CTS may each be connected to one of two pads. Note that RTS and CTS are selected independently. Table 354 shows the connections for RTS, which should have the corresponding PADnINPEN and PADnPULL bits clear. Table 355 shows the connections for CTS, which must have the corresponding PADnINPEN bit set and should have the corresponding PADnPULL bit clear.

Table 358: UART1 RTS Configuration

Field	Value	Pad
PAD10FNCSEL	5	10
PAD16FNCSEL	7	16
PAD30FNCSEL	5	30
PAD44FNCSEL	0	44

Table 359: UART1 CTS Configuration

Field	Value	Pad
PAD11FNCSEL	5	11
PAD17FNCSEL	7	17
PAD29FNCSEL	5	29
PAD45FNCSEL	0	45

©2017 Ambiq Micro, Inc.
All rights reserved.

8.5.5 Implementing Audio Connections

The Audio signals can be connected to a variety of pads.

8.5.5.1 PDM Connections

The PDM CLK and DATA signals may each be connected to several pads. Note that CLK and DATA are selected independently. Table 360 shows the connections for PDM CLK, which should have the corresponding PADnINPEN and PADnPULL bits clear. Table 361 shows the connections for PDM DATA, which must have the corresponding PADnINPEN bit set and should have the corresponding PADnPULL bit clear.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 360: PDM CLK Configuration

Field	Value	Pad
PAD12FNCSEL	5	12
PAD22FNCSEL	4	22

Table 361: PDM DATA Configuration

Field	Value	Pad
PAD11FNCSEL	7	11

8.5.5.2 I2S Connections

The I2S BCLK, WCLK and DAT signals may each be connected to several pads. Note that BCLK, WCLK and DAT are selected independently. Table 362 shows the connections for PDM BCLK, which should have the corresponding PADnINPEN and PADnPULL bits clear. Table 362 shows the connections for PDM WCLK, which should have the corresponding PADnINPEN and PADnPULL bits clear. Table 364 shows the connections for PDM DAT, which must have the corresponding PADnINPEN bit set and should have the corresponding PADnPULL bit clear.

Table 362: I2S BCLK Configuration

Field	Value	Pad
PAD19FNCSEL	7	19
PAD24FNCSEL	6	24

Table 363: I2S WCLK Configuration

Field	Value	Pad
PAD3FNCSEL	7	3

Table 364: I2S DAT Configuration

Field	Value	Pad
PAD6FNCSEL	7	6
PAD30FNCSEL	7	30

8.5.6 Implementing GPIO Connections

Each pad of the Apollo2 Blue can be configured as a GPIO port by setting PADnFNCSEL to 3. PADnINPEN and PADnPULL must be set appropriately depending on the specific GPIO function.

©2017 Ambiq Micro, Inc.
All rights reserved.

8.5.7 Implementing CLKOUT Connections

The flexible clock output of the Clock Generator module, CLKOUT, may be configured on several pads as shown in Table 365. PADnINPEN and PADnPULL should be cleared in each case.

Table 365: CLKOUT Configuration

Field	Value	Pad
PAD0FNCSEL	2	0
PAD4FNCSEL	6	4
PAD7FNCSEL	2	7
PAD11FNCSEL	2	11
PAD12FNCSEL	4	12
PAD24FNCSEL	2	24
PAD39FNCSEL	2	39
PAD41FNCSEL	1	41

8.5.8 Implementing 32kHz CLKOUT Connections

In addition to the CLKOUT mux output, there is also a dedicated 32 kHz clock output. This clock is primarily for leveraging the 32 kHz oscillator clock from Apollo2 Blue . This clock output may be configured on several pads as shown in Table 366. PADnINPEN and PADnPULL should be cleared in each case.

Table 366: 32kHz CLKOUT Configuration

Field	Value	Pad
PAD4FNCSEL	7	4
PAD14FNCSEL	7	14
PAD18FNCSEL	7	18
PAD36FNCSEL	4	36
PAD46FNCSEL	0	46

8.5.9 Implementing ADC Connections

Three types of pad connections may be made for the ADC module. Up to six pads may be configured as the analog inputs, as shown in Table 367. The ADCREF reference voltage input is supplied on a dedicated input pin. If an external digital trigger is desired, up to fourtwo selectable pad choices may be configured, as shown in Table 368. For the trigger inputs, PADnINPEN must be set. For other inputs, PADnINPEN should be cleared. PADnPULL should be cleared except in the case of an open drain trigger input.

Table 367: ADC Analog Input Configuration

Field	Value	Input	Pad
PAD16FNCSEL	0	ADCSE0	16
PAD29FNCSEL	0	ADCSE1	29
PAD11FNCSEL	0	ADCSE2	11
PAD35FNCSEL	0	ADCSE7	35
PAD13FNCSEL	0	ADCD0M/ SE8	13

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 367: ADC Analog Input Configuration

Field	Value	Input	Pad
PAD12FNCSEL	0	ADCD0P/ SE9	12
PAD14FNCSEL	0	ADCD1P	14
PAD15FNCSEL	0	ADCD1M	15

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 368: ADC Trigger Input Configuration

Field	Value	Input	Pad
PAD7FNCSEL	4	TRIG0	7
PAD16FNCSEL	2	TRIG0	16
PAD40FNCSEL	2	TRIG0	40
PAD3FNCSEL	6	TRIG1	3
PAD17FNCSEL	2	TRIG1	17
PAD36FNCSEL	0	TRIG1	36

8.5.10 Implementing Voltage Comparator Connections

Two types of pad connections may be made for the Voltage Comparator (VCOMP) module. Three reference voltages may be used for the comparator negative input as shown in Table 369. The voltage to be applied to the comparator positive input are shown in Table 370. In each case PADnINPEN and PADnPULL should be cleared. Note that for CMPRF2, this pin is muxed with ADCSE6 allowing for the same reference input to be used for both ADC and VCOMP operations. Additionally, CMPIN0 is muxed with ADCSE0 allowing for the same input to be used for both ADC and VCOMP operations.

NOTE: if voltage comparator and ADC operation are concurrently sampling the CMPIN0/ADCSE0 input, quality of the sample may be degraded and cannot be guaranteed. It is recommended that voltage comparator and ADC operations are sampled independently (time sliced) to avoid any signal quality loss.

Table 369: Voltage Comparator Reference Configuration

Field	Value	Input	Pad
PAD19FNCSEL	0	CMPRF0	19
PAD17FNCSEL	0	CMPRF1	17

Table 370: Voltage Comparator Input Configuration

Field	Value	Input	Pad
PAD16FNCSEL	5	CMPIN0	16
PAD18FNCSEL	0	CMPIN1	18

8.5.11 Implementing the Software Debug Port Connections

The software debug clock (SWDCK) and data (SWDIO) must be connected on pads 20 and 21 respectively. PAD20FNCSEL and PAD21FNCSEL must be set to 0, PAD20INPEN and PAD21INPEN must be set, and PAD20PULL and PAD21PULL must be set, which results in a default state of SWDCK low and SWDIO high. Pads 14 and 15 can alternatively be used for SWDCK and SWDIO functionality, respectively. These pads are, however, not selected by default. Using pads 14 and 15 requires PAD14FNCSEL to be set to 6 and PAD15FNCSEL to be set to 6, PAD14INPEN and PAD15INPEN to be set, and PAD14PULL

©2017 Ambiq Micro, Inc.
All rights reserved.

and PAD15PULL to be set. The optional continuous output signal SWO may be configured on a variety of pads as shown in Table 371, and PADnINPEN and PADnPULL should be cleared for the selected pad.

Table 371: SWO Configuration

Field	Value	Pad
PAD15FNCSEL	7	15
PAD22FNCSEL	7	22
PAD24FNCSEL	7	24
PAD30FNCSEL	6	30
PAD41FNCSEL	2	41
PAD45FNCSEL	7	45
PAD46FNCSEL	7	46

8.6 GPIO Registers

General Purpose IO

INSTANCE 0 BASE ADDRESS:0x40010000

This is the detailed description of the general purpose I/O (GPIO) block, as well as for the PAD multiplexor. Note that GPIO interrupt bits are edge triggered. WARNING: if an interrupt bit is cleared while the combination of polarity and input are still asserted then this bit will not set again.

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.1 Register Memory Map

Table 372: GPIO Register Map

Address(s)	Register Name	Description
0x40010000	PADREGA	Pad Configuration Register A
0x40010004	PADREGB	Pad Configuration Register B
0x40010008	PADREGC	Pad Configuration Register C
0x4001000C	PADREGD	Pad Configuration Register D
0x40010010	PADREGE	Pad Configuration Register E
0x40010014	PADREGF	Pad Configuration Register F
0x40010018	PADREGG	Pad Configuration Register G
0x4001001C	PADREGH	Pad Configuration Register H
0x40010024	PADREGJ	Pad Configuration Register J
0x40010028	PADREGK	Pad Configuration Register K
0x4001002C	PADREGL	Pad Configuration Register L
0x40010030	PADREGM	Pad Configuration Register M
0x40010040	CFGA	GPIO Configuration Register A
0x40010044	CFGB	GPIO Configuration Register B
0x40010048	CFGC	GPIO Configuration Register C
0x4001004C	CFGD	GPIO Configuration Register D
0x40010050	CFGE	GPIO Configuration Register E
0x40010054	CFGF	GPIO Configuration Register F
0x40010060	PADKEY	Key Register for all pad configuration registers
0x40010080	RDA	GPIO Input Register A
0x40010084	RDB	GPIO Input Register B
0x40010088	WTA	GPIO Output Register A
0x4001008C	WTB	GPIO Output Register B
0x40010090	WTSA	GPIO Output Register A Set
0x40010094	WTSB	GPIO Output Register B Set
0x40010098	WTCA	GPIO Output Register A Clear
0x4001009C	WTCB	GPIO Output Register B Clear
0x400100A0	ENA	GPIO Enable Register A
0x400100A4	ENB	GPIO Enable Register B
0x400100A8	ENSA	GPIO Enable Register A Set
0x400100AC	ENSB	GPIO Enable Register B Set
0x400100B4	ENCA	GPIO Enable Register A Clear
0x400100B8	ENCB	GPIO Enable Register B Clear
0x400100BC	STMRCAP	STIMER Capture Control
0x400100C0	IOM0IRQ	IOM0 Flow Control IRQ Select
0x400100C4	IOM1IRQ	IOM1 Flow Control IRQ Select

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 372: GPIO Register Map

Address(s)	Register Name	Description
0x400100C8	IOM2IRQ	IOM2 Flow Control IRQ Select
0x400100CC	IOM3IRQ	IOM3 Flow Control IRQ Select
0x400100D0	IOM4IRQ	IOM4 Flow Control IRQ Select
0x400100D4	IOM5IRQ	IOM5 Flow Control IRQ Select
0x400100D8	LOOPBACK	IOM to IOS Loopback Control
0x400100DC	GPIOOBS	GPIO Observation Mode Sample register
0x400100E0	ALTPADCFGA	Alternate Pad Configuration reg0 (Pads 3,2,1,0)
0x400100E4	ALTPADCFGB	Alternate Pad Configuration reg1 (Pads 7,6,5,4)
0x400100E8	ALTPADCFGC	Alternate Pad Configuration reg2 (Pads 11,10,9,8)
0x400100EC	ALTPADCFGD	Alternate Pad Configuration reg3 (Pads 15,14,13,12)
0x400100F0	ALTPADCFGE	Alternate Pad Configuration reg4 (Pads 19,18,17,16)
0x400100F4	ALTPADCFGF	Alternate Pad Configuration reg5 (Pads 23,22,21,20)
0x400100F8	ALTPADCFGG	Alternate Pad Configuration reg6 (Pads 27,26,25,24)
0x400100FC	ALTPADCFGH	Alternate Pad Configuration reg7 (Pads 31,30,29,28)
0x40010100	ALTPADCFGI	Alternate Pad Configuration reg8 (Pads 35,34,33,32)
0x40010104	ALTPADCFGJ	Alternate Pad Configuration reg9 (Pads 39,38,37,36)
0x40010108	ALTPADCFGK	Alternate Pad Configuration reg10 (Pads 43,42,41,40)
0x4001010C	ALTPADCFGL	Alternate Pad Configuration reg11 (Pads 47,46,45,44)
0x40010110	ALTPADCFGM	Alternate Pad Configuration reg12 (Pads 49,48)
0x40010200	INT0EN	GPIO Interrupt Registers 31-0: Enable
0x40010204	INT0STAT	GPIO Interrupt Registers 31-0: Status
0x40010208	INT0CLR	GPIO Interrupt Registers 31-0: Clear
0x4001020C	INT0SET	GPIO Interrupt Registers 31-0: Set
0x40010210	INT1EN	GPIO Interrupt Registers 49-32: Enable
0x40010214	INT1STAT	GPIO Interrupt Registers 49-32: Status
0x40010218	INT1CLR	GPIO Interrupt Registers 49-32: Clear
0x4001021C	INT1SET	GPIO Interrupt Registers 49-32: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2 GPIO Registers

8.6.2.1 PADREGA Register

Pad Configuration Register A

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x40010000

This register controls the pad configuration controls for PAD3 through PAD0. Writes to this register must be unlocked by the PADKEY register.

Table 373: PADREGA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		PAD3FNCSEL			PAD3STRNG	PAD3INPEN	PAD3PULL	RSVD		PAD2FNCSEL			PAD2STRNG	PAD2INPEN	PAD2PULL	PAD1RSEL		PAD1FNCSEL			PAD1STRNG	PAD1INPEN	PAD1PULL	PAD0RSEL		PAD0FNCSEL			PAD0STRNG	PAD0INPEN	PAD0PULL

Table 374: PADREGA Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:27	PAD3FNCSEL	0x3	RW	Pad 3 function select UA0RTS = 0x0 - Configure as the UART0 RTS output SLnCE = 0x1 - Configure as the IOSLAVE SPI nCE signal M1nCE4 = 0x2 - Configure as the SPI channel 4 nCE signal from IOMSTR1 GPIO3 = 0x3 - Configure as GPIO3 MxnCELB = 0x4 - Configure as the IOSLAVE SPI nCE loopback signal from IOMSTRx M2nCE0 = 0x5 - Configure as the SPI channel 0 nCE signal from IOMSTR2 TRIG1 = 0x6 - Configure as the ADC Trigger 1 signal I2S_WCLK = 0x7 - Configure as the PDM I2S Word Clock input
26	PAD3STRNG	0x0	RW	Pad 3 drive strength. LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
25	PAD3INPEN	0x0	RW	Pad 3 input enable. DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
24	PAD3PULL	0x0	RW	Pad 3 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
23:22	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 374: PADREGA Register Bits

Bit	Name	Reset	RW	Description
21:19	PAD2FNCSEL	0x3	RW	Pad 2 function select SLWIR3 = 0x0 - Configure as the IOSLAVE SPI 3-wire MOSI/MISO signal SLMOSI = 0x1 - Configure as the IOSLAVE SPI MOSI signal UART0RX = 0x2 - Configure as the UART0 RX input GPIO2 = 0x3 - Configure as GPIO2 MxMOSILB = 0x4 - Configure as the IOSLAVE SPI MOSI loopback signal from IOMSTRx M2MOSI = 0x5 - Configure as the IOMSTR2 SPI MOSI output signal MxWIR3LB = 0x6 - Configure as the IOSLAVE SPI 3-wire MOSI/MISO loop-back signal from IOMSTRx M2WIR3 = 0x7 - Configure as the IOMSTR2 SPI 3-wire MOSI/MISO signal
18	PAD2STRNG	0x0	RW	Pad 2 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
17	PAD2INPEN	0x0	RW	Pad 2 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
16	PAD2PULL	0x0	RW	Pad 2 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
15:14	PAD1RSEL	0x0	RW	Pad 1 pullup resistor selection. PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
13:11	PAD1FNCSEL	0x3	RW	Pad 1 function select SLSDA = 0x0 - Configure as the IOSLAVE I2C SDA signal SLMISO = 0x1 - Configure as the IOSLAVE SPI MISO signal UART0TX = 0x2 - Configure as the UART0 TX output signal GPIO1 = 0x3 - Configure as GPIO1 MxMISOLB = 0x4 - Configure as the IOSLAVE SPI MISO loopback signal from IOMSTRx M2MISO = 0x5 - Configure as the IOMSTR2 SPI MISO input signal MxSDALB = 0x6 - Configure as the IOSLAVE I2C SDA loopback signal from IOMSTRx M2SDA = 0x7 - Configure as the IOMSTR2 I2C Serial data I/O signal
10	PAD1STRNG	0x0	RW	Pad 1 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
9	PAD1INPEN	0x0	RW	Pad 1 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
8	PAD1PULL	0x0	RW	Pad 1 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 374: PADREGA Register Bits

Bit	Name	Reset	RW	Description
7:6	PAD0RSEL	0x0	RW	Pad 0 pullup resistor selection. PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
5:3	PAD0FNCSEL	0x3	RW	Pad 0 function select SLSCL = 0x0 - Configure as the IOSLAVE I2C SCL signal SLSCK = 0x1 - Configure as the IOSLAVE SPI SCK signal CLKOUT = 0x2 - Configure as the CLKOUT signal GPIO0 = 0x3 - Configure as GPIO0 MxSCKLB = 0x4 - Configure as the IOSLAVE SPI SCK loopback signal from IOMSTRx M2SCK = 0x5 - Configure as the IOMSTR2 SPI SCK output MxSCLLB = 0x6 - Configure as the IOSLAVE I2C SCL loopback signal from IOMSTRx M2SCL = 0x7 - Configure as the IOMSTR2 I2C SCL clock I/O signal
2	PAD0STRNG	0x0	RW	Pad 0 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
1	PAD0INPEN	0x0	RW	Pad 0 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD0PULL	0x0	RW	Pad 0 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

8.6.2.2 PADREGB Register

Pad Configuration Register B

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x40010004

This register controls the pad configuration controls for PAD7 through PAD4. Writes to this register must be unlocked by the PADKEY register.

Table 375: PADREGB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		PAD7FNCSEL			PAD7STRNG	PAD7INPEN	PAD7PULL	PAD6RSEL		PAD6FNCSEL			PAD6STRNG	PAD6INPEN	PAD6PULL	PAD5RSEL		PAD5FNCSEL			PAD5STRNG	PAD5INPEN	PAD5PULL	PAD4PWRDN	RSVD	PAD4FNCSEL			PAD4STRNG	PAD4INPEN	PAD4PULL

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 376: PADREGB Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:27	PAD7FNCSEL	0x3	RW	Pad 7 function select M0WIR3 = 0x0 - Configure as the IOMSTR0 SPI 3-wire MOSI/MISO signal M0MOSI = 0x1 - Configure as the IOMSTR0 SPI MOSI signal CLKOUT = 0x2 - Configure as the CLKOUT signal GPIO7 = 0x3 - Configure as GPIO7 TRIG0 = 0x4 - Configure as the ADC Trigger 0 signal UART0TX = 0x5 - Configure as the UART0 TX output signal SLWIR3LB = 0x6 - Configure as the IOMSTR0 SPI 3-wire MOSI/MISO loop-back signal from IOSLAVE M1nCE1 = 0x7 - Configure as the SPI channel 1 nCE signal from IOMSTR1
26	PAD7STRNG	0x0	RW	Pad 7 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
25	PAD7INPEN	0x0	RW	Pad 7 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
24	PAD7PULL	0x0	RW	Pad 7 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
23:22	PAD6RSEL	0x0	RW	Pad 6 pullup resistor selection. PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
21:19	PAD6FNCSEL	0x3	RW	Pad 6 function select M0SDA = 0x0 - Configure as the IOMSTR0 I2C SDA signal M0MISO = 0x1 - Configure as the IOMSTR0 SPI MISO signal UA0CTS = 0x2 - Configure as the UART0 CTS input signal GPIO6 = 0x3 - Configure as GPIO6 SLMISOLB = 0x4 - Configure as the IOMSTR0 SPI MISO loopback signal from IOSLAVE M1nCE0 = 0x5 - Configure as the SPI channel 0 nCE signal from IOMSTR1 SLSDALB = 0x6 - Configure as the IOMSTR0 I2C SDA loopback signal from IOSLAVE I2S_DAT = 0x7 - Configure as the PDM I2S Data output signal
18	PAD6STRNG	0x0	RW	Pad 6 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
17	PAD6INPEN	0x0	RW	Pad 6 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 376: PADREGB Register Bits

Bit	Name	Reset	RW	Description
16	PAD6PULL	0x0	RW	Pad 6 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
15:14	PAD5RSEL	0x0	RW	Pad 5 pullup resistor selection. PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
13:11	PAD5FNCSEL	0x3	RW	Pad 5 function select M0SCL = 0x0 - Configure as the IOMSTR0 I2C SCL signal M0SCK = 0x1 - Configure as the IOMSTR0 SPI SCK signal UA0RTS = 0x2 - Configure as the UART0 RTS signal output GPIO5 = 0x3 - Configure as GPIO5 M0SCKLB = 0x4 - Configure as the IOMSTR0 SPI SCK loopback signal from IOSLAVE RSV = 0x5 - Reserved for future use M0SCLLB = 0x6 - Configure as the IOMSTR0 I2C SCL loopback signal from IOSLAVE M1nCE2 = 0x7 - Configure as the SPI Channel 2 nCE signal from IOMSTR1
10	PAD5STRNG	0x0	RW	Pad 5 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
9	PAD5INPEN	0x0	RW	Pad 5 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
8	PAD5PULL	0x0	RW	Pad 5 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
7	PAD4PWRDN	0x0	RW	Pad 4 VSS power switch enable DIS = 0x0 - Power switch disabled EN = 0x1 - Power switch enabled (switch to GND)
6	RSVD	0x0	RO	RESERVED
5:3	PAD4FNCSEL	0x3	RW	Pad 4 function select UA0CTS = 0x0 - Configure as the UART0 CTS input signal SLINT = 0x1 - Configure as the IOSLAVE interrupt out signal M0nCE5 = 0x2 - Configure as the SPI channel 5 nCE signal from IOMSTR0 GPIO4 = 0x3 - Configure as GPIO4 SLINTGP = 0x4 - Configure as the IOSLAVE interrupt loopback signal M2nCE5 = 0x5 - Configure as the SPI channel 5 nCE signal from IOMSTR2 CLKOUT = 0x6 - Configure as the CLKOUT signal 32khz_XT = 0x7 - Configure as the 32kHz crystal output signal
2	PAD4STRNG	0x0	RW	Pad 4 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 376: PADREGB Register Bits

Bit	Name	Reset	RW	Description
1	PAD4INPEN	0x0	RW	Pad 4 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD4PULL	0x0	RW	Pad 4 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

8.6.2.3 PADREGC Register

Pad Configuration Register C

OFFSET: 0x00000008

INSTANCE 0 ADDRESS: 0x40010008

This register controls the pad configuration controls for PAD11 through PAD8. Writes to this register must be unlocked by the PADKEY register.

Table 377: PADREGC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		PAD11FNCSEL			PAD11STRNG	PAD11INPEN	PAD11PULL	RSVD		PAD10FNC-SEL			PAD10STRNG	PAD10INPEN	PAD10PULL	PAD9RSEL		PAD9FNCSEL			PAD9STRNG	PAD9INPEN	PAD9PULL	PAD8RSEL		PAD8FNCSEL			PAD8STRNG	PAD8INPEN	PAD8PULL

Table 378: PADREGC Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:27	PAD11FNCSEL	0x3	RW	Pad 11 function select ADCSE2 = 0x0 - Configure as the analog input for ADC single ended input 2 M0nCE0 = 0x1 - Configure as the SPI channel 0 nCE signal from IOMSTR0 CLKOUT = 0x2 - Configure as the CLKOUT signal GPIO11 = 0x3 - Configure as GPIO11 M2nCE7 = 0x4 - Configure as the SPI channel 7 nCE signal from IOMSTR2 UA1CTS = 0x5 - Configure as the UART1 CTS input signal UART0RX = 0x6 - Configure as the UART0 RX input signal PDM_DATA = 0x7 - Configure as the PDM Data input signal
26	PAD11STRNG	0x0	RW	Pad 11 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 378: PADREGC Register Bits

Bit	Name	Reset	RW	Description
25	PAD11INPEN	0x0	RW	Pad 11 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
24	PAD11PULL	0x0	RW	Pad 11 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
23:22	RSVD	0x0	RO	RESERVED
21:19	PAD10FNCSEL	0x3	RW	Pad 10 function select M1WIR3 = 0x0 - Configure as the IOMSTR1 SPI 3-wire MOSI/MISO signal M1MOSI = 0x1 - Configure as the IOMSTR1 SPI MOSI signal M0nCE6 = 0x2 - Configure as the SPI channel 6 nCE signal from IOMSTR0 GPIO10 = 0x3 - Configure as GPIO10 M2nCE6 = 0x4 - Configure as the SPI channel 6 nCE signal from IOMSTR2 UA1RTS = 0x5 - Configure as the UART1 RTS output signal M4nCE4 = 0x6 - Configure as the SPI channel 4 nCE signal from the IOM-STR4 SLWIR3LB = 0x7 - Configure as the IOMSTR1 SPI 3-wire MOSI/MISO loop-back signal from IOSLAVE
18	PAD10STRNG	0x0	RW	Pad 10 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
17	PAD10INPEN	0x0	RW	Pad 10 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
16	PAD10PULL	0x0	RW	Pad 10 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
15:14	PAD9RSEL	0x0	RW	Pad 9 pullup resistor selection PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
13:11	PAD9FNCSEL	0x3	RW	Pad 9 function select M1SDA = 0x0 - Configure as the IOMSTR1 I2C SDA signal M1MISO = 0x1 - Configure as the IOMSTR1 SPI MISO signal M0nCE5 = 0x2 - Configure as the SPI channel 5 nCE signal from IOMSTR0 GPIO9 = 0x3 - Configure as GPIO9 M4nCE5 = 0x4 - Configure as the SPI channel 5 nCE signal from IOMSTR4 SLMISOLB = 0x5 - Configure as the IOMSTR1 SPI MISO loopback signal from IOSLAVE UART1RX = 0x6 - Configure as UART1 RX input signal SLSDALB = 0x7 - Configure as the IOMSTR1 I2C SDA loopback signal from IOSLAVE

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 378: PADREGC Register Bits

Bit	Name	Reset	RW	Description
10	PAD9STRNG	0x0	RW	Pad 9 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
9	PAD9INPEN	0x0	RW	Pad 9 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
8	PAD9PULL	0x0	RW	Pad 9 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
7:6	PAD8RSEL	0x0	RW	Pad 8 pullup resistor selection. PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
5:3	PAD8FNCSEL	0x3	RW	Pad 8 function select M1SCL = 0x0 - Configure as the IOMSTR1 I2C SCL signal M1SCK = 0x1 - Configure as the IOMSTR1 SPI SCK signal M0nCE4 = 0x2 - Configure as the SPI channel 4 nCE signal from IOMSTR0 GPIO8 = 0x3 - Configure as GPIO8 M2nCE4 = 0x4 - Configure as the SPI channel 4 nCE signal from IOMSTR2 M1SCKLB = 0x5 - Configure as the IOMSTR1 SPI SCK loopback signal from IOSLAVE UART1TX = 0x6 - Configure as the UART1 TX output signal M1SCLLB = 0x7 - Configure as the IOMSTR1 I2C SCL loopback signal from IOSLAVE
2	PAD8STRNG	0x0	RW	Pad 8 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
1	PAD8INPEN	0x0	RW	Pad 8 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD8PULL	0x0	RW	Pad 8 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

8.6.2.4 PADREGD Register

Pad Configuration Register D

OFFSET: 0x0000000C

INSTANCE 0 ADDRESS: 0x4001000C

This register controls the pad configuration controls for PAD15 through PAD12. Writes to this register must be unlocked by the PADKEY register.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 379: PADREGD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		PAD15FNC-SEL			PAD15STRNG	PAD15INPEN	PAD15PULL	RSVD		PAD14FNC-SEL			PAD14STRNG	PAD14INPEN	PAD14PULL	RSVD		PAD13FNC-SEL			PAD13STRNG	PAD13INPEN	PAD13PULL	RSVD		PAD12FNC-SEL			PAD12STRNG	PAD12INPEN	PAD12PULL

Table 380: PADREGD Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:27	PAD15FNCSEL	0x3	RW	Pad 15 function select ADCD1N = 0x0 - Configure as the analog ADC differential pair 1 N input signal M1nCE3 = 0x1 - Configure as the SPI channel 3 nCE signal from IOMSTR1 UART1RX = 0x2 - Configure as the UART1 RX signal GPIO15 = 0x3 - Configure as GPIO15 M2nCE2 = 0x4 - Configure as the SPI Channel 2 nCE signal from IOMSTR2 RSV = 0x5 - Function reserved for future use SWDIO = 0x6 - Configure as an alternate port for the SWDIO I/O signal SWO = 0x7 - Configure as an SWO (Serial Wire Trace output)
26	PAD15STRNG	0x0	RW	Pad 15 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
25	PAD15INPEN	0x0	RW	Pad 15 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
24	PAD15PULL	0x0	RW	Pad 15 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
23:22	RSVD	0x0	RO	RESERVED
21:19	PAD14FNCSEL	0x3	RW	Pad 14 function select ADCD1P = 0x0 - Configure as the analog ADC differential pair 1 P input signal M1nCE2 = 0x1 - Configure as the SPI channel 2 nCE signal from IOMSTR1 UART1TX = 0x2 - Configure as the UART1 TX output signal GPIO14 = 0x3 - Configure as GPIO14 M2nCE1 = 0x4 - Configure as the SPI channel 1 nCE signal from IOMSTR2 RSV = 0x5 - Function reserved for future use SWDCK = 0x6 - Configure as the alternate input for the SWDCK input signal 32khz_XT = 0x7 - Configure as the 32kHz crystal output signal

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 380: PADREGD Register Bits

Bit	Name	Reset	RW	Description
18	PAD14STRNG	0x0	RW	Pad 14 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
17	PAD14INPEN	0x0	RW	Pad 14 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
16	PAD14PULL	0x0	RW	Pad 14 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
15:14	RSVD	0x0	RO	RESERVED
13:11	PAD13FNCSEL	0x3	RW	Pad 13 function select ADCD0PSE8 = 0x0 - Configure as the ADC Differential pair 0 P, or Single Ended input 8 analog input signal. Determination of the D0P vs SE8 usage is done when the particular channel is selected within the ADC module M1nCE1 = 0x1 - Configure as the SPI channel 1 nCE signal from IOMSTR1 TCTB0 = 0x2 - Configure as the input/output signal from CTIMER B0 GPIO13 = 0x3 - Configure as GPIO13 M2nCE3 = 0x4 - Configure as the SPI channel 3 nCE signal from IOMSTR2 RSV = 0x5 - Function reserved for future use UA0RTS = 0x6 - Configure as the UART0 RTS signal output UART1RX = 0x7 - Configure as the UART1 RX input signal
10	PAD13STRNG	0x0	RW	Pad 13 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
9	PAD13INPEN	0x0	RW	Pad 13 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
8	PAD13PULL	0x0	RW	Pad 13 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
7:6	RSVD	0x0	RO	RESERVED
5:3	PAD12FNCSEL	0x3	RW	Pad 12 function select ADCD0NSE9 = 0x0 - Configure as the ADC Differential pair 0 N, or Single Ended input 9 analog input signal. Determination of the D0N vs SE9 usage is done when the particular channel is selected within the ADC module M1nCE0 = 0x1 - Configure as the SPI channel 0 nCE signal from IOMSTR1 TCTA0 = 0x2 - Configure as the input/output signal from CTIMER A0 GPIO12 = 0x3 - Configure as GPIO12 CLKOUT = 0x4 - Configure as CLKOUT signal PDM_CLK = 0x5 - Configure as the PDM CLK output signal UA0CTS = 0x6 - Configure as the UART0 CTS input signal UART1TX = 0x7 - Configure as the UART1 TX output signal

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 380: PADREGD Register Bits

Bit	Name	Reset	RW	Description
2	PAD12STRNG	0x0	RW	Pad 12 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
1	PAD12INPEN	0x0	RW	Pad 12 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD12PULL	0x0	RW	Pad 12 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

8.6.2.5 PADREGE Register

Pad Configuration Register E

OFFSET: 0x00000010

INSTANCE 0 ADDRESS: 0x40010010

This register controls the pad configuration controls for PAD19 through PAD16. Writes to this register must be unlocked by the PADKEY register.

Table 381: PADREGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		PAD19FNC-SEL			PAD19STRNG	PAD19INPEN	PAD19PULL	RSVD		PAD18FNC-SEL			PAD18STRNG	PAD18INPEN	PAD18PULL	RSVD		PAD17FNC-SEL			PAD17STRNG	PAD17INPEN	PAD17PULL	RSVD		PAD16FNC-SEL			PAD16STRNG	PAD16INPEN	PAD16PULL

Table 382: PADREGE Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:27	PAD19FNCSEL	0x3	RW	Pad 19 function select CMPRF0 = 0x0 - Configure as the analog comparator reference 0 signal M0nCE3 = 0x1 - Configure as the SPI channel 3 nCE signal from IOMSTR0 TCTB1 = 0x2 - Configure as the input/output signal from CTIMER B1 GPIO19 = 0x3 - Configure as GPIO19 TCTA1 = 0x4 - Configure as the input/output signal from CTIMER A1 ANATEST1 = 0x5 - Configure as the ANATEST1 I/O signal UART1RX = 0x6 - Configure as the UART1 RX input signal I2S_BCLK = 0x7 - Configure as the PDM I2S Byte clock input signal

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 382: PADREGE Register Bits

Bit	Name	Reset	RW	Description
26	PAD19STRNG	0x0	RW	Pad 19 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
25	PAD19INPEN	0x0	RW	Pad 19 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
24	PAD19PULL	0x0	RW	Pad 19 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
23:22	RSVD	0x0	RO	RESERVED
21:19	PAD18FNCSEL	0x3	RW	Pad 18 function select CMPIN1 = 0x0 - Configure as the analog comparator input 1 signal M0nCE2 = 0x1 - Configure as the SPI channel 2 nCE signal from IOMSTR0 TCTA1 = 0x2 - Configure as the input/output signal from CTIMER A1 GPIO18 = 0x3 - Configure as GPIO18 M4nCE1 = 0x4 - Configure as the SPI nCE channel 1 from IOMSTR4 ANATEST2 = 0x5 - Configure as ANATEST2 I/O signal UART1TX = 0x6 - Configure as UART1 TX output signal 32khz_XT = 0x7 - Configure as the 32kHz output clock from the crystal
18	PAD18STRNG	0x0	RW	Pad 18 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
17	PAD18INPEN	0x0	RW	Pad 18 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
16	PAD18PULL	0x0	RW	Pad 18 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
15:14	RSVD	0x0	RO	RESERVED
13:11	PAD17FNCSEL	0x3	RW	Pad 17 function select CMPRF1 = 0x0 - Configure as the analog comparator reference signal 1 input signal M0nCE1 = 0x1 - Configure as the SPI channel 1 nCE signal from IOMSTR0 TRIG1 = 0x2 - Configure as the ADC Trigger 1 signal GPIO17 = 0x3 - Configure as GPIO17 M4nCE3 = 0x4 - Configure as the SPI channel 3 nCE signal from IOMSTR4 RSV = 0x5 - Function reserved for future use UART0RX = 0x6 - Configure as UART0 RX input signal UA1CTS = 0x7 - Configure as UART1 CTS input signal
10	PAD17STRNG	0x0	RW	Pad 17 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 382: PADREGE Register Bits

Bit	Name	Reset	RW	Description
9	PAD17INPEN	0x0	RW	Pad 17 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
8	PAD17PULL	0x0	RW	Pad 17 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
7:6	RSVD	0x0	RO	RESERVED
5:3	PAD16FNCSEL	0x3	RW	Pad 16 function select ADCSE0 = 0x0 - Configure as the analog ADC single ended port 0 input signal M0nCE4 = 0x1 - Configure as the SPI channel 4 nCE signal from IOMSTR0 TRIG0 = 0x2 - Configure as the ADC Trigger 0 signal GPIO16 = 0x3 - Configure as GPIO16 M2nCE3 = 0x4 - Configure as SPI channel 3 nCE for IOMSTR2 CMPIN0 = 0x5 - Configure as comparator input 0 signal UART0TX = 0x6 - Configure as UART0 TX output signal UA1RTS = 0x7 - Configure as UART1 RTS output signal
2	PAD16STRNG	0x0	RW	Pad 16 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
1	PAD16INPEN	0x0	RW	Pad 16 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD16PULL	0x0	RW	Pad 16 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

8.6.2.6 PADREGF Register

Pad Configuration Register F

OFFSET: 0x00000014

INSTANCE 0 ADDRESS: 0x40010014

This register controls the pad configuration controls for PAD23 through PAD20. Writes to this register must be unlocked by the PADKEY register.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 383: PADREGF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		RSVD			RSVD	RSVD	RSVD	RSVD	RSVD	PAD22FNC-SEL			PAD22STRNG	PAD22INPEN	PAD22PULL	RSVD		PAD21FNC-SEL			PAD21STRNG	PAD21INPEN	PAD21PULL	RSVD		PAD20FNC-SEL			PAD20STRNG	PAD20INPEN	PAD20PULL

Table 384: PADREGF Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:27	RSVD	0x3	RW	RESERVED
26	RSVD	0x0	RW	RESERVED
25	RSVD	0x0	RW	RESERVED
24	RSVD	0x0	RW	RESERVED
23	PAD22PWRUP	0x0	RW	Pad 22 upper power switch enable DIS = 0x0 - Power switch disabled EN = 0x1 - Power switch enabled
22	RSVD	0x0	RO	RESERVED
21:19	PAD22FNCSEL	0x3	RW	Pad 22 function select UART0TX = 0x0 - Configure as the UART0 TX signal M1nCE7 = 0x1 - Configure as the SPI channel 7 nCE signal from IOMSTR1 TCTA3 = 0x2 - Configure as the input/output signal from CTIMER A3 GPIO22 = 0x3 - Configure as GPIO22 PDM_CLK = 0x4 - Configure as the PDM CLK output UNDEF5 = 0x5 - Undefined/should not be used TCTB1 = 0x6 - Configure as the input/output signal from CTIMER B1 SWO = 0x7 - Configure as the serial trace data output signal
18	PAD22STRNG	0x0	RW	Pad 22 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
17	PAD22INPEN	0x0	RW	Pad 22 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
16	PAD22PULL	0x0	RW	Pad 22 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
15:14	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 384: PADREGF Register Bits

Bit	Name	Reset	RW	Description
13:11	PAD21FNCSEL	0x0	RW	Pad 21 function select SWDIO = 0x0 - Configure as the serial wire debug data signal M1nCE6 = 0x1 - Configure as the SPI channel 6 nCE signal from IOMSTR1 TCTB2 = 0x2 - Configure as the input/output signal from CTIMER B2 GPIO21 = 0x3 - Configure as GPIO21 UART0RX = 0x4 - Configure as UART0 RX input signal UART1RX = 0x5 - Configure as UART1 RX input signal UNDEF6 = 0x6 - Undefined/should not be used UNDEF7 = 0x7 - Undefined/should not be used
10	PAD21STRNG	0x0	RW	Pad 21 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
9	PAD21INPEN	0x1	RW	Pad 21 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
8	PAD21PULL	0x0	RW	Pad 21 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
7:6	RSVD	0x0	RO	RESERVED
5:3	PAD20FNCSEL	0x0	RW	Pad 20 function select SWDCK = 0x0 - Configure as the serial wire debug clock signal M1nCE5 = 0x1 - Configure as the SPI channel 5 nCE signal from IOMSTR1 TCTA2 = 0x2 - Configure as the input/output signal from CTIMER A2 GPIO20 = 0x3 - Configure as GPIO20 UART0TX = 0x4 - Configure as UART0 TX output signal UART1TX = 0x5 - Configure as UART1 TX output signal UNDEF6 = 0x6 - Undefined/should not be used UNDEF7 = 0x7 - Undefined/should not be used
2	PAD20STRNG	0x0	RW	Pad 20 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
1	PAD20INPEN	0x1	RW	Pad 20 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD20PULL	0x0	RW	Pad 20 pulldown enable DIS = 0x0 - Pulldown disabled EN = 0x1 - Pulldown enabled

8.6.2.7 PADREGG Register

Pad Configuration Register G

OFFSET: 0x00000018

INSTANCE 0 ADDRESS: 0x40010018

©2017 Ambiq Micro, Inc.
All rights reserved.

This register controls the pad configuration controls for PAD27 through PAD24. Writes to this register must be unlocked by the PADKEY register.

Table 385: PADREGG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		RSVD			RSVD	RSVD	RSVD	RSVD		RSVD			RSVD	RSVD	RSVD	RSVD		RSVD			RSVD	RSVD	RSVD	RSVD		PAD24FNC-SEL			PAD24STRNG	PAD24INPEN	PAD24PULL

Table 386: PADREGG Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RW	RESERVED
29:27	RSVD	0x3	RW	RESERVED
26	RSVD	0x0	RW	RESERVED
25	RSVD	0x0	RW	RESERVED
24	RSVD	0x0	RW	RESERVED
23:22	RSVD	0x0	RO	RESERVED
21:19	RSVD	0x3	RW	RESERVED
18	RSVD	0x0	RW	RESERVED
17	RSVD	0x0	RW	RESERVED
16	RSVD	0x0	RW	RESERVED
15:14	RSVD	0x0	RW	RESERVED
13:11	RSVD	0x3	RW	RESERVED
10	RSVD	0x0	RW	RESERVED
9	RSVD	0x0	RW	RESERVED
8	RSVD	0x0	RW	RESERVED
7:6	RSVD	0x0	RO	RESERVED
5:3	PAD24FNCSEL	0x3	RW	Pad 24 function select CLKOUT = 0x2 - Configure as the CLKOUT signal All other settings RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 386: PADREGG Register Bits

Bit	Name	Reset	RW	Description
2	PAD24STRNG	0x0	RW	Pad 24 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
1	PAD24INPEN	0x0	RW	Pad 24 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD24PULL	0x0	RW	Pad 24 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

8.6.2.8 PADREGH Register

Pad Configuration Register H

OFFSET: 0x0000001C

INSTANCE 0 ADDRESS: 0x4001001C

This register controls the pad configuration controls for PAD31 through PAD28. Writes to this register must be unlocked by the PADKEY register.

Table 387: PADREGH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		RSVD			RSVD	RSVD	RSVD	RSVD		PAD30FNC-SEL			PAD30STRNG	PAD30INPEN	PAD30PULL	RSVD		PAD29FNC-SEL			PAD29STRNG	PAD29INPEN	PAD29PULL	RSVD		RSVD			RSVD	RSVD	RSVD

Table 388: PADREGH Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:27	RSVD	0x3	RW	RESERVED
26	RSVD	0x0	RW	RESERVED
25	RSVD	0x0	RW	RESERVED
24	RSVD	0x0	RW	RESERVED
23:22	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 388: PADREGH Register Bits

Bit	Name	Reset	RW	Description
21:19	PAD30FNCSEL	0x3	RW	Pad 30 function select UNDEF0 = 0x0 - Undefined/should not be used M1nCE7 = 0x1 - Configure as the SPI channel 7 nCE signal from IOMSTR1 TCTB2 = 0x2 - Configure as the input/output signal from CTIMER B2 GPIO30 = 0x3 - Configure as GPIO30 UART0TX = 0x4 - Configure as UART0 TX output signal UA1RTS = 0x5 - Configure as UART1 RTS output signal UNDEF6 = 0x6 - Undefined/should not be used I2S_DAT = 0x7 - Configure as the PDM I2S Data output signal
18	PAD30STRNG	0x0	RW	Pad 30 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
17	PAD30INPEN	0x0	RW	Pad 30 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
16	PAD30PULL	0x0	RW	Pad 30 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
15:14	RSVD	0x0	RO	RESERVED
13:11	PAD29FNCSEL	0x3	RW	Pad 29 function select ADCSE1 = 0x0 - Configure as the analog input for ADC single ended input 1 M1nCE6 = 0x1 - Configure as the SPI channel 6 nCE signal from IOMSTR1 TCTA2 = 0x2 - Configure as the input/output signal from CTIMER A2 GPIO29 = 0x3 - Configure as GPIO29 UA0CTS = 0x4 - Configure as the UART0 CTS signal UA1CTS = 0x5 - Configure as the UART1 CTS signal M4nCE0 = 0x6 - Configure as the SPI channel 0 nCE signal from IOMSTR4 PDM_DATA = 0x7 - Configure as PDM DATA input
10	PAD29STRNG	0x0	RW	Pad 29 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
9	PAD29INPEN	0x0	RW	Pad 29 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
8	PAD29PULL	0x0	RW	Pad 29 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
7:6	RSVD	0x0	RO	RESERVED
5:3	RSVD	0x3	RW	RESERVED
2	RSVD	0x0	RW	RESERVED
1	RSVD	0x0	RW	RESERVED
0	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2.9 PADREGJ Register

Pad Configuration Register J

OFFSET: 0x00000024

INSTANCE 0 ADDRESS: 0x40010024

This register controls the pad configuration controls for PAD39 through PAD36. Writes to this register must be unlocked by the PADKEY register.

Table 389: PADREGJ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAD39RSEL		PAD39FNC-SEL			PAD39STRNG	PAD39INPEN	PAD39PULL	RSVD		RSVD			RSVD	RSVD	RSVD	RSVD		RSVD			RSVD	RSVD	RSVD	RSVD		PAD36FNC-SEL			PAD36STRNG	PAD36INPEN	PAD36PULL

Table 390: PADREGJ Register Bits

Bit	Name	Reset	RW	Description
31:30	PAD39RSEL	0x0	RW	Pad 39 pullup resistor selection. PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
29:27	PAD39FNCSEL	0x3	RW	Pad 39 function select UART0TX = 0x0 - Configure as the UART0 TX Signal UART1TX = 0x1 - Configure as the UART1 TX signal CLKOUT = 0x2 - Configure as the CLKOUT signal GPIO39 = 0x3 - Configure as GPIO39 M4SCL = 0x4 - Configure as the IOMSTR4 I2C SCL signal M4SCK = 0x5 - Configure as the IOMSTR4 SPI SCK signal M4SCKLB = 0x6 - Configure as the IOMSTR4 SPI SCK loopback signal from IOSLAVE M4SCLLB = 0x7 - Configure as the IOMSTR4 I2C SCL loopback signal from IOSLAVE
26	PAD39STRNG	0x0	RW	Pad 39 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
25	PAD39INPEN	0x0	RW	Pad 39 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
24	PAD39PULL	0x0	RW	Pad 39 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 390: PADREGJ Register Bits

Bit	Name	Reset	RW	Description
23:22	RSVD	0x0	RO	RESERVED
21:19	RSVD	0x3	RW	RESERVED
18	RSVD	0x0	RW	RESERVED
17	RSVD	0x0	RW	RESERVED
16	RSVD	0x0	RW	RESERVED
15:14	RSVD	0x0	RO	RESERVED
13:11	RSVD	0x3	RW	RESERVED
10	RSVD	0x0	RW	RESERVED
9	RSVD	0x0	RW	RESERVED
8	RSVD	0x0	RW	RESERVED
7:6	RSVD	0x0	RO	RESERVED
5:3	PAD36FNCSEL	0x3	RW	Pad 36 function select TRIG1 = 0x0 - Configure as the ADC Trigger 1 signal M1nCE1 = 0x1 - Configure as the SPI channel 1 nCE signal from IOMSTR1 UART1RX = 0x2 - Configure as the UART1 RX signal GPIO36 = 0x3 - Configure as GPIO36 32khz_XT = 0x4 - Configure as the 32kHz output clock from the crystal M2nCE0 = 0x5 - Configure as the SPI channel 0 nCE signal from IOMSTR2 UA0CTS = 0x6 - Configure as the UART0 CTS signal M3nCE3 = 0x7 - Configure as the SPI channel 3 nCE signal from IOMSTR3
2	PAD36STRNG	0x0	RW	Pad 36 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
1	PAD36INPEN	0x0	RW	Pad 36 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD36PULL	0x0	RW	Pad 36 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

8.6.2.10 PADREGK Register

Pad Configuration Register K

OFFSET: 0x00000028

INSTANCE 0 ADDRESS: 0x40010028

This register controls the pad configuration controls for PAD43 through PAD40. Writes to this register must be unlocked by the PADKEY register.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 391: PADREGK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		RSVD			RSVD	RSVD	RSVD	PAD42RSEL		PAD42FNC-SEL			PAD42STRNG	PAD42INPEN	PAD42PULL	PAD41PWRUP	RSVD	PAD41FNC-SEL			PAD41STRNG	PAD41INPEN	PAD41PULL	PAD40RSEL		PAD40FNC-SEL			PAD40STRNG	PAD40INPEN	PAD40PULL

Table 392: PADREGK Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RW	RESERVED
29:27	RSVD	0x3	RW	RESERVED
26	RSVD	0x0	RW	RESERVED
25	RSVD	0x0	RW	RESERVED
24	RSVD	0x0	RW	RESERVED
23:22	PAD42RSEL	0x0	RW	Pad 42 pullup resistor selection. PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
21:19	PAD42FNCSEL	0x3	RW	Pad 42 function select M2nCE2 = 0x0 - Configure as the SPI channel 2 nCE signal from IOMSTR2 All other settings RESERVED
18	PAD42STRNG	0x0	RW	Pad 42 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
17	PAD42INPEN	0x0	RW	Pad 42 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
16	PAD42PULL	0x0	RW	Pad 42 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
15	PAD41PWRUP	0x0	RW	Pad 41 upper power switch enable DIS = 0x0 - Power switch disabled EN = 0x1 - Power switch enabled (VDD switch)
14	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 392: PADREGK Register Bits

Bit	Name	Reset	RW	Description
13:11	PAD41FNCSEL	0x3	RW	Pad 41 function select M2nCE1 = 0x0 - Configure as the SPI channel 1 nCE signal from IOMSTR2 CLKOUT = 0x1 - Configure as the CLKOUT signal SWO = 0x2 - Configure as the serial wire debug SWO signal GPIO41 = 0x3 - Configure as GPIO41 M3nCE5 = 0x4 - Configure as the SPI channel 5 nCE signal from IOMSTR3 M5nCE7 = 0x5 - Configure as the SPI channel 7 nCE signal from IOMSTR5 M4nCE2 = 0x6 - Configure as the SPI channel 2 nCE signal from IOMSTR4 UA0RTS = 0x7 - Configure as the UART0 RTS output
10	PAD41STRNG	0x0	RW	Pad 41 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
9	PAD41INPEN	0x0	RW	Pad 41 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
8	PAD41PULL	0x0	RW	Pad 41 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
7:6	PAD40RSEL	0x0	RW	Pad 40 pullup resistor selection. PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
5:3	PAD40FNCSEL	0x3	RW	Pad 40 function select UART0RX = 0x0 - Configure as the UART0 RX input signal UART1RX = 0x1 - Configure as the UART1 RX input signal TRIG0 = 0x2 - Configure as the ADC Trigger 0 signal GPIO40 = 0x3 - Configure as GPIO40 M4SDA = 0x4 - Configure as the IOMSTR4 I2C serial data I/O signal M4MISO = 0x5 - Configure as the IOMSTR4 SPI MISO input signal SLMISOLB = 0x6 - Configure as the IOMSTR4 SPI MISO loopback signal from IOSLAVE SLSDALB = 0x7 - Configure as the IOMSTR4 I2C SDA loopback signal from IOSLAVE
2	PAD40STRNG	0x0	RW	Pad 40 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
1	PAD40INPEN	0x0	RW	Pad 40 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD40PULL	0x0	RW	Pad 40 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2.11 PADREGL Register

Pad Configuration Register L

OFFSET: 0x0000002C

INSTANCE 0 ADDRESS: 0x4001002C

This register controls the pad configuration controls for PAD47 through PAD44. Writes to this register must be unlocked by the PADKEY register.

Table 393: PADREGL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		PAD47FNC-SEL			PAD47STRNG	PAD47INPEN	PAD47PULL	RSVD		PAD46FNC-SEL			PAD46STRNG	PAD46INPEN	PAD46PULL	RSVD		PAD45FNC-SEL			PAD45STRNG	PAD45INPEN	PAD45PULL	RSVD		PAD44FNC-SEL			PAD44STRNG	PAD44INPEN	PAD44PULL

Table 394: PADREGL Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:27	PAD47FNCSEL	0x3	RW	Pad 47 function select M5MOSI = 0x5 - Configure as the IOMSTR5 SPI MOSI output signal All other settings RESERVED
26	PAD47STRNG	0x0	RW	Pad 47 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
25	PAD47INPEN	0x0	RW	Pad 47 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
24	PAD47PULL	0x0	RW	Pad 47 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
23:22	RSVD	0x0	RO	RESERVED
21:19	PAD46FNCSEL	0x3	RW	Pad 46 function select M5nCE4 = 0x5 - Configure as the SPI channel 4 nCE signal from IOMSTR5 All other settings RESERVED
18	PAD46STRNG	0x0	RW	Pad 46 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 394: PADREGL Register Bits

Bit	Name	Reset	RW	Description
17	PAD46INPEN	0x0	RW	Pad 46 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
16	PAD46PULL	0x0	RW	Pad 46 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
15:14	RSVD	0x0	RO	RESERVED
13:11	PAD45FNCSEL	0x3	RW	Pad 45 function select M5nCE5 = 0x6 - Configure as the SPI channel 5 nCE signal from IOMSTR5 All other settings RESERVED
10	PAD45STRNG	0x0	RW	Pad 45 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
9	PAD45INPEN	0x0	RW	Pad 45 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
8	PAD45PULL	0x0	RW	Pad 45 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled
7:6	RSVD	0x0	RO	RESERVED
5:3	PAD44FNCSEL	0x3	RW	Pad 44 function select UA1RTS = 0x0 - Configure as the UART1 RTS output signal M0nCE2 = 0x1 - Configure as the SPI channel 2 nCE signal from IOMSTR0 TCTA1 = 0x2 - Configure as the input/output signal from CTIMER A1 GPIO44 = 0x3 - Configure as GPIO44 M4WIR3 = 0x4 - Configure as the IOMSTR4 SPI 3-wire MOSI/MISO signal M4MOSI = 0x5 - Configure as the IOMSTR4 SPI MOSI signal M5nCE6 = 0x6 - Configure as the SPI channel 6 nCE signal from IOMSTR5 SLWIR3LB = 0x7 - Configure as the IOMSTR4 SPI 3-wire MOSI/MISO loop-back signal from IOSLAVE
2	PAD44STRNG	0x0	RW	Pad 44 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
1	PAD44INPEN	0x0	RW	Pad 44 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD44PULL	0x0	RW	Pad 44 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2.12 PADREGM Register

Pad Configuration Register M

OFFSET: 0x00000030

INSTANCE 0 ADDRESS: 0x40010030

This register controls the pad configuration controls for PAD49 through PAD48. Writes to this register must be unlocked by the PADKEY register.

Table 395: PADREGM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																PAD49RSEL		PAD49FNC-SEL			PAD49STRNG	PAD49INPEN	PAD49PULL	PAD48RSEL		PAD48FNC-SEL			PAD48STRNG	PAD48INPEN	PAD48PULL

Table 396: PADREGM Register Bits

Bit	Name	Reset	RW	Description
31:16	RSVD	0x0	RO	RESERVED
15:14	PAD49RSEL	0x0	RW	Pad 49 pullup resistor selection. PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
13:11	PAD49FNCSEL	0x3	RW	Pad 49 function select M5MISO = 0x5 - Configure as the IOMSTR5 SPI MISO input signal All other settings RESERVED
10	PAD49STRNG	0x0	RW	Pad 49 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
9	PAD49INPEN	0x0	RW	Pad 49 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
8	PAD49PULL	0x0	RW	Pad 49 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 396: PADREGM Register Bits

Bit	Name	Reset	RW	Description
7:6	PAD48RSEL	0x0	RW	Pad 48 pullup resistor selection. PULL1_5K = 0x0 - Pullup is ~1.5 KOhms PULL6K = 0x1 - Pullup is ~6 KOhms PULL12K = 0x2 - Pullup is ~12 KOhms PULL24K = 0x3 - Pullup is ~24 KOhms
5:3	PAD48FNCSEL	0x3	RW	Pad 48 function select M5SCK = 0x5 - Configure as the IOMSTR5 SPI SCK output All other settings RESERVED
2	PAD48STRNG	0x0	RW	Pad 48 drive strength LOW = 0x0 - Low drive strength HIGH = 0x1 - High drive strength
1	PAD48INPEN	0x0	RW	Pad 48 input enable DIS = 0x0 - Pad input disabled EN = 0x1 - Pad input enabled
0	PAD48PULL	0x0	RW	Pad 48 pullup enable DIS = 0x0 - Pullup disabled EN = 0x1 - Pullup enabled

8.6.2.13 CFGA Register

GPIO Configuration Register A

OFFSET: 0x00000040

INSTANCE 0 ADDRESS: 0x40010040

GPIO configuration controls for GPIO[7:0]. Writes to this register must be unlocked by the PADKEY register.

Table 397: CFGA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
GPIO7INTD	GPIO7OUTCFG		GPIO7INCFG	GPIO6INTD	GPIO6OUTCFG		GPIO6INCFG	GPIO5INTD	GPIO5OUTCFG		GPIO5INCFG	GPIO4INTD	GPIO4OUTCFG		GPIO4INCFG	GPIO3INTD	GPIO3OUTCFG		GPIO3INCFG	GPIO2INTD	GPIO2OUTCFG		GPIO2INCFG	GPIO1INTD	GPIO1OUTCFG		GPIO1INCFG	GPIO0INTD	GPIO0OUTCFG		GPIO0INCFG

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 398: CFGA Register Bits

Bit	Name	Reset	RW	Description
31	GPIO7INTD	0x0	RW	GPIO7 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
30:29	GPIO7OUTCFG	0x0	RW	GPIO7 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
28	GPIO7INCFG	0x0	RW	GPIO7 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
27	GPIO6INTD	0x0	RW	GPIO6 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
26:25	GPIO6OUTCFG	0x0	RW	GPIO6 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
24	GPIO6INCFG	0x0	RW	GPIO6 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
23	GPIO5INTD	0x0	RW	GPIO5 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
22:21	GPIO5OUTCFG	0x0	RW	GPIO5 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
20	GPIO5INCFG	0x0	RW	GPIO5 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
19	GPIO4INTD	0x0	RW	GPIO4 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
18:17	GPIO4OUTCFG	0x0	RW	GPIO4 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 398: CFGA Register Bits

Bit	Name	Reset	RW	Description
16	GPIO4INCFG	0x0	RW	GPIO4 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
15	GPIO3INTD	0x0	RW	GPIO3 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
14:13	GPIO3OUTCFG	0x0	RW	GPIO3 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
12	GPIO3INCFG	0x0	RW	GPIO3 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
11	GPIO2INTD	0x0	RW	GPIO2 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
10:9	GPIO2OUTCFG	0x0	RW	GPIO2 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
8	GPIO2INCFG	0x0	RW	GPIO2 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
7	GPIO1INTD	0x0	RW	GPIO1 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
6:5	GPIO1OUTCFG	0x0	RW	GPIO1 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
4	GPIO1INCFG	0x0	RW	GPIO1 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
3	GPIO0INTD	0x0	RW	GPIO0 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 398: CFGA Register Bits

Bit	Name	Reset	RW	Description
2:1	GPIO0OUTCFG	0x0	RW	GPIO0 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
0	GPIO0INCFG	0x0	RW	GPIO0 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero

8.6.2.14 CFGB Register

GPIO Configuration Register B

OFFSET: 0x00000044

INSTANCE 0 ADDRESS: 0x40010044

GPIO configuration controls for GPIO[15:8]. Writes to this register must be unlocked by the PADKEY register.

Table 399: CFGB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
GPIO15INTD	GPIO15OUTCFG		GPIO15INCFG	GPIO14INTD	GPIO14OUTCFG		GPIO14INCFG	GPIO13INTD	GPIO13OUTCFG		GPIO13INCFG	GPIO12INTD	GPIO12OUTCFG		GPIO12INCFG	GPIO11INTD	GPIO11OUTCFG		GPIO11INCFG	GPIO10INTD	GPIO10OUTCFG		GPIO10INCFG	GPIO9INTD	GPIO9OUTCFG		GPIO9INCFG	GPIO8INTD	GPIO8OUTCFG		GPIO8INCFG

Table 400: CFGB Register Bits

Bit	Name	Reset	RW	Description
31	GPIO15INTD	0x0	RW	GPIO15 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
30:29	GPIO15OUT-CFG	0x0	RW	GPIO15 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
28	GPIO15INCFG	0x0	RW	GPIO15 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 400: CFGB Register Bits

Bit	Name	Reset	RW	Description
27	GPIO14INTD	0x0	RW	GPIO14 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
26:25	GPIO14OUT-CFG	0x0	RW	GPIO14 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
24	GPIO14INCFG	0x0	RW	GPIO14 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
23	GPIO13INTD	0x0	RW	GPIO13 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
22:21	GPIO13OUT-CFG	0x0	RW	GPIO13 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
20	GPIO13INCFG	0x0	RW	GPIO13 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
19	GPIO12INTD	0x0	RW	GPIO12 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
18:17	GPIO12OUT-CFG	0x0	RW	GPIO12 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
16	GPIO12INCFG	0x0	RW	GPIO12 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
15	GPIO11INTD	0x0	RW	GPIO11 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
14:13	GPIO11OUT-CFG	0x0	RW	GPIO11 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 400: CFGB Register Bits

Bit	Name	Reset	RW	Description
12	GPIO11INCFG	0x0	RW	GPIO11 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
11	GPIO10INTD	0x0	RW	GPIO10 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
10:9	GPIO10OUT-CFG	0x0	RW	GPIO10 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
8	GPIO10INCFG	0x0	RW	GPIO10 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
7	GPIO9INTD	0x0	RW	GPIO9 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
6:5	GPIO9OUTCFG	0x0	RW	GPIO9 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
4	GPIO9INCFG	0x0	RW	GPIO9 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
3	GPIO8INTD	0x0	RW	GPIO8 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
2:1	GPIO8OUTCFG	0x0	RW	GPIO8 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
0	GPIO8INCFG	0x0	RW	GPIO8 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero

8.6.2.15 CFGC Register

GPIO Configuration Register C

OFFSET: 0x00000048

INSTANCE 0 ADDRESS: 0x40010048

©2017 Ambiq Micro, Inc.
All rights reserved.

GPIO configuration controls for GPIO[23:16]. Writes to this register must be unlocked by the PADKEY register.

Table 401: CFGC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	RSVD		RSVD	GPIO22INTD	GPIO22OUTCFG		GPIO22INCFG	GPIO21INTD	GPIO21OUTCFG		GPIO21INCFG	GPIO20INTD	GPIO20OUTCFG		GPIO20INCFG	GPIO19INTD	GPIO19OUTCFG		GPIO19INCFG	GPIO18INTD	GPIO18OUTCFG		GPIO18INCFG	GPIO17INTD	GPIO17OUTCFG		GPIO17INCFG	GPIO16INTD	GPIO16OUTCFG		GPIO16INCFG

Table 402: CFGC Register Bits

Bit	Name	Reset	RW	Description
31	RSVD	0x0	RW	RESERVED
30:29	RSVD	0x0	RW	RESERVED
28	RSVD	0x0	RW	RESERVED
27	GPIO22INTD	0x0	RW	GPIO22 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
26:25	GPIO22OUT-CFG	0x0	RW	GPIO22 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
24	GPIO22INCFG	0x0	RW	GPIO22 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
23	GPIO21INTD	0x0	RW	GPIO21 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
22:21	GPIO21OUT-CFG	0x0	RW	GPIO21 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
20	GPIO21INCFG	0x1	RW	GPIO21 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 402: CFGC Register Bits

Bit	Name	Reset	RW	Description
19	GPIO20INTD	0x0	RW	GPIO20 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
18:17	GPIO20OUT-CFG	0x0	RW	GPIO20 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
16	GPIO20INCFG	0x1	RW	GPIO20 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
15	GPIO19INTD	0x0	RW	GPIO19 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
14:13	GPIO19OUT-CFG	0x0	RW	GPIO19 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
12	GPIO19INCFG	0x0	RW	GPIO19 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
11	GPIO18INTD	0x0	RW	GPIO18 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
10:9	GPIO18OUT-CFG	0x0	RW	GPIO18 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
8	GPIO18INCFG	0x0	RW	GPIO18 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
7	GPIO17INTD	0x0	RW	GPIO17 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
6:5	GPIO17OUT-CFG	0x0	RW	GPIO17 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 402: CFGC Register Bits

Bit	Name	Reset	RW	Description
4	GPIO17INCFG	0x0	RW	GPIO17 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
3	GPIO16INTD	0x0	RW	GPIO16 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
2:1	GPIO16OUT-CFG	0x0	RW	GPIO16 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
0	GPIO16INCFG	0x0	RW	GPIO16 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero

8.6.2.16 CFGD Register

GPIO Configuration Register D

OFFSET: 0x0000004C

INSTANCE 0 ADDRESS: 0x4001004C

GPIO configuration controls for GPIO[31:24]. Writes to this register must be unlocked by the PADKEY register.

Table 403: CFGD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	RSVD	RSVD	GPIO30INTD	GPIO30OUTCFG			GPIO30INCFG	GPIO29INTD	GPIO29OUTCFG		GPIO29INCFG	RSVD	RSVD		RSVD	RSVD	RSVD		RSVD	RSVD	RSVD		RSVD	RSVD	RSVD		RSVD	RSVD	RSVD		RSVD

Table 404: CFGD Register Bits

Bit	Name	Reset	RW	Description
31	RSVD	0x0	RW	RESERVED
30:29	RSVD	0x0	RW	RESERVED
28	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 404: CFGD Register Bits

Bit	Name	Reset	RW	Description
27	GPIO30INTD	0x0	RW	GPIO30 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
26:25	GPIO30OUT-CFG	0x0	RW	GPIO30 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
24	GPIO30INCFG	0x0	RW	GPIO30 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
23	GPIO29INTD	0x0	RW	GPIO29 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
22:21	GPIO29OUT-CFG	0x0	RW	GPIO29 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
20	GPIO29INCFG	0x0	RW	GPIO29 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
19	RSVD	0x0	RW	RESERVED
18:17	RSVD	0x0	RW	RESERVED
16	RSVD	0x0	RW	RESERVED
15	RSVD	0x0	RW	RESERVED
14:13	RSVD	0x0	RW	RESERVED
12	RSVD	0x0	RW	RESERVED
11	RSVD	0x0	RW	RESERVED
10:9	RSVD	0x0	RW	RESERVED
8	RSVD	0x0	RW	RESERVED
7	RSVD	0x0	RW	RESERVED
6:5	RSVD	0x0	RW	RESERVED
4	RSVD	0x0	RW	RESERVED
3	GPIO24INTD RSVD	0x0	RW	GPIO24 interrupt direction. RESERVED
2:1	GPIO24OUT-CFG RSVD	0x0	RW	GPIO24 output configuration. RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 404: CFGD Register Bits

Bit	Name	Reset	RW	Description
0	GPIO24INCFG RSVD	0x0	RW	GPIO24 input enable. RESERVED

8.6.2.17 CFGE Register

GPIO Configuration Register E

OFFSET: 0x00000050

INSTANCE 0 ADDRESS: 0x40010050

GPIO configuration controls for GPIO[39:32]. Writes to this register must be unlocked by the PADKEY register.

Table 405: CFGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
GPIO39INTD	GPIO39OUTCFG		GPIO39INCFG	RSVD	RSVD		RSVD	RSVD	RSVD		RSVD	GPIO36INTD	GPIO36OUTCFG		GPIO36INCFG	GPIO35INTD	GPIO35OUTCFG		GPIO35INCFG	RSVD	RSVD		RSVD	RSVD	RSVD		RSVD	RSVD	RSVD		RSVD	RSVD

Table 406: CFGE Register Bits

Bit	Name	Reset	RW	Description
31	GPIO39INTD	0x0	RW	GPIO39 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
30:29	GPIO39OUT-CFG	0x0	RW	GPIO39 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
28	GPIO39INCFG	0x0	RW	GPIO39 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
27	RSVD	0x0	RW	RESERVED
26:25	RSVD	0x0	RW	RESERVED
24	RSVD	0x0	RW	RESERVED
23	RSVD	0x0	RW	RESERVED
22:21	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 406: CFGE Register Bits

Bit	Name	Reset	RW	Description
20	RSVD	0x0	RW	RESERVED
19	GPIO36INTD	0x0	RW	GPIO36 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
18:17	GPIO36OUT-CFG	0x0	RW	GPIO36 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
16	GPIO36INCFG	0x0	RW	GPIO36 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
15	GPIO35INTD	0x0	RW	GPIO35 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
14:13	GPIO35OUT-CFG	0x0	RW	GPIO35 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
12	GPIO35INCFG	0x0	RW	GPIO35 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
11	RSVD	0x0	RW	RESERVED
10:9	RSVD	0x0	RW	RESERVED
8	RSVD	0x0	RW	RESERVED
7	RSVD	0x0	RW	RESERVED
6:5	RSVD	0x0	RW	RESERVED
4	RSVD	0x0	RW	RESERVED
3	RSVD	0x0	RW	RESERVED
2:1	RSVD	0x0	RW	RESERVED
0	RSVD	0x0	RW	RESERVED

8.6.2.18 CFGF Register

GPIO Configuration Register F

OFFSET: 0x00000054

INSTANCE 0 ADDRESS: 0x40010054

GPIO configuration controls for GPIO[47:40]. Writes to this register must be unlocked by the PADKEY register.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 407: CFGF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	RSVD		RSVD	RSVD	RSVD		RSVD	RSVD	RSVD		RSVD	GPIO44INTD	GPIO44OUTCFG		GPIO44INCFG	RSVD	RSVD		RSVD	RSVD	RSVD		RSVD	GPIO41INTD	GPIO41OUTCFG		GPIO41INCFG	GPIO40INTD	GPIO40OUTCFG		GPIO40INCFG

Table 408: CFGF Register Bits

Bit	Name	Reset	RW	Description
31	RSVD	0x0	RW	GPIO47 interrupt direction. RESERVED
30:29	RSVD	0x0	RW	GPIO47 output configuration. RESERVED
28	RSVD	0x0	RW	GPIO47 input enable. RESERVED
27	RSVD	0x0	RW	GPIO46 interrupt direction. RESERVED
26:25	RSVD	0x0	RW	GPIO46 output configuration. RESERVED
24	RSVD	0x0	RW	GPIO46 input enable. RESERVED
23	RSVD	0x0	RW	GPIO45 interrupt direction. RESERVED
22:21	RSVD	0x0	RW	GPIO45 output configuration. RESERVED
20	RSVD	0x0	RW	GPIO45 input enable. RESERVED
19	GPIO44INTD	0x0	RW	GPIO44 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 408: CFGF Register Bits

Bit	Name	Reset	RW	Description
18:17	GPIO44OUT-CFG	0x0	RW	GPIO44 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
16	GPIO44INCFG	0x0	RW	GPIO44 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
15	RSVD	0x0	RW	RESERVED
14:13	RSVD	0x0	RW	RESERVED
12	RSVD	0x0	RW	RESERVED
11	RSVD	0x0	RW	GPIO42 interrupt direction. RESERVED
10:9	RSVD	0x0	RW	GPIO42 output configuration. RESERVED
8	RSVD	0x0	RW	GPIO42 input enable. RESERVED
7	GPIO41INTD	0x0	RW	GPIO41 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
6:5	GPIO41OUT-CFG	0x0	RW	GPIO41 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
4	GPIO41INCFG	0x0	RW	GPIO41 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero
3	GPIO40INTD	0x0	RW	GPIO40 interrupt direction. INTLH = 0x0 - Interrupt on low to high GPIO transition INTHL = 0x1 - Interrupt on high to low GPIO transition
2:1	GPIO40OUT-CFG	0x0	RW	GPIO40 output configuration. DIS = 0x0 - Output disabled PUSHPULL = 0x1 - Output is push-pull OD = 0x2 - Output is open drain TS = 0x3 - Output is tri-state
0	GPIO40INCFG	0x0	RW	GPIO40 input enable. READ = 0x0 - Read the GPIO pin data RDZERO = 0x1 - Readback will always be zero

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2.19 PADKEY Register

Key Register for all pad configuration registers

OFFSET: 0x00000060

INSTANCE 0 ADDRESS: 0x40010060

Key Register for all pad configuration registers

Table 409: PADKEY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PADKEY																															

Table 410: PADKEY Register Bits

Bit	Name	Reset	RW	Description
31:0	PADKEY	0x0	RW	Key register value. Key = 0x73 - Key

8.6.2.20 RDA Register

GPIO Input Register A

OFFSET: 0x00000080

INSTANCE 0 ADDRESS: 0x40010080

GPIO Input Register A

Table 411: RDA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RDA																															

Table 412: RDA Register Bits

Bit	Name	Reset	RW	Description
31:0	RDA	0x0	RO	GPIO31-0 read data.

8.6.2.21 RDB Register

GPIO Input Register B

OFFSET: 0x00000084

©2017 Ambiq Micro, Inc.
All rights reserved.

INSTANCE 0 ADDRESS: 0x40010084

GPIO Input Register B

Table 413: RDB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														RDB																	

Table 414: RDB Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17:0	RDB	0x0	RO	GPIO49-32 read data.

8.6.2.22 WTA Register

GPIO Output Register A

OFFSET: 0x00000088

INSTANCE 0 ADDRESS: 0x40010088

GPIO Output Register A

Table 415: WTA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WTA																															

Table 416: WTA Register Bits

Bit	Name	Reset	RW	Description
31:0	WTA	0x0	RW	GPIO31-0 write data.

8.6.2.23 WTB Register

GPIO Output Register B

OFFSET: 0x0000008C

INSTANCE 0 ADDRESS: 0x4001008C

GPIO Output Register B

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 417: WTB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														WTB																	

Table 418: WTB Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17:0	WTB	0x0	RW	GPIO49-32 write data.

8.6.2.24 WTSA Register

GPIO Output Register A Set

OFFSET: 0x00000090

INSTANCE 0 ADDRESS: 0x40010090

GPIO Output Register A Set

Table 419: WTSA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WTSA																															

Table 420: WTSA Register Bits

Bit	Name	Reset	RW	Description
31:0	WTSA	0x0	WO	Set the GPIO31-0 write data.

8.6.2.25 WTSB Register

GPIO Output Register B Set

OFFSET: 0x00000094

INSTANCE 0 ADDRESS: 0x40010094

GPIO Output Register B Set

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 421: WTSB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														WTSB																	

Table 422: WTSB Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17:0	WTSB	0x0	WO	Set the GPIO49-32 write data.

8.6.2.26 WTCA Register

GPIO Output Register A Clear

OFFSET: 0x00000098

INSTANCE 0 ADDRESS: 0x40010098

GPIO Output Register A Clear

Table 423: WTCA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WTCA																															

Table 424: WTCA Register Bits

Bit	Name	Reset	RW	Description
31:0	WTCA	0x0	WO	Clear the GPIO31-0 write data.

8.6.2.27 WTCB Register

GPIO Output Register B Clear

OFFSET: 0x0000009C

INSTANCE 0 ADDRESS: 0x4001009C

GPIO Output Register B Clear

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 425: WTCB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														WTCB																	

Table 426: WTCB Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17:0	WTCB	0x0	WO	Clear the GPIO49-32 write data.

8.6.2.28 ENA Register

GPIO Enable Register A

OFFSET: 0x000000A0

INSTANCE 0 ADDRESS: 0x400100A0

GPIO Enable Register A

Table 427: ENA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ENA																															

Table 428: ENA Register Bits

Bit	Name	Reset	RW	Description
31:0	ENA	0x0	RW	GPIO31-0 output enables

8.6.2.29 ENB Register

GPIO Enable Register B

OFFSET: 0x000000A4

INSTANCE 0 ADDRESS: 0x400100A4

GPIO Enable Register B

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 429: ENB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														ENB																	

Table 430: ENB Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17:0	ENB	0x0	RW	GPIO49-32 output enables

8.6.2.30 ENSA Register

GPIO Enable Register A Set

OFFSET: 0x000000A8

INSTANCE 0 ADDRESS: 0x400100A8

GPIO Enable Register A Set

Table 431: ENSA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ENSA																															

Table 432: ENSA Register Bits

Bit	Name	Reset	RW	Description
31:0	ENSA	0x0	RW	Set the GPIO31-0 output enables

8.6.2.31 ENSB Register

GPIO Enable Register B Set

OFFSET: 0x000000AC

INSTANCE 0 ADDRESS: 0x400100AC

GPIO Enable Register B Set

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 433: ENSB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														ENSB																	

Table 434: ENSB Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17:0	ENSB	0x0	RW	Set the GPIO49-32 output enables

8.6.2.32 ENCA Register

GPIO Enable Register A Clear

OFFSET: 0x000000B4

INSTANCE 0 ADDRESS: 0x400100B4

GPIO Enable Register A Clear

Table 435: ENCA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ENCA																															

Table 436: ENCA Register Bits

Bit	Name	Reset	RW	Description
31:0	ENCA	0x0	RW	Clear the GPIO31-0 output enables

8.6.2.33 ENCB Register

GPIO Enable Register B Clear

OFFSET: 0x000000B8

INSTANCE 0 ADDRESS: 0x400100B8

GPIO Enable Register B Clear

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 437: ENCB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														ENCB																	

Table 438: ENCB Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17:0	ENCB	0x0	RW	Clear the GPIO49-32 output enables

8.6.2.34 STMRCAP Register

STIMER Capture Control

OFFSET: 0x000000BC

INSTANCE 0 ADDRESS: 0x400100BC

STIMER Capture trigger select and enable.

Table 439: STMRCAP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	STPOL3	STSEL3						RSVD	STPOL2	STSEL2						RSVD	STPOL1	STSEL1						RSVD	STPOL0	STSEL0					

Table 440: STMRCAP Register Bits

Bit	Name	Reset	RW	Description
31	RSVD	0x0	RO	RESERVED
30	STPOL3	0x0	RW	STIMER Capture 3 Polarity. CAPLH = 0x0 - Capture on low to high GPIO transition CAPHL = 0x1 - Capture on high to low GPIO transition
29:24	STSEL3	0x3f	RW	STIMER Capture 3 Select.
23	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 440: STMRCAP Register Bits

Bit	Name	Reset	RW	Description
22	STPOL2	0x0	RW	STIMER Capture 2 Polarity. CAPLH = 0x0 - Capture on low to high GPIO transition CAPHL = 0x1 - Capture on high to low GPIO transition
21:16	STSEL2	0x3f	RW	STIMER Capture 2 Select.
15	RSVD	0x0	RO	RESERVED
14	STPOL1	0x0	RW	STIMER Capture 1 Polarity. CAPLH = 0x0 - Capture on low to high GPIO transition CAPHL = 0x1 - Capture on high to low GPIO transition
13:8	STSEL1	0x3f	RW	STIMER Capture 1 Select.
7	RSVD	0x0	RO	RESERVED
6	STPOL0	0x0	RW	STIMER Capture 0 Polarity. CAPLH = 0x0 - Capture on low to high GPIO transition CAPHL = 0x1 - Capture on high to low GPIO transition
5:0	STSEL0	0x3f	RW	STIMER Capture 0 Select.

8.6.2.35 IOM0IRQ Register

IOM0 Flow Control IRQ Select

OFFSET: 0x000000C0

INSTANCE 0 ADDRESS: 0x400100C0

IOMSTR0 IRQ select for flow control.

Table 441: IOM0IRQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										IOM0IRQ					

Table 442: IOM0IRQ Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED
5:0	IOM0IRQ	0x3f	RW	IOMSTR0 IRQ pad select.

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2.36 IOM1IRQ Register

IOM1 Flow Control IRQ Select

OFFSET: 0x000000C4

INSTANCE 0 ADDRESS: 0x400100C4

IOMSTR1 IRQ select for flow control.

Table 443: IOM1IRQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										IOM1IRQ					

Table 444: IOM1IRQ Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED
5:0	IOM1IRQ	0x3f	RW	IOMSTR1 IRQ pad select.

8.6.2.37 IOM2IRQ Register

IOM2 Flow Control IRQ Select

OFFSET: 0x000000C8

INSTANCE 0 ADDRESS: 0x400100C8

IOMSTR2 IRQ select for flow control.

Table 445: IOM2IRQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										IOM2IRQ					

Table 446: IOM2IRQ Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED
5:0	IOM2IRQ	0x3f	RW	IOMSTR2 IRQ pad select.

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2.38 IOM3IRQ Register

IOM3 Flow Control IRQ Select

OFFSET: 0x000000CC

INSTANCE 0 ADDRESS: 0x400100CC

IOMSTR3 IRQ select for flow control.

Table 447: IOM3IRQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										IOM3IRQ					

Table 448: IOM3IRQ Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED
5:0	IOM3IRQ	0x3f	RW	IOMSTR3 IRQ pad select.

8.6.2.39 IOM4IRQ Register

IOM4 Flow Control IRQ Select

OFFSET: 0x000000D0

INSTANCE 0 ADDRESS: 0x400100D0

IOMSTR4 IRQ select for flow control.

Table 449: IOM4IRQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										IOM4IRQ					

Table 450: IOM4IRQ Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED
5:0	IOM4IRQ	0x3f	RW	IOMSTR4 IRQ pad select.

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2.40 IOM5IRQ Register

IOM5 Flow Control IRQ Select

OFFSET: 0x000000D4

INSTANCE 0 ADDRESS: 0x400100D4

IOMSTR5 IRQ select for flow control.

Table 451: IOM5IRQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										IOM5IRQ					

Table 452: IOM5IRQ Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED
5:0	IOM5IRQ	0x3f	RW	IOMSTR5 IRQ pad select.

8.6.2.41 LOOPBACK Register

IOM to IOS Loopback Control

OFFSET: 0x000000D8

INSTANCE 0 ADDRESS: 0x400100D8

IOM to IOS loopback control.

Table 453: LOOPBACK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																													LOOPBACK		

Table 454: LOOPBACK Register Bits

Bit	Name	Reset	RW	Description
31:3	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 454: LOOPBACK Register Bits

Bit	Name	Reset	RW	Description
2:0	LOOPBACK	0x0	RW	IOM to IOS loopback control. LOOP0 = 0x0 - Loop IOM0 to IOS LOOP1 = 0x1 - Loop IOM1 to IOS LOOP2 = 0x2 - Loop IOM2 to IOS LOOP3 = 0x3 - Loop IOM3 to IOS LOOP4 = 0x4 - Loop IOM4 to IOS LOOP5 = 0x5 - Loop IOM5 to IOS LOOPNONE = 0x6 - No loopback connections

8.6.2.42 GPIOOBS Register

GPIO Observation Mode Sample register

OFFSET: 0x000000DC

INSTANCE 0 ADDRESS: 0x400100DC

GPIO Observation mode sample register

Table 455: GPIOOBS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																OBS_DATA															

Table 456: GPIOOBS Register Bits

Bit	Name	Reset	RW	Description
31:16	RSVD	0x0	RO	RESERVED
15:0	OBS_DATA	0x0	RW	Sample of the data output on the GPIO observation port. May have async sampling issues, as the data is not synchronized to the read operation. Intended for debug purposes only

8.6.2.43 ALTPADCFGA Register

Alternate Pad Configuration reg0 (Pads 3,2,1,0)

OFFSET: 0x000000E0

INSTANCE 0 ADDRESS: 0x400100E0

This register has additional configuration control for pads 3, 2, 1, 0

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 457: ALTPADCFGA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			PAD3_SR	RSVD			PAD3_DS1	RSVD			PAD2_SR	RSVD			PAD2_DS1	RSVD			PAD1_SR	RSVD			PAD1_DS1	RSVD			PAD0_SR	RSVD			PAD0_DS1

Table 458: ALTPADCFGA Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	PAD3_SR	0x0	RW	Pad 3 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
27:25	RSVD	0x0	RO	RESERVED
24	PAD3_DS1	0x0	RW	Pad 3 high order drive strength selection. Used in conjunction with PAD3STRNG field to set the pad drive strength.
23:21	RSVD	0x0	RO	RESERVED
20	PAD2_SR	0x0	RW	Pad 2 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
19:17	RSVD	0x0	RO	RESERVED
16	PAD2_DS1	0x0	RW	Pad 2 high order drive strength selection. Used in conjunction with PAD2STRNG field to set the pad drive strength.
15:13	RSVD	0x0	RO	RESERVED
12	PAD1_SR	0x0	RW	Pad 1 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
11:9	RSVD	0x0	RO	RESERVED
8	PAD1_DS1	0x0	RW	Pad 1 high order drive strength selection. Used in conjunction with PAD1STRNG field to set the pad drive strength.
7:5	RSVD	0x0	RO	RESERVED
4	PAD0_SR	0x0	RW	Pad 0 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 458: ALTPADCFGA Register Bits

Bit	Name	Reset	RW	Description
3:1	RSVD	0x0	RO	RESERVED
0	PAD0_DS1	0x0	RW	Pad 0 high order drive strength selection. Used in conjunction with PAD0STRNG field to set the pad drive strength.

8.6.2.44 ALTPADCFGB Register

Alternate Pad Configuration reg1 (Pads 7,6,5,4)

OFFSET: 0x000000E4

INSTANCE 0 ADDRESS: 0x400100E4

This register has additional configuration control for pads 7, 6, 5, 4

Table 459: ALTPADCFGB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			PAD7_SR	RSVD			PAD7_DS1	RSVD			PAD6_SR	RSVD			PAD6_DS1	RSVD			PAD5_SR	RSVD			PAD5_DS1	RSVD			PAD4_SR	RSVD			PAD4_DS1

Table 460: ALTPADCFGB Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	PAD7_SR	0x0	RW	Pad 7 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
27:25	RSVD	0x0	RO	RESERVED
24	PAD7_DS1	0x0	RW	Pad 7 high order drive strength selection. Used in conjunction with PAD7STRNG field to set the pad drive strength.
23:21	RSVD	0x0	RO	RESERVED
20	PAD6_SR	0x0	RW	Pad 6 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
19:17	RSVD	0x0	RO	RESERVED
16	PAD6_DS1	0x0	RW	Pad 6 high order drive strength selection. Used in conjunction with PAD6STRNG field to set the pad drive strength.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 460: ALTPADCFGB Register Bits

Bit	Name	Reset	RW	Description
15:13	RSVD	0x0	RO	RESERVED
12	PAD5_SR	0x0	RW	Pad 5 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
11:9	RSVD	0x0	RO	RESERVED
8	PAD5_DS1	0x0	RW	Pad 5 high order drive strength selection. Used in conjunction with PAD5STRNG field to set the pad drive strength.
7:5	RSVD	0x0	RO	RESERVED
4	PAD4_SR	0x0	RW	Pad 4 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
3:1	RSVD	0x0	RO	RESERVED
0	PAD4_DS1	0x0	RW	Pad 4 high order drive strength selection. Used in conjunction with PAD4STRNG field to set the pad drive strength.

8.6.2.45 ALTPADCFGC Register

Alternate Pad Configuration reg2 (Pads 11,10,9,8)

OFFSET: 0x000000E8

INSTANCE 0 ADDRESS: 0x400100E8

This register has additional configuration control for pads 11, 10, 9, 8

Table 461: ALTPADCFGC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			PAD11_SR	RSVD			PAD11_DS1	RSVD			PAD10_SR	RSVD			PAD10_DS1	RSVD			PAD9_SR	RSVD			PAD9_DS1	RSVD			PAD8_SR	RSVD			PAD8_DS1

Table 462: ALTPADCFGC Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	PAD11_SR	0x0	RW	Pad 11 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 462: ALTPADCFGC Register Bits

Bit	Name	Reset	RW	Description
27:25	RSVD	0x0	RO	RESERVED
24	PAD11_DS1	0x0	RW	Pad 11 high order drive strength selection. Used in conjunction with PAD11STRNG field to set the pad drive strength.
23:21	RSVD	0x0	RO	RESERVED
20	PAD10_SR	0x0	RW	Pad 10 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
19:17	RSVD	0x0	RO	RESERVED
16	PAD10_DS1	0x0	RW	Pad 10 high order drive strength selection. Used in conjunction with PAD10STRNG field to set the pad drive strength.
15:13	RSVD	0x0	RO	RESERVED
12	PAD9_SR	0x0	RW	Pad 9 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
11:9	RSVD	0x0	RO	RESERVED
8	PAD9_DS1	0x0	RW	Pad 9 high order drive strength selection. Used in conjunction with PAD9STRNG field to set the pad drive strength.
7:5	RSVD	0x0	RO	RESERVED
4	PAD8_SR	0x0	RW	Pad 8 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
3:1	RSVD	0x0	RO	RESERVED
0	PAD8_DS1	0x0	RW	Pad 8 high order drive strength selection. Used in conjunction with PAD8STRNG field to set the pad drive strength.

8.6.2.46 ALTPADCFGD Register

Alternate Pad Configuration reg3 (Pads 15,14,13,12)

OFFSET: 0x000000EC

INSTANCE 0 ADDRESS: 0x400100EC

This register has additional configuration control for pads 15, 14, 13, 12

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 463: ALTPADCFGD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			PAD15_SR	RSVD			PAD15_DS1	RSVD			PAD14_SR	RSVD			PAD14_DS1	RSVD			PAD13_SR	RSVD			PAD13_DS1	RSVD			PAD12_SR	RSVD			PAD12_DS1

Table 464: ALTPADCFGD Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	PAD15_SR	0x0	RW	Pad 15 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
27:25	RSVD	0x0	RO	RESERVED
24	PAD15_DS1	0x0	RW	Pad 15 high order drive strength selection. Used in conjunction with PAD15STRNG field to set the pad drive strength.
23:21	RSVD	0x0	RO	RESERVED
20	PAD14_SR	0x0	RW	Pad 14 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
19:17	RSVD	0x0	RO	RESERVED
16	PAD14_DS1	0x0	RW	Pad 14 high order drive strength selection. Used in conjunction with PAD14STRNG field to set the pad drive strength.
15:13	RSVD	0x0	RO	RESERVED
12	PAD13_SR	0x0	RW	Pad 13 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
11:9	RSVD	0x0	RO	RESERVED
8	PAD13_DS1	0x0	RW	Pad 13 high order drive strength selection. Used in conjunction with PAD13STRNG field to set the pad drive strength.
7:5	RSVD	0x0	RO	RESERVED
4	PAD12_SR	0x0	RW	Pad 12 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 464: ALTPADCFGD Register Bits

Bit	Name	Reset	RW	Description
3:1	RSVD	0x0	RO	RESERVED
0	PAD12_DS1	0x0	RW	Pad 12 high order drive strength selection. Used in conjunction with PAD12STRNG field to set the pad drive strength.

8.6.2.47 ALTPADCFGE Register

Alternate Pad Configuration reg4 (Pads 19,18,17,16)

OFFSET: 0x000000F0

INSTANCE 0 ADDRESS: 0x400100F0

This register has additional configuration control for pads 19, 18, 17, 16

Table 465: ALTPADCFGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			PAD19_SR	RSVD			PAD19_DS1	RSVD			PAD18_SR	RSVD			PAD18_DS1	RSVD			PAD17_SR	RSVD			PAD17_DS1	RSVD			PAD16_SR	RSVD			PAD16_DS1

Table 466: ALTPADCFGE Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	PAD19_SR	0x0	RW	Pad 19 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
27:25	RSVD	0x0	RO	RESERVED
24	PAD19_DS1	0x0	RW	Pad 19 high order drive strength selection. Used in conjunction with PAD19STRNG field to set the pad drive strength.
23:21	RSVD	0x0	RO	RESERVED
20	PAD18_SR	0x0	RW	Pad 18 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
19:17	RSVD	0x0	RO	RESERVED
16	PAD18_DS1	0x0	RW	Pad 18 high order drive strength selection. Used in conjunction with PAD18STRNG field to set the pad drive strength.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 466: ALTPADCFGE Register Bits

Bit	Name	Reset	RW	Description
15:13	RSVD	0x0	RO	RESERVED
12	PAD17_SR	0x0	RW	Pad 17 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
11:9	RSVD	0x0	RO	RESERVED
8	PAD17_DS1	0x0	RW	Pad 17 high order drive strength selection. Used in conjunction with PAD17STRNG field to set the pad drive strength.
7:5	RSVD	0x0	RO	RESERVED
4	PAD16_SR	0x0	RW	Pad 16 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
3:1	RSVD	0x0	RO	RESERVED
0	PAD16_DS1	0x0	RW	Pad 16 high order drive strength selection. Used in conjunction with PAD16STRNG field to set the pad drive strength.

8.6.2.48 ALTPADCFGF Register

Alternate Pad Configuration reg5 (Pads 23,22,21,20)

OFFSET: 0x000000F4

INSTANCE 0 ADDRESS: 0x400100F4

This register has additional configuration control for pads 23, 22, 21, 20

Table 467: ALTPADCFGF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			RSVD	RSVD			RSVD	RSVD			PAD22_SR	RSVD			PAD22_DS1	RSVD			PAD21_SR	RSVD			PAD21_DS1	RSVD			PAD20_SR	RSVD			PAD20_DS1

Table 468: ALTPADCFGF Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 468: ALTPADCFGF Register Bits

Bit	Name	Reset	RW	Description
27:25	RSVD	0x0	RO	RESERVED
24	RSVD	0x0	RW	RESERVED
23:21	RSVD	0x0	RO	RESERVED
20	PAD22_SR	0x0	RW	Pad 22 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
19:17	RSVD	0x0	RO	RESERVED
16	PAD22_DS1	0x0	RW	Pad 22 high order drive strength selection. Used in conjunction with PAD22STRNG field to set the pad drive strength.
15:13	RSVD	0x0	RO	RESERVED
12	PAD21_SR	0x0	RW	Pad 21 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
11:9	RSVD	0x0	RO	RESERVED
8	PAD21_DS1	0x0	RW	Pad 21 high order drive strength selection. Used in conjunction with PAD21STRNG field to set the pad drive strength.
7:5	RSVD	0x0	RO	RESERVED
4	PAD20_SR	0x0	RW	Pad 20 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
3:1	RSVD	0x0	RO	RESERVED
0	PAD20_DS1	0x0	RW	Pad 20 high order drive strength selection. Used in conjunction with PAD20STRNG field to set the pad drive strength.

8.6.2.49 ALTPADCFGG Register

Alternate Pad Configuration reg6 (Pads 27,26,25,24)

OFFSET: 0x000000F8

INSTANCE 0 ADDRESS: 0x400100F8

This register has additional configuration control for pads 27, 26, 25, 24

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 469: ALTPADCFGG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			RSVD	RSVD			RSVD	RSVD			RSVD	RSVD			RSVD	RSVD			RSVD	RSVD			RSVD	RSVD			PAD24_SR	RSVD			PAD24_DS1

Table 470: ALTPADCFGG Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	RSVD	0x0	RW	RESERVED
27:25	RSVD	0x0	RO	RESERVED
24	RSVD	0x0	RW	RESERVED
23:21	RSVD	0x0	RO	RESERVED
20	RSVD	0x0	RW	RESERVED
19:17	RSVD	0x0	RO	RESERVED
16	RSVD	0x0	RW	RESERVED
15:13	RSVD	0x0	RO	RESERVED
12	RSVD	0x0	RW	RESERVED
11:9	RSVD	0x0	RO	RESERVED
8	RSVD	0x0	RW	RESERVED
7:5	RSVD	0x0	RO	RESERVED
4	PAD24_SR	0x0	RW	Pad 24 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
3:1	RSVD	0x0	RO	RESERVED
0	PAD24_DS1	0x0	RW	Pad 24 high order drive strength selection. Used in conjunction with PAD24STRNG field to set the pad drive strength.

8.6.2.50 ALTPADCFGH Register

Alternate Pad Configuration reg7 (Pads 31,30,29,28)

OFFSET: 0x000000FC

©2017 Ambiq Micro, Inc.
All rights reserved.

INSTANCE 0 ADDRESS: 0x400100FC

This register has additional configuration control for pads 31, 30, 29, 28

Table 471: ALTPADCFGH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			RSVD	RSVD			RSVD	RSVD			PAD30_SR	RSVD			PAD30_DS1	RSVD			PAD29_SR	RSVD			PAD29_DS1	RSVD			RSVD	RSVD			RSVD

Table 472: ALTPADCFGH Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	RSVD	0x0	RW	RESERVED
27:25	RSVD	0x0	RO	RESERVED
24	RSVD	0x0	RW	RESERVED
23:21	RSVD	0x0	RO	RESERVED
20	PAD30_SR	0x0	RW	Pad 30 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
19:17	RSVD	0x0	RO	RESERVED
16	PAD30_DS1	0x0	RW	Pad 30 high order drive strength selection. Used in conjunction with PAD30STRNG field to set the pad drive strength.
15:13	RSVD	0x0	RO	RESERVED
12	PAD29_SR	0x0	RW	Pad 29 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
11:9	RSVD	0x0	RO	RESERVED
8	PAD29_DS1	0x0	RW	Pad 29 high order drive strength selection. Used in conjunction with PAD29STRNG field to set the pad drive strength.
7:5	RSVD	0x0	RO	RESERVED
4	RSVD	0x0	RW	RESERVED
3:1	RSVD	0x0	RO	RESERVED
0	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2.51 ALTPADCFGI Register

Alternate Pad Configuration reg8 (Pads 35,34,33,32)

OFFSET: 0x00000100

INSTANCE 0 ADDRESS: 0x40010100

This register has additional configuration control for pads 35, 34, 33, 32

Table 473: ALTPADCFGI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			PAD35_SR	RSVD			PAD35_DS1	RSVD			RSVD	RSVD			RSVD	RSVD			RSVD	RSVD			RSVD	RSVD			RSVD	RSVD			RSVD

Table 474: ALTPADCFGI Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	PAD35_SR	0x0	RW	Pad 35 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
27:25	RSVD	0x0	RO	RESERVED
24	PAD35_DS1	0x0	RW	Pad 35 high order drive strength selection. Used in conjunction with PAD35STRNG field to set the pad drive strength.
23:21	RSVD	0x0	RO	RESERVED
20	RSVD	0x0	RW	RESERVED
19:17	RSVD	0x0	RO	RESERVED
16	RSVD	0x0	RW	RESERVED
15:13	RSVD	0x0	RO	RESERVED
12	RSVD	0x0	RW	RESERVED
11:9	RSVD	0x0	RO	RESERVED
8	RSVD	0x0	RW	RESERVED
7:5	RSVD	0x0	RO	RESERVED
4	RSVD	0x0	RW	RESERVED
3:1	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 474: ALTPADCFGI Register Bits

Bit	Name	Reset	RW	Description
0	RSVD	0x0	RW	RESERVED

8.6.2.52 ALTPADCFGJ Register

Alternate Pad Configuration reg9 (Pads 39,38,37,36)

OFFSET: 0x00000104

INSTANCE 0 ADDRESS: 0x40010104

This register has additional configuration control for pads 39, 38, 37, 36

Table 475: ALTPADCFGJ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			PAD39_SR	RSVD			PAD39_DS1	RSVD			RSVD	RSVD			RSVD	RSVD			RSVD	RSVD			RSVD	RSVD			PAD36_SR	RSVD			PAD36_DS1

Table 476: ALTPADCFGJ Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	PAD39_SR	0x0	RW	Pad 39 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
27:25	RSVD	0x0	RO	RESERVED
24	PAD39_DS1	0x0	RW	Pad 39 high order drive strength selection. Used in conjunction with PAD39STRNG field to set the pad drive strength.
23:21	RSVD	0x0	RO	RESERVED
20	RSVD	0x0	RW	RESERVED
19:17	RSVD	0x0	RO	RESERVED
16	RSVD	0x0	RW	RESERVED
15:13	RSVD	0x0	RO	RESERVED
12	RSVD	0x0	RW	RESERVED
11:9	RSVD	0x0	RO	RESERVED
8	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 476: ALTPADCFGJ Register Bits

Bit	Name	Reset	RW	Description
7:5	RSVD	0x0	RO	RESERVED
4	PAD36_SR	0x0	RW	Pad 36 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
3:1	RSVD	0x0	RO	RESERVED
0	PAD36_DS1	0x0	RW	Pad 36 high order drive strength selection. Used in conjunction with PAD36STRNG field to set the pad drive strength.

8.6.2.53 ALTPADCFGK Register

Alternate Pad Configuration reg10 (Pads 43,42,41,40)

OFFSET: 0x00000108

INSTANCE 0 ADDRESS: 0x40010108

This register has additional configuration control for pads 43, 42, 41, 40

Table 477: ALTPADCFGK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			RSVD	RSVD			RSVD	RSVD			PAD42_SR	RSVD			PAD42_DS1	RSVD			PAD41_SR	RSVD			PAD41_DS1	RSVD			PAD40_SR	RSVD			PAD40_DS1

Table 478: ALTPADCFGK Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED
28	RSVD	0x0	RW	RESERVED
27:25	RSVD	0x0	RO	RESERVED
24	RSVD	0x0	RW	RESERVED
23:21	RSVD	0x0	RO	RESERVED
20	PAD42_SR	0x0	RW	Pad 42 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
19:17	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 478: ALTPADCFGK Register Bits

Bit	Name	Reset	RW	Description
16	PAD42_DS1	0x0	RW	Pad 42 high order drive strength selection. Used in conjunction with PAD42STRNG field to set the pad drive strength.
15:13	RSVD	0x0	RO	RESERVED
12	PAD41_SR	0x0	RW	Pad 41 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
11:9	RSVD	0x0	RO	RESERVED
8	PAD41_DS1	0x0	RW	Pad 41 high order drive strength selection. Used in conjunction with PAD41STRNG field to set the pad drive strength.
7:5	RSVD	0x0	RO	RESERVED
4	PAD40_SR	0x0	RW	Pad 40 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
3:1	RSVD	0x0	RO	RESERVED
0	PAD40_DS1	0x0	RW	Pad 40 high order drive strength selection. Used in conjunction with PAD40STRNG field to set the pad drive strength.

8.6.2.54 ALTPADCFGL Register

Alternate Pad Configuration reg11 (Pads 47,46,45,44)

OFFSET: 0x0000010C

INSTANCE 0 ADDRESS: 0x4001010C

This register has additional configuration control for pads 47, 46, 45, 44

Table 479: ALTPADCFGL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD			PAD47_SR	RSVD			PAD47_DS1	RSVD			PAD46_SR	RSVD			PAD46_DS1	RSVD			PAD45_SR	RSVD			PAD45_DS1	RSVD			PAD44_SR	RSVD			PAD44_DS1

Table 480: ALTPADCFGL Register Bits

Bit	Name	Reset	RW	Description
31:29	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 480: ALTPADCFGL Register Bits

Bit	Name	Reset	RW	Description
28	PAD47_SR	0x0	RW	Pad 47 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
27:25	RSVD	0x0	RO	RESERVED
24	PAD47_DS1	0x0	RW	Pad 47 high order drive strength selection. Used in conjunction with PAD47STRNG field to set the pad drive strength.
23:21	RSVD	0x0	RO	RESERVED
20	PAD46_SR	0x0	RW	Pad 46 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
19:17	RSVD	0x0	RO	RESERVED
16	PAD46_DS1	0x0	RW	Pad 46 high order drive strength selection. Used in conjunction with PAD46STRNG field to set the pad drive strength.
15:13	RSVD	0x0	RO	RESERVED
12	PAD45_SR	0x0	RW	Pad 45 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
11:9	RSVD	0x0	RO	RESERVED
8	PAD45_DS1	0x0	RW	Pad 45 high order drive strength selection. Used in conjunction with PAD45STRNG field to set the pad drive strength.
7:5	RSVD	0x0	RO	RESERVED
4	PAD44_SR	0x0	RW	Pad 44 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
3:1	RSVD	0x0	RO	RESERVED
0	PAD44_DS1	0x0	RW	Pad 44 high order drive strength selection. Used in conjunction with PAD44STRNG field to set the pad drive strength.

8.6.2.55 ALTPADCFGM Register

Alternate Pad Configuration reg12 (Pads 49,48)

OFFSET: 0x00000110

INSTANCE 0 ADDRESS: 0x40010110

This register has additional configuration control for pads 49, 48

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 481: ALTPADCFGM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																			PAD49_SR	RSVD			PAD49_DS1	RSVD			PAD48_SR	RSVD			PAD48_DS1

Table 482: ALTPADCFGM Register Bits

Bit	Name	Reset	RW	Description
31:13	RSVD	0x0	RO	RESERVED
12	PAD49_SR	0x0	RW	Pad 49 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
11:9	RSVD	0x0	RO	RESERVED
8	PAD49_DS1	0x0	RW	Pad 49 high order drive strength selection. Used in conjunction with PAD49STRNG field to set the pad drive strength.
7:5	RSVD	0x0	RO	RESERVED
4	PAD48_SR	0x0	RW	Pad 48 slew rate selection. SR_EN = 0x1 - Enables Slew rate control on pad
3:1	RSVD	0x0	RO	RESERVED
0	PAD48_DS1	0x0	RW	Pad 48 high order drive strength selection. Used in conjunction with PAD48STRNG field to set the pad drive strength.

8.6.2.56 INT0EN Register

GPIO Interrupt Registers 31-0: Enable

OFFSET: 0x00000200

INSTANCE 0 ADDRESS: 0x40010200

Set bits in this register to allow this module to generate the corresponding interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 483: INT0EN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	GPIO30	GPIO29	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 484: INT0EN Register Bits

Bit	Name	Reset	RW	Description
31	RSVD	0x0	RW	RESERVED
30	GPIO30	0x0	RW	GPIO30 interrupt.
29	GPIO29	0x0	RW	GPIO29 interrupt.
28	RSVD	0x0	RW	RESERVED
27	RSVD	0x0	RW	RESERVED
26	RSVD	0x0	RW	RESERVED
25	RSVD	0x0	RW	RESERVED
24	RSVD	0x0	RW	RESERVED
23	RSVD	0x0	RW	RESERVED
22	GPIO22	0x0	RW	GPIO22 interrupt.
21	GPIO21	0x0	RW	GPIO21 interrupt.
20	GPIO20	0x0	RW	GPIO20 interrupt.
19	GPIO19	0x0	RW	GPIO19 interrupt.
18	GPIO18	0x0	RW	GPIO18interrupt.
17	GPIO17	0x0	RW	GPIO17 interrupt.
16	GPIO16	0x0	RW	GPIO16 interrupt.
15	GPIO15	0x0	RW	GPIO15 interrupt.
14	GPIO14	0x0	RW	GPIO14 interrupt.
13	GPIO13	0x0	RW	GPIO13 interrupt.
12	GPIO12	0x0	RW	GPIO12 interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 484: INT0EN Register Bits

Bit	Name	Reset	RW	Description
11	GPIO11	0x0	RW	GPIO11 interrupt.
10	GPIO10	0x0	RW	GPIO10 interrupt.
9	GPIO9	0x0	RW	GPIO9 interrupt.
8	GPIO8	0x0	RW	GPIO8 interrupt.
7	GPIO7	0x0	RW	GPIO7 interrupt.
6	GPIO6	0x0	RW	GPIO6 interrupt.
5	GPIO5	0x0	RW	GPIO5 interrupt.
4	GPIO4	0x0	RW	GPIO4 interrupt.
3	GPIO3	0x0	RW	GPIO3 interrupt.
2	GPIO2	0x0	RW	GPIO2 interrupt.
1	GPIO1	0x0	RW	GPIO1 interrupt.
0	GPIO0	0x0	RW	GPIO0 interrupt.

8.6.2.57 INT0STAT Register

GPIO Interrupt Registers 31-0: Status

OFFSET: 0x00000204

INSTANCE 0 ADDRESS: 0x40010204

Read bits from this register to discover the cause of a recent interrupt.

Table 485: INT0STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	GPIO30	GPIO29	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 486: INT0STAT Register Bits

Bit	Name	Reset	RW	Description
31	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 486: INT0STAT Register Bits

Bit	Name	Reset	RW	Description
30	GPIO30	0x0	RW	GPIO30 interrupt.
29	GPIO29	0x0	RW	GPIO29 interrupt.
28	RSVD	0x0	RW	RESERVED
27	RSVD	0x0	RW	RESERVED
26	RSVD	0x0	RW	RESERVED
25	RSVD	0x0	RW	RESERVED
24	RSVD	0x0	RW	RESERVED
23	RSVD	0x0	RW	RESERVED
22	GPIO22	0x0	RW	GPIO22 interrupt.
21	GPIO21	0x0	RW	GPIO21 interrupt.
20	GPIO20	0x0	RW	GPIO20 interrupt.
19	GPIO19	0x0	RW	GPIO19 interrupt.
18	GPIO18	0x0	RW	GPIO18interrupt.
17	GPIO17	0x0	RW	GPIO17 interrupt.
16	GPIO16	0x0	RW	GPIO16 interrupt.
15	GPIO15	0x0	RW	GPIO15 interrupt.
14	GPIO14	0x0	RW	GPIO14 interrupt.
13	GPIO13	0x0	RW	GPIO13 interrupt.
12	GPIO12	0x0	RW	GPIO12 interrupt.
11	GPIO11	0x0	RW	GPIO11 interrupt.
10	GPIO10	0x0	RW	GPIO10 interrupt.
9	GPIO9	0x0	RW	GPIO9 interrupt.
8	GPIO8	0x0	RW	GPIO8 interrupt.
7	GPIO7	0x0	RW	GPIO7 interrupt.
6	GPIO6	0x0	RW	GPIO6 interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 486: INT0STAT Register Bits

Bit	Name	Reset	RW	Description
5	GPIO5	0x0	RW	GPIO5 interrupt.
4	GPIO4	0x0	RW	GPIO4 interrupt.
3	GPIO3	0x0	RW	GPIO3 interrupt.
2	GPIO2	0x0	RW	GPIO2 interrupt.
1	GPIO1	0x0	RW	GPIO1 interrupt.
0	GPIO0	0x0	RW	GPIO0 interrupt.

8.6.2.58 INT0CLR Register

GPIO Interrupt Registers 31-0: Clear

OFFSET: 0x00000208

INSTANCE 0 ADDRESS: 0x40010208

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 487: INT0CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	GPIO30	GPIO29	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 488: INT0CLR Register Bits

Bit	Name	Reset	RW	Description
31	RSVD	0x0	RW	RESERVED
30	GPIO30	0x0	RW	GPIO30 interrupt.
29	GPIO29	0x0	RW	GPIO29 interrupt.
28	RSVD	0x0	RW	RESERVED
27	RSVD	0x0	RW	RESERVED
26	RSVD	0x0	RW	RESERVED
25	RSVD	0x0	RW	RESERVED
24	RSVD	0x0	RW	RESERVED
23	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 488: INT0CLR Register Bits

Bit	Name	Reset	RW	Description
22	GPIO22	0x0	RW	GPIO22 interrupt.
21	GPIO21	0x0	RW	GPIO21 interrupt.
20	GPIO20	0x0	RW	GPIO20 interrupt.
19	GPIO19	0x0	RW	GPIO19 interrupt.
18	GPIO18	0x0	RW	GPIO18interrupt.
17	GPIO17	0x0	RW	GPIO17 interrupt.
16	GPIO16	0x0	RW	GPIO16 interrupt.
15	GPIO15	0x0	RW	GPIO15 interrupt.
14	GPIO14	0x0	RW	GPIO14 interrupt.
13	GPIO13	0x0	RW	GPIO13 interrupt.
12	GPIO12	0x0	RW	GPIO12 interrupt.
11	GPIO11	0x0	RW	GPIO11 interrupt.
10	GPIO10	0x0	RW	GPIO10 interrupt.
9	GPIO9	0x0	RW	GPIO9 interrupt.
8	GPIO8	0x0	RW	GPIO8 interrupt.
7	GPIO7	0x0	RW	GPIO7 interrupt.
6	GPIO6	0x0	RW	GPIO6 interrupt.
5	GPIO5	0x0	RW	GPIO5 interrupt.
4	GPIO4	0x0	RW	GPIO4 interrupt.
3	GPIO3	0x0	RW	GPIO3 interrupt.
2	GPIO2	0x0	RW	GPIO2 interrupt.
1	GPIO1	0x0	RW	GPIO1 interrupt.
0	GPIO0	0x0	RW	GPIO0 interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2.59 INT0SET Register

GPIO Interrupt Registers 31-0: Set

OFFSET: 0x0000020C

INSTANCE 0 ADDRESS: 0x4001020C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 489: INT0SET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	GPIO30	GPIO29	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 490: INT0SET Register Bits

Bit	Name	Reset	RW	Description
31	RSVD	0x0	RW	RESERVED
30	GPIO30	0x0	RW	GPIO30 interrupt.
29	GPIO29	0x0	RW	GPIO29 interrupt.
28	RSVD	0x0	RW	RESERVED
27	RSVD	0x0	RW	RESERVED
26	RSVD	0x0	RW	RESERVED
25	RSVD	0x0	RW	RESERVED
24	RSVD	0x0	RW	RESERVED
23	RSVD	0x0	RW	RESERVED
22	GPIO22	0x0	RW	GPIO22 interrupt.
21	GPIO21	0x0	RW	GPIO21 interrupt.
20	GPIO20	0x0	RW	GPIO20 interrupt.
19	GPIO19	0x0	RW	GPIO19 interrupt.
18	GPIO18	0x0	RW	GPIO18interrupt.
17	GPIO17	0x0	RW	GPIO17 interrupt.
16	GPIO16	0x0	RW	GPIO16 interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 490: INT0SET Register Bits

Bit	Name	Reset	RW	Description
15	GPIO15	0x0	RW	GPIO15 interrupt.
14	GPIO14	0x0	RW	GPIO14 interrupt.
13	GPIO13	0x0	RW	GPIO13 interrupt.
12	GPIO12	0x0	RW	GPIO12 interrupt.
11	GPIO11	0x0	RW	GPIO11 interrupt.
10	GPIO10	0x0	RW	GPIO10 interrupt.
9	GPIO9	0x0	RW	GPIO9 interrupt.
8	GPIO8	0x0	RW	GPIO8 interrupt.
7	GPIO7	0x0	RW	GPIO7 interrupt.
6	GPIO6	0x0	RW	GPIO6 interrupt.
5	GPIO5	0x0	RW	GPIO5 interrupt.
4	GPIO4	0x0	RW	GPIO4 interrupt.
3	GPIO3	0x0	RW	GPIO3 interrupt.
2	GPIO2	0x0	RW	GPIO2 interrupt.
1	GPIO1	0x0	RW	GPIO1 interrupt.
0	GPIO0	0x0	RW	GPIO0 interrupt.

8.6.2.60 INT1EN Register

GPIO Interrupt Registers 49-32: Enable

OFFSET: 0x00000210

INSTANCE 0 ADDRESS: 0x40010210

Set bits in this register to allow this module to generate the corresponding interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 491: INT1EN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														RSVD	RSVD	RSVD	RSVD	RSVD	GPIO44	RSVD	RSVD	GPIO41	GPIO40	GPIO39	RSVD	RSVD	GPIO36	GPIO35	RSVD	RSVD	RSVD

Table 492: INT1EN Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17	RSVD	0x0	RW	RESERVED
16	RSVD	0x0	RW	RESERVED
15	RSVD	0x0	RW	RESERVED
14	RSVD	0x0	RW	RESERVED
13	RSVD	0x0	RW	RESERVED
12	GPIO44	0x0	RW	GPIO44 interrupt.
11	RSVD	0x0	RW	RESERVED
10	RSVD	0x0	RW	RESERVED
9	GPIO41	0x0	RW	GPIO41 interrupt.
8	GPIO40	0x0	RW	GPIO40 interrupt.
7	GPIO39	0x0	RW	GPIO39 interrupt.
6	RSVD	0x0	RW	RESERVED
5	RSVD	0x0	RW	RESERVED
4	GPIO36	0x0	RW	GPIO36 interrupt.
3	GPIO35	0x0	RW	GPIO35 interrupt.
2	RSVD	0x0	RW	RESERVED
1	RSVD	0x0	RW	RESERVED
0	RSVD	0x0	RW	RESERVED

8.6.2.61 INT1STAT Register

GPIO Interrupt Registers 49-32: Status

OFFSET: 0x00000214

INSTANCE 0 ADDRESS: 0x40010214

©2017 Ambiq Micro, Inc.
All rights reserved.

Read bits from this register to discover the cause of a recent interrupt.

Table 493: INT1STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														RSVD	RSVD	RSVD	RSVD	RSVD	GPIO44	RSVD	RSVD	GPIO41	GPIO40	GPIO39	RSVD	RSVD	GPIO36	GPIO35	RSVD	RSVD	RSVD

Table 494: INT1STAT Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17	RSVD	0x0	RW	RESERVED
16	RSVD	0x0	RW	RESERVED
15	RSVD	0x0	RW	RESERVED
14	RSVD	0x0	RW	RESERVED
13	RSVD	0x0	RW	RESERVED
12	GPIO44	0x0	RW	GPIO44 interrupt.
11	RSVD	0x0	RW	RESERVED
10	GPIO42 RSVD	0x0	RW	RESERVED
9	GPIO41	0x0	RW	GPIO41 interrupt.
8	GPIO40	0x0	RW	GPIO40 interrupt.
7	GPIO39	0x0	RW	GPIO39 interrupt.
6	RSVD	0x0	RW	RESERVED
5	RSVD	0x0	RW	RESERVED
4	GPIO36	0x0	RW	GPIO36 interrupt.
3	GPIO35	0x0	RW	GPIO35 interrupt.
2	RSVD	0x0	RW	RESERVED
1	RSVD	0x0	RW	RESERVED
0	RSVD	0x0	RW	RESERVED

8.6.2.62 INT1CLR Register

GPIO Interrupt Registers 49-32: Clear

OFFSET: 0x00000218

©2017 Ambiq Micro, Inc.
All rights reserved.

INSTANCE 0 ADDRESS: 0x40010218

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 495: INT1CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														RSVD	RSVD	RSVD	RSVD	RSVD	GPIO44	RSVD	RSVD	GPIO41	GPIO40	GPIO39	RSVD	RSVD	GPIO36	GPIO35	RSVD	RSVD	RSVD

Table 496: INT1CLR Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17	RSVD	0x0	RW	RESERVED
16	RSVD	0x0	RW	RESERVED
15	RSVD	0x0	RW	RESERVED
14	RSVD	0x0	RW	RESERVED
13	RSVD	0x0	RW	RESERVED
12	GPIO44	0x0	RW	GPIO44 interrupt.
11	RSVD	0x0	RW	RESERVED
10	RSVD	0x0	RW	RESERVED
9	GPIO41	0x0	RW	GPIO41 interrupt.
8	GPIO40	0x0	RW	GPIO40 interrupt.
7	GPIO39	0x0	RW	GPIO39 interrupt.
6	RSVD	0x0	RW	RESERVED
5	RSVD	0x0	RW	RESERVED
4	GPIO36	0x0	RW	GPIO36 interrupt.
3	GPIO35	0x0	RW	GPIO35 interrupt.
2	RSVD	0x0	RW	RESERVED
1	RSVD	0x0	RW	RESERVED
0	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

8.6.2.63 INT1SET Register

GPIO Interrupt Registers 49-32: Set

OFFSET: 0x0000021C

INSTANCE 0 ADDRESS: 0x4001021C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 497: INT1SET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														RSVD	RSVD	RSVD	RSVD	RSVD	GPIO44 RSVD	RSVD	RSVD	GPIO41	GPIO40	GPIO39	RSVD	RSVD	GPIO36	GPIO35	RSVD	RSVD	RSVD

Table 498: INT1SET Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17	RSVD	0x0	RW	RESERVED
16	RSVD	0x0	RW	RESERVED
15	RSVD	0x0	RW	RESERVED
14	RSVD	0x0	RW	RESERVED
13	RSVD	0x0	RW	RESERVED
12	GPIO44	0x0	RW	GPIO44 interrupt.
11	RSVD	0x0	RW	RESERVED
10	RSVD	0x0	RW	RESERVED
9	GPIO41	0x0	RW	GPIO41 interrupt.
8	GPIO40	0x0	RW	GPIO40 interrupt.
7	GPIO39	0x0	RW	GPIO39 interrupt.
6	RSVD	0x0	RW	RESERVED
5	RSVD	0x0	RW	RESERVED
4	GPIO36	0x0	RW	GPIO36 interrupt.
3	GPIO35	0x0	RW	GPIO35 interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 498: INT1SET Register Bits

Bit	Name	Reset	RW	Description
2	RSVD	0x0	RW	RESERVED
1	RSVD	0x0	RW	RESERVED
0	RSVD	0x0	RW	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

9. Clock Generator and Real Time Clock Module

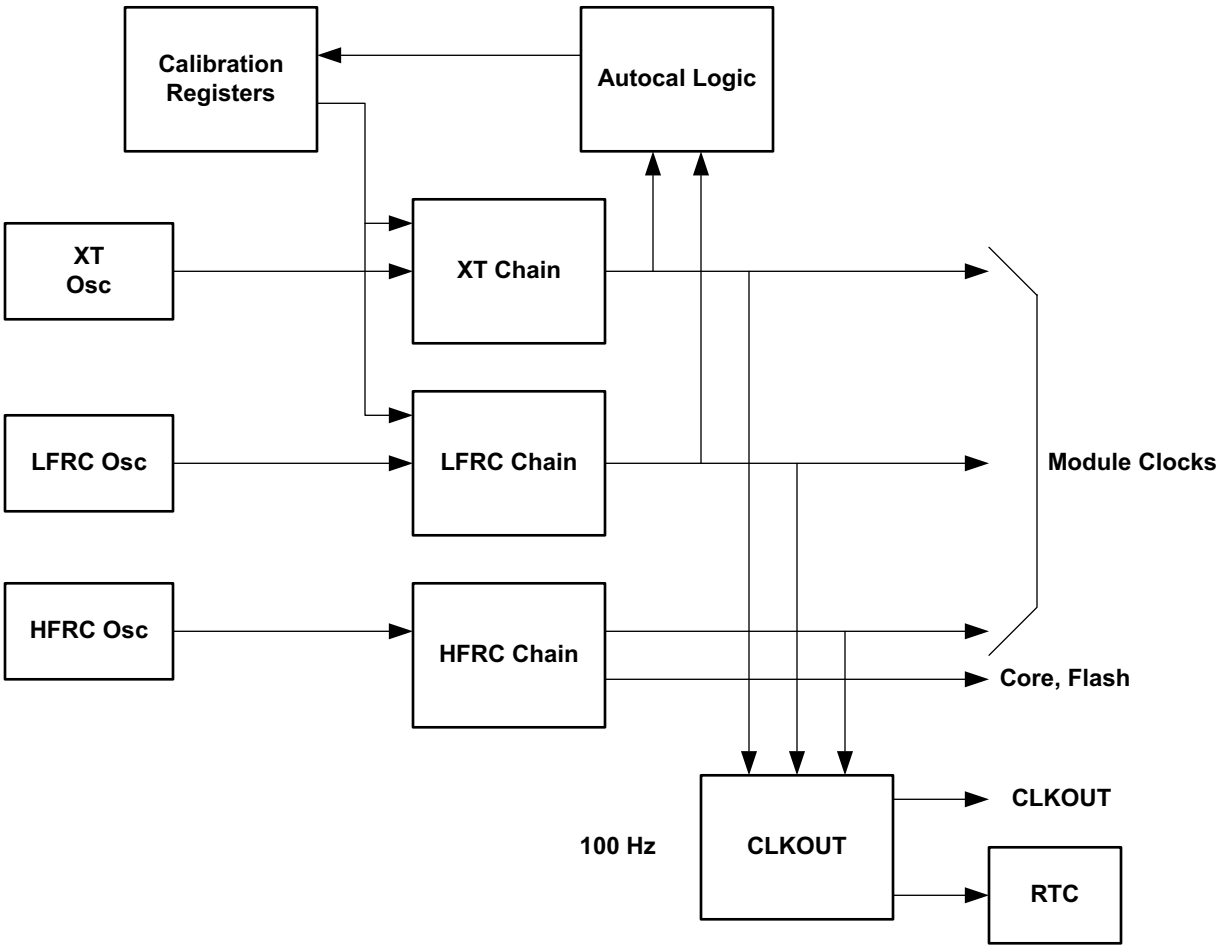


Figure 55. Block diagram for the Clock Generator and Real Time Clock Module

9.1 Clock Generator

9.1.1 Functional Overview

The Clock Generator Module, shown in Figure 55, supplies all clocks required by the Apollo2 Blue . These clocks are derived from one of three fundamental clock sources: a high precision crystal controlled oscillator (XT), a low power 1 kHz RC oscillator (LFRC) and a high frequency 48 MHz oscillator (HFRC).

A clockCLKOUT, generated from any of the oscillators, may be configured and driven onto an external pin.CLKOUT also drives the Real Time Clock (RTC) Module and other internal clock nodes.

The Clock Generator automatically controls the enabling of the oscillators, so that they are only powered up and used when requested by another module. This allows minimal power consumption without complex software intervention, so that software does not need to manage any enabling or disabling of the oscillators. As an example, an I^2C/SPI Master requires the HFRC in order to generate the serial interface clock. If a transfer is initiated and the processor is put into Deep Sleep mode, the HFRC will remain active

©2017 Ambiq Micro, Inc.
All rights reserved.

until the I/O transfer is completed. At that point the HFRC will be powered down without requiring any software intervention.

9.1.2 Low Frequency RC Oscillator (LFRC)

The low power LFRC, with a nominal frequency of 1024 Hz, is used when short term frequency accuracy is not important. It also supplies clocks for some basic state machines and is always enabled. Calibration logic is included.

9.1.2.1 LFRC Oscillator Digital Calibration

The LFRC Oscillator includes a patented Distributed Digital Calibration function similar to that of the XT Oscillator (Section 9.1.3.2). Because the LFRC Oscillator has a greater fundamental variability, the required range of calibration is much larger. When the 1024 Hz RC oscillator is selected, the clock at the 512 Hz level of the divider chain is modified on a selectable interval using the calibration value CALRC in the REG_CLKGEN_CALRC Register. Clock pulses are either added or subtracted to ensure accuracy of the LFRC. CALRC cycles of the 512 Hz clock are gated (negative calibration) or replaced by 1024 Hz pulses (positive calibration) within every 1024 second calibration period. Each step in CALRC modifies the clock frequency by 1.907 ppm, with a maximum adjustment of +249,954/-249,955 ppm (±25%).

The pulses which are added to or subtracted from the 512 Hz clock are spread evenly over each 1024 second period using the Ambiq Micro patented Distributed Calibration algorithm. This ensures that in LFRC mode the maximum cycle-to-cycle jitter in any clock of a frequency 512 Hz or lower caused by calibration will be no more than one 512 Hz period (~2 ms). This maximum jitter applies to all clocks in the Apollo2 Blue which use the LFRC.

Note that since the 512 Hz LFRC clock is calibrated, the 1024 Hz LFRC is an uncalibrated clock. This may be a useful selection in some cases.

9.1.2.2 LFRC Calibration Process

The LFRC oscillator calibration value is determined by the following process:

1. Set the CALRC field to 0 to insure calibration is not occurring.
2. Select the LFRC oscillator by setting the REG_CLKGEN_OCTRL_OSEL bit to 1.
3. Select the LFRC or a division of it on a CLKOUT pad.
4. Measure the frequency Fmeas at the CLKOUT pad.
5. Compute the adjustment value required in ppm as ((Fnom – Fmeas)*1000000)/Fmeas = PAdj
6. Compute the adjustment value in steps as PAdj/(1000000/2^19) = PAdj/(1.90735) = Adj
7. Compare Adj value with min/max range of -249,955 to 249,954
8. If target Adj is within min and max, set CALRC = Adj
9. Otherwise, the LFRC frequency is too low to be calibrated

9.1.3 High Precision XT Oscillator (XT)

The high accuracy XT Oscillator is tuned to an external 32.768 kHz crystal, and has a nominal frequency of 32.768 kHz. It is used when frequency accuracy is critically important. Because a crystal oscillator uses a significant amount of power, the XT is only enabled when an internal module is using it. Digital calibration logic is included.The output of the XT oscillator may be digitally calibrated to ±1 ppm (part per million).

It should be noted that the XT oscillator is also optional if the requirements of the design can tolerate the internal LFRC/HFRC oscillator specifications. It should also be noted that external capacitors are not required to tune an internal divided clock of the crystal input to achieve a precise scaling of 32.768kHz. This is handled within the Apollo2 Blue.

©2017 Ambiq Micro, Inc.
All rights reserved.

NOTE: The XTAL is highly sensitive to external leakage on the XI pin. Therefore it is recommended to minimize the components on XI and to use extremely low leakage load capacitors.

9.1.3.1 XT Oscillator Digital Calibration

The XT Oscillator includes a Distributed Digital Calibration function. When the 32 kHz XT oscillator is selected, the clock at the 16 kHz level of the divider chain is modified on a selectable interval using the calibration value CALXT in the REG_CLKGEN_CALXT Register. Clock pulses are either added or subtracted to ensure accuracy of the XT. CALXT cycles of the 16 kHz clock are gated (negative calibration) or replaced by 32 kHz pulses (positive calibration) within every 64 second calibration period. Each step in CALXT modifies the clock frequency by 0.9535 ppm, with a maximum adjustment of +975/-976 ppm (±0.1%).

The pulses which are added to or subtracted from the 16 kHz clock are spread evenly over each 64 second period using the Ambiq Micro patented Distributed Calibration algorithm. This insures that in XT mode the maximum cycle-to-cycle jitter in any clock of a frequency 16 kHz or lower caused by calibration will be no more than one 16 kHz period (~60 us). This maximum jitter applies to all clocks in the Apollo2 Blue which use the XT.

Note that since the 16 kHz XT clock is calibrated, the 32 kHz XT is an uncalibrated clock. This may be a useful selection in some cases.

9.1.3.2 XT Calibration Process

The XT Oscillator calibration value is determined by the following process:

1. Set the CALXT register field to 0 to insure calibration is not occurring.
2. Select the XT oscillator by setting the REG_CLKGEN_OCTRL_OSEL bit to 0.
3. Select the XT or a division of it on a CLKOUT pad.
4. Measure the frequency Fmeas at the CLKOUT pad.
5. Compute the adjustment value required in ppm as ((Fnom – Fmeas)*1000000)/Fmeas = PAdj
6. Compute the adjustment value in steps as PAdj/(1000000/2^{19}) = PAdj/(0.9535) = Adj
7. Compare Adj value with min/max range of -976 to 975
8. If target Adj is within min and max, set CALXT = Adj
9. Otherwise, the XT frequency is too low to be calibrated.

9.1.3.3 XT Oscillator Failure Detection

If the 32 kHz XT Oscillator generates clocks at less than 8 kHz for a period of more than 32 ms, the Apollo2 Blue detects an Oscillator Failure. The OF flag is set when an Oscillator Failure occurs, and is also set when the Apollo2 Blue initially powers up. If the OFIE bit is set, the OF flag will generate an interrupt. The current status of the XT Oscillator can be read in the REG_CLKGEN_STATUS_OSCF bit, which will be a 1 if the XT Oscillator is not running at least 8 kHz. Note that OSCF will always be set if the LFRC Oscillator is currently selected by the REG_CLKGEN_OCTRL_OSEL bit.

If the FOS bit is set and the Apollo2 Blue RTC is currently using the XT Oscillator, it will automatically switch to the LFRC Oscillator on an Oscillator Failure. This guarantees that the RTC clock will not stop in any case. If the XT Oscillator experiences a temporary failure and subsequently restarts, the Apollo2 Blue will switch back to the XT Oscillator. The REG_CLKGEN_STATUS_OMODE bit indicates the currently selected oscillator, which may not match the oscillator requested by the REG_CLKGEN_OCTRL_OSEL bit if the XT Oscillator is not running.

©2017 Ambiq Micro, Inc.
All rights reserved.

9.1.4 High Frequency RC Oscillator (HFRC)

The high frequency HFRC Oscillator, with a nominal frequency of 48 MHz, is used to supply all high frequency clocks in the Apollo2 Blue such as the processor clock for the ARM core, memories and many peripheral modules. Digital calibration is not supported for the HFRC, but its frequency may be automatically adjusted by the Autoadjustment function which is a combination of analog and digital operations.

The HFRC is enabled only when it is required by an internal module. When the ARM core goes into a sleep mode, the HFRC will be disabled unless another module is using it. If the ARM core goes into deep sleep mode, the HFRC will be powered down when it is not needed. When the HFRC is powered up, it will take a few microseconds for it to begin oscillating, and a few more microseconds before the output is completely stable. In order to prevent erroneous internal clocks from occurring, the internal clocks are gated until the HFRC is stable.

9.1.5 HFRC Autoadjustment

In some applications it is important that the HFRC frequency be more accurate than the ±2% variation typically seen, particularly in cases where the temperature may vary widely. A good example of this is in cases where the Apollo2 Blue communicates with another device via the UART. The frequency matching with the other device in the connection is an important factor in the reliability of the connection. In order to support a highly accurate HFRC, a function called Autoadjustment is provided.

It should be noted that Autoadjustment is dependent on an accurate clock source such as the crystal. The min/max variation of the HFRC frequency with and without adjustment is different. See Section 18.5 on page 496.

During Autoadjustment, the number of HFRC cycles which occur in one 32.768 kHz XT Oscillator cycle is compared to a target value. If the count is different from the target, an HFRC tuning value is modified to change the HFRC frequency. The target count is held in the REG_CLKGEN_HFADJ_HFXTADJ field. If the target HFRC frequency is 48 MHz, the optimal HFXTADJ value is 48,000/32.768 or 1464. A different value will result in a different nominal HFRC frequency.

Autoadjustment works by periodically enabling the HFRC and the XT, counting the HFRC cycles in a single XT cycle, subtracting that value from HFXTADJ and adding the resulting difference to the actual HFRC tuning value. The current tuning value may be read back in the HFTUNERB field of the REG_CLKGEN_HFVAL Register. Autoadjustment is enabled in the REG_CLKGEN_HFADJ Register by loading the repeat frequency value into the HFADJCK field and then setting the HFADJEN bit.

Autoadjustment cycles will occur continuously if both the XT and the HFRC are currently requested by other modules. If either oscillator is disabled, Autoadjustment cycles will then occur at intervals determined by the REG_CLKGEN_HFADJ_HFADJCK field, as shown in the register description. Shorter repeat intervals will result in more accurate HFRC frequencies, especially if the temperature is changing rapidly, but will result in higher power consumption. When an Autoadjustment cycle occurs, if the XT was disabled it is enabled and then a delay occurs to allow the XT to stabilize. This delay is defined by the REG_CLKGEN_HFADJ_HFWARMUP field as defined in the Register document. Once the HFRC is stable, the HFRC is enabled and several Auto-adjustments occur, each of which results in a refinement of the tuning value. Once those adjustments are complete, the HFRC and XT are powered down unless they are in use by other functions.

9.1.6 Frequency Measurement

The Autocalibration logic may be used to measure the frequency of an internal clock signal relative to the XT Oscillator frequency. The following steps are required to perform this measurement:

1. Set the REG_CLKGEN_OCTRL_ACAL field to 000.

©2017 Ambiq Micro, Inc.
All rights reserved.

2. Clear the ACC interrupt flag.
3. Select the clock to be measured with the CKSEL REG_CLKGEN_CLKOUT_CKSEL field.
4. Set ACAL to 110.
5. Wait for the ACC interrupt flag to be set.
6. Read the REG_CLKGEN_ACALCTR_ACALCTR field. This will contain the number of reference clocks which occurred during one cycle of the XT Oscillator.
7. Calculate the frequency of the measured clock.

The measured frequency is:

$F_{MEAS} = F_{REF} \div ACALCTR$

where F_{REF} is the frequency of the reference clock and ACALCTR is the value read from ACALCTR when the measurement is complete. Note that the longer the measurement period is, the more time the measurement takes, but the resulting F_{MEAS} will be more accurate.

9.1.7 Generating 100 Hz

The Real Time Clock (RTC) module requires a 100 Hz clock which is provided by the Clock Generator. This clock may come either from the LFRC or the XT Oscillators, as determined by the REG_CLKGEN_OCTRL_OSEL bit. Since 100 Hz is not a simple power of two division of either of these oscillators, special functions are used to create it.

If the XT Oscillator is selected, 100 Hz is generated by dividing the 2048 Hz division of the XT by 21 for 12 iterations and by 20 for 13 iterations out of every 25 clock periods. This produces an effective division of:

(21 * 12 + 20 * 13)/25 = 20.48

producing an exact average frequency of 100 Hz with a maximum jitter of less than 1 ms.

If the LFRC Oscillator is selected, 100 Hz is generated by dividing the 256 Hz division of the LFRC by 2 for 11 iterations and by 3 for 14 iterations out of every 25 clock periods. This produces an effective division of:

(2 * 11 + 3 * 14)/25 = 2.56

producing an exact average frequency of 100 Hz with a maximum jitter of less than 8 ms.

9.2 CLKGEN Registers

Clock Generator

INSTANCE 0 BASE ADDRESS:0x40004000

©2017 Ambiq Micro, Inc.
All rights reserved.

9.2.1 Register Memory Map

Table 499: CLKGEN Register Map

Address(s)	Register Name	Description
0x40004000	CALXT	XT Oscillator Control
0x40004004	CALRC	RC Oscillator Control
0x40004008	ACALCTR	Autocalibration Counter
0x4000400C	OCTRL	Oscillator Control
0x40004010	CLKOUT	CLKOUT Frequency Select
0x40004018	CCTRL	HFRC Clock Control
0x4000401C	STATUS	Clock Generator Status
0x40004020	HFADJ	HFRC Adjustment
0x40004024	HFVAL	HFADJ readback
0x40004028	CLOCKEN	Clock Enable Status
0x4000402C	CLOCKEN2	Clock Enable Status
0x40004030	CLOCKEN3	Clock Enable Status
0x40004034	UARTEN	UART Enable
0x40004100	INTEN	CLKGEN Interrupt Register: Enable
0x40004104	INTSTAT	CLKGEN Interrupt Register: Status
0x40004108	INTCLR	CLKGEN Interrupt Register: Clear
0x4000410C	INTSET	CLKGEN Interrupt Register: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

9.2.2 CLKGEN Registers

9.2.2.1 CALXT Register

XT Oscillator Control

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x40004000

XT Oscillator Control

Table 500: CALXT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					CALXT										

Table 501: CALXT Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	RESERVED
10:0	CALXT	0x0	RW	XT Oscillator calibration value

9.2.2.2 CALRC Register

RC Oscillator Control

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x40004004

RC Oscillator Control

Table 502: CALRC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD														CALRC																	

Table 503: CALRC Register Bits

Bit	Name	Reset	RW	Description
31:18	RSVD	0x0	RO	RESERVED
17:0	CALRC	0x0	RW	LFRC Oscillator calibration value

©2017 Ambiq Micro, Inc.
All rights reserved.

9.2.2.3 ACALCTR Register

Autocalibration Counter

OFFSET: 0x00000008

INSTANCE 0 ADDRESS: 0x40004008

Autocalibration Counter

Table 504: ACALCTR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD								ACALCTR																							

Table 505: ACALCTR Register Bits

Bit	Name	Reset	RW	Description
31:24	RSVD	0x0	RO	RESERVED
23:0	ACALCTR	0x0	RO	Autocalibration Counter result.

9.2.2.4 OCTRL Register

Oscillator Control

OFFSET: 0x0000000C

INSTANCE 0 ADDRESS: 0x4000400C

Oscillator Control

Table 506: OCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					ACAL			OSEL	FOS	RSVD				STOPRC	STOPXT

Table 507: OCTRL Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 507: OCTRL Register Bits

Bit	Name	Reset	RW	Description
10:8	ACAL	0x0	RW	Autocalibration control DIS = 0x0 - Disable Autocalibration 1024SEC = 0x2 - Autocalibrate every 1024 seconds 512SEC = 0x3 - Autocalibrate every 512 seconds XTFREQ = 0x6 - Frequency measurement using XT
7	OSEL	0x0	RW	Selects the RTC oscillator (1 => LFRC, 0 => XT) RTC_XT = 0x0 - RTC uses the XT RTC_LFRC = 0x1 - RTC uses the LFRC
6	FOS	0x0	RW	Oscillator switch on failure function DIS = 0x0 - Disable the oscillator switch on failure function EN = 0x1 - Enable the oscillator switch on failure function
5:2	RSVD	0x0	RO	RESERVED
1	STOPRC	0x0	RW	Stop the LFRC Oscillator to the RTC EN = 0x0 - Enable the LFRC Oscillator to drive the RTC STOP = 0x1 - Stop the LFRC Oscillator when driving the RTC
0	STOPXT	0x0	RW	Stop the XT Oscillator to the RTC EN = 0x0 - Enable the XT Oscillator to drive the RTC STOP = 0x1 - Stop the XT Oscillator when driving the RTC

9.2.2.5 CLKOUT Register

CLKOUT Frequency Select

OFFSET: 0x00000010

INSTANCE 0 ADDRESS: 0x40004010

CLKOUT Frequency Select

Table 508: CLKOUT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								CKEN	RSVD	CKSEL					

Table 509: CLKOUT Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 509: CLKOUT Register Bits

Bit	Name	Reset	RW	Description
7	CKEN	0x0	RW	Enable the CLKOUT signal DIS = 0x0 - Disable CLKOUT EN = 0x1 - Enable CLKOUT
6	RSVD	0x0	RO	RESERVED
5:0	CKSEL	0x0	RW	CLKOUT signal select. Note that HIGH_DRIVE should be selected if any high frequencies (such as from HFRC) are selected for CLKOUT. LFRC = 0x0 - LFRC XT_DIV2 = 0x1 - XT / 2 XT_DIV4 = 0x2 - XT / 4 XT_DIV8 = 0x3 - XT / 8 XT_DIV16 = 0x4 - XT / 16 XT_DIV32 = 0x5 - XT / 32 RTC_1Hz = 0x10 - 1 Hz as selected in RTC XT_DIV2M = 0x16 - XT / 2^21 XT = 0x17 - XT CG_100Hz = 0x18 - 100 Hz as selected in CLKGEN RSV = 0x19-0x22 - Reserved for future use LFRC_DIV2 = 0x23 - LFRC / 2 LFRC_DIV32 = 0x24 - LFRC / 32 LFRC_DIV512 = 0x25 - LFRC / 512 LFRC_DIV32K = 0x26 - LFRC / 32768 XT_DIV256 = 0x27 - XT / 256 XT_DIV8K = 0x28 - XT / 8192 XT_DIV64K = 0x29 - XT / 2^16 ULFRC_DIV16 = 0x2A - Uncal LFRC / 16 ULFRC_DIV128 = 0x2B - Uncal LFRC / 128 ULFRC_1Hz = 0x2C - Uncal LFRC / 1024 ULFRC_DIV4K = 0x2D - Uncal LFRC / 4096 ULFRC_DIV1M = 0x2E - Uncal LFRC / 2^20 RSV - 0x2F-0x30 - Reserved for future use LFRC_DIV2M = 0x31 - LFRC / 2^20 RSV - 0x32-0x33 - Reserved for future use XTNE = 0x35 - XT (not autoenabled) XTNE_DIV16 = 0x36 - XT / 16 (not autoenabled) LFRCNE_DIV32 = 0x37 - LFRC / 32 (not autoenabled) LFRCNE = 0x39 - LFRC (not autoenabled) - Default for undefined values

9.2.2.6 CCTRL Register

HFRC Clock Control

OFFSET: 0x00000018

INSTANCE 0 ADDRESS: 0x40004018

HFRC Clock Control

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 510: CCTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															CORESEL

Table 511: CCTRL Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED
0	CORESEL	0x1	RW	Core Clock divisor HFRC = 0x0 - Core Clock is HFRC HFRC_DIV2 = 0x1 - Core Clock is HFRC / 2 NOTE: HFRC_DIV2 is not supported. CORESEL must be set to HFRC (0x0) during device initialization for proper operation of MCU and modules.

9.2.2.7 STATUS Register

Clock Generator Status

OFFSET: 0x0000001C

INSTANCE 0 ADDRESS: 0x4000401C

Clock Generator Status

Table 512: STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														OSCF	OMODE

Table 513: STATUS Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	RESERVED
1	OSCF	0x0	RO	XT Oscillator is enabled but not oscillating

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 513: STATUS Register Bits

Bit	Name	Reset	RW	Description
0	OMODE	0x0	RO	Current RTC oscillator (1 => LFRC, 0 => XT)

9.2.2.8 HFADJ Register

HFRC Adjustment

OFFSET: 0x00000020

INSTANCE 0 ADDRESS: 0x40004020

HFRC Adjustment

Table 514: HFADJ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD								HFADJ_GAIN			HFWARMUP	HFXTADJ												RSVD				HFADJCK			HFADJEN

Table 515: HFADJ Register Bits

Bit	Name	Reset	RW	Description
31:24	RSVD	0x0	RO	RESERVED
23:21	HFADJ_GAIN	0x1	RW	Gain control for HFRC adjustment Gain_of_1 = 0x0 - HF Adjust with Gain of 1 Gain_of_1_in_2 = 0x1 - HF Adjust with Gain of 0.5 Gain_of_1_in_4 = 0x2 - HF Adjust with Gain of 0.25 Gain_of_1_in_8 = 0x3 - HF Adjust with Gain of 0.125 Gain_of_1_in_16 = 0x4 - HF Adjust with Gain of 0.0625 Gain_of_1_in_32 = 0x5 - HF Adjust with Gain of 0.03125
20	HFWARMUP	0x0	RW	XT warmup period for HFRC adjustment 1SEC = 0x0 - Autoadjust XT warmup period = 1-2 seconds 2SEC = 0x1 - Autoadjust XT warmup period = 2-4 seconds
19:8	HFXTADJ	0x5b8	RW	Target HFRC adjustment value.
7:4	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 515: HFADJ Register Bits

Bit	Name	Reset	RW	Description
3:1	HFADJCK	0x0	RW	Repeat period for HFRC adjustment 4SEC = 0x0 - Autoadjust repeat period = 4 seconds 16SEC = 0x1 - Autoadjust repeat period = 16 seconds 32SEC = 0x2 - Autoadjust repeat period = 32 seconds 64SEC = 0x3 - Autoadjust repeat period = 64 seconds 128SEC = 0x4 - Autoadjust repeat period = 128 seconds 256SEC = 0x5 - Autoadjust repeat period = 256 seconds 512SEC = 0x6 - Autoadjust repeat period = 512 seconds 1024SEC = 0x7 - Autoadjust repeat period = 1024 seconds
0	HFADJEN	0x0	RW	HFRC adjustment control DIS = 0x0 - Disable the HFRC adjustment EN = 0x1 - Enable the HFRC adjustment

9.2.2.9 HFVAL Register

HFADJ readback

OFFSET: 0x00000024

INSTANCE 0 ADDRESS: 0x40004024

HFADJ readback

Table 516: HFVAL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					HFTUNERB										

Table 517: HFVAL Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	RESERVED
10:0	HFTUNERB	0x0	RO	Current HFTUNE value

9.2.2.10 CLOCKEN Register

Clock Enable Status

OFFSET: 0x00000028

INSTANCE 0 ADDRESS: 0x40004028

Clock Enable Status

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 518: CLOCKEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CLOCKEN																															

Table 519: CLOCKEN Register Bits

Bit	Name	Reset	RW	Description
31:0	CLOCKEN	0x0	RO	Clock enable status ADC_CLKEN = 0x1 - Clock enable for the ADC. CTIMER_CLKEN = 0x2 - Clock enable for the CTIMER. CTIMER0A_CLKEN = 0x4 - Clock enable for the CTIMER0A. CTIMER0B_CLKEN = 0x8 - Clock enable for the CTIMER0B. CTIMER1A_CLKEN = 0x10 - Clock enable for the CTIMER1A. CTIMER1B_CLKEN = 0x20 - Clock enable for the CTIMER1B. CTIMER2A_CLKEN = 0x40 - Clock enable for the CTIMER2A. CTIMER2B_CLKEN = 0x80 - Clock enable for the CTIMER2B. CTIMER3A_CLKEN = 0x100 - Clock enable for the CTIMER3A. CTIMER3B_CLKEN = 0x200 - Clock enable for the CTIMER3B. IOMSTR0_CLKEN = 0x400 - Clock enable for the IO Master 0. IOMSTR1_CLKEN = 0x800 - Clock enable for the IO Master 1. IOMSTR2_CLKEN = 0x1000 - Clock enable for the IO Master 2. IOMSTR3_CLKEN = 0x2000 - Clock enable for the IO Master 3. IOMSTR4_CLKEN = 0x4000 - Clock enable for the IO Master 4. IOMSTR5_CLKEN = 0x8000 - Clock enable for the IO Master 5. IOMSTRIFC0_CLKEN = 0x10000 - Clock enable for the IO Master IFC0. IOMSTRIFC1_CLKEN = 0x20000 - Clock enable for the IO Master IFC1. IOMSTRIFC2_CLKEN = 0x40000 - Clock enable for the IO Master IFC2. IOMSTRIFC3_CLKEN = 0x80000 - Clock enable for the IO Master IFC3. IOMSTRIFC4_CLKEN = 0x100000 - Clock enable for the IO Master IFC4. IOMSTRIFC5_CLKEN = 0x200000 - Clock enable for the IO Master IFC5. IOSLAVE_CLKEN = 0x400000 - Clock enable for the IO Slave. PDM_CLKEN = 0x800000 - Clock enable for the PDM. PDMIFC_CLKEN = 0x1000000 - Clock enable for the PDM IFC. RSTGEN_CLKEN = 0x2000000 - Clock enable for the RSTGEN. SRAM_WIPE_CLKEN = 0x4000000 - Clock enable for the SRAM_WIPE. STIMER_CLKEN = 0x8000000 - Clock enable for the STIMER. STIMER_CNT_CLKEN = 0x10000000 - Clock enable for the STIMER_CNT. TPIU_CLKEN = 0x20000000 - Clock enable for the TPIU. UART0_HCLK_CLKEN = 0x40000000 - Clock enable for the UART0_HCLK. UART0HF_CLKEN = 0x80000000 - Clock enable for the UART0HF.

9.2.2.11 CLOCKEN2 Register

Clock Enable Status

OFFSET: 0x0000002C

INSTANCE 0 ADDRESS: 0x4000402C

Clock Enable Status

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 520: CLOCKEN2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CLOCKEN2																															

Table 521: CLOCKEN2 Register Bits

Bit	Name	Reset	RW	Description
31:0	CLOCKEN2	0x0	RO	Clock enable status 2 UART1_HCLK_CLKEN = 0x1 - Clock enable for the UART1_HCLK. UART1HF_CLKEN = 0x2 - Clock enable for the UART1HF. WDT_CLKEN = 0x4 - Clock enable for the WDT. XT_32KHz_EN = 0x40000000 - Clock enable for the XT_32KHz. FRCHFRC = 0x80000000 - Force HFRC On Status

9.2.2.12 CLOCKEN3 Register

Clock Enable Status

OFFSET: 0x00000030

INSTANCE 0 ADDRESS: 0x40004030

Clock Enable Status

Table 522: CLOCKEN3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CLOCKEN3																															

Table 523: CLOCKEN3 Register Bits

Bit	Name	Reset	RW	Description
31:0	CLOCKEN3	0x0	RO	Clock enable status 3 periph_all_xtal_en = 0x1000000 - At least 1 peripherial is requesting for XTAL Clock periph_all_hfrc_en = 0x2000000 - At least 1 peripherial is requesting for HFRC Clock HFADJEN = 0x4000000 - HFRC Adjust Enable Status HFRC_en_out = 0x8000000 - HFRC is enabled during adjustment status RTC_SOURCE = 0x10000000 - Selects the RTC oscillator (0 => LFRC, 1 => XT) XTAL_EN = 0x20000000 - XT is enabled Status HFRC_EN = 0x40000000 - HFRC is enabled Status FLASHCLK_EN = 0x80000000 - Flash Clock is enabled Status

©2017 Ambiq Micro, Inc.
All rights reserved.

9.2.2.13 UARTEN Register

UART Enable

OFFSET: 0x00000034

INSTANCE 0 ADDRESS: 0x40004034

UART Enable

Table 524: UARTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																						UART1EN		RSVD						UART0EN	

Table 525: UARTEN Register Bits

Bit	Name	Reset	RW	Description
31:10	RSVD	0x0	RO	RESERVED
9:8	UART1EN	0x0	RW	UART1 system clock control DIS = 0x0 - Disable the UART1 system clock EN = 0x1 - Enable the UART1 system clock REDUCE_FREQ = 0x2 - Run UART_Hclk at the same frequency as UART_hfclk EN_POWER_SAV = 0x3 - Enable UART_hclk to reduce to UART_hfclk at low power mode
7:2	RSVD	0x0	RO	RESERVED
1:0	UART0EN	0x0	RW	UART0 system clock control DIS = 0x0 - Disable the UART0 system clock EN = 0x1 - Enable the UART0 system clock REDUCE_FREQ = 0x2 - Run UART_Hclk at the same frequency as UART_hfclk EN_POWER_SAV = 0x3 - Enable UART_hclk to reduce to UART_hfclk at low power mode

9.2.2.14 INTEN Register

CLKGEN Interrupt Register: Enable

OFFSET: 0x00000100

INSTANCE 0 ADDRESS: 0x40004100

Set bits in this register to allow this module to generate the corresponding interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 526: INTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												ALM	OF	ACC	ACF

Table 527: INTEN Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED
3	ALM	0x0	RW	RTC Alarm interrupt
2	OF	0x0	RW	XT Oscillator Fail interrupt
1	ACC	0x0	RW	Autocalibration Complete interrupt
0	ACF	0x0	RW	Autocalibration Fail interrupt

9.2.2.15 INTSTAT Register

CLKGEN Interrupt Register: Status

OFFSET: 0x00000104

INSTANCE 0 ADDRESS: 0x40004104

Read bits from this register to discover the cause of a recent interrupt.

Table 528: INTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												ALM	OF	ACC	ACF

Table 529: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED
3	ALM	0x0	RW	RTC Alarm interrupt

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 529: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
2	OF	0x0	RW	XT Oscillator Fail interrupt
1	ACC	0x0	RW	Autocalibration Complete interrupt
0	ACF	0x0	RW	Autocalibration Fail interrupt

9.2.2.16 INTCLR Register

CLKGEN Interrupt Register: Clear

OFFSET: 0x00000108

INSTANCE 0 ADDRESS: 0x40004108

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 530: INTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												ALM	OF	ACC	ACF

Table 531: INTCLR Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED
3	ALM	0x0	RW	RTC Alarm interrupt
2	OF	0x0	RW	XT Oscillator Fail interrupt
1	ACC	0x0	RW	Autocalibration Complete interrupt
0	ACF	0x0	RW	Autocalibration Fail interrupt

9.2.2.17 INTSET Register

CLKGEN Interrupt Register: Set

OFFSET: 0x0000010C

INSTANCE 0 ADDRESS: 0x4000410C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 532: INTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												ALM	OF	ACC	ACF

Table 533: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED
3	ALM	0x0	RW	RTC Alarm interrupt
2	OF	0x0	RW	XT Oscillator Fail interrupt
1	ACC	0x0	RW	Autocalibration Complete interrupt
0	ACF	0x0	RW	Autocalibration Fail interrupt

©2017 Ambiq Micro, Inc.
All rights reserved.

9.3 Real Time Clock

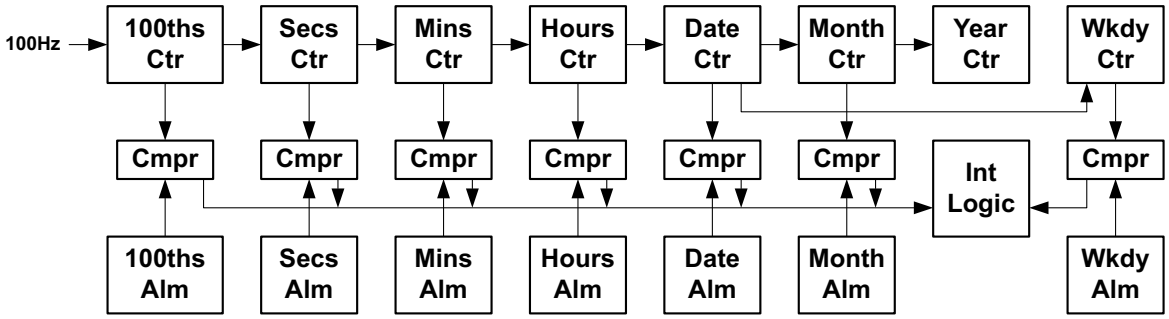


Figure 56. Block diagram for the Real Time Clock Module

9.3.1 RTC Functional Overview

The Real Time Clock (RTC) Module, shown in Figure 56, provides an accurate real time measurement. Key features are:

- 100^{th} of a second resolution
- Time is measured for the years between 1900 and 2199
- Automatic leap year calculation
- Hours may be specified in 12 or 24 hour mode
- Alarm precise to 1/100 second
- Alarm interval every 100^{th} second, 10^{th} second, second, minute, hour, day, week, month or year.
- 100 Hz input clock taken from either the high accuracy XT Oscillator or the low power LFRC Oscillator.

9.3.2 Calendar Counters

The real time is held in a set of eight Calendar Counters, which hold the current $1/100^{th}$ of a second (REG_CLK_GEN_CTRLOW_CTR100), the current second (REG_CLK_GEN_CTRLOW_CTRSEC), the minute (REG_CLK_GEN_CTRLOW_CTRMIN), the hour (REG_CLK_GEN_CTRLOW_CTRHR), the current day of the month (REG_CLK_GEN_CTRUP_CTRDATE), the current day of the week (REG_CLK_GEN_CTRUP_CTRWKDY), the current month (REG_CLK_GEN_CTRUP_CTRMO), the current year (REG_CLK_GEN_CTRUP_CTRYR) and the current century (REG_CLK_GEN_CTRUP_CB), all in BCD format. In order to insure that the RTC starts precisely, the timer chain which generates the 100 Hz clock is reset to 0 whenever any of the Calendar Counter Registers is written. Since unintentional modification of the Calendar Counters is a serious problem, the REG_CLK_GEN_RTCCTL_WRTC bit must be set in order to write any of the counters, and should be reset by software after any load of the Calendar Counters.

Software may stop the clock to the Calendar Counters by setting the REG_CLK_GEN_RTCCTL_RSTOP bit. This may be used in modes like Stopwatch to precisely start and stop the Calendar Counters.

9.3.3 Calendar Counter Reads

The RTC includes special logic to help insure that the Calendar Counters may be read reliably, i.e. that no rollover has occurred. Because two 32-bit reads are required to read the complete set of counters, it is possible that a delay occurs between the two reads which causes a rollover to occur. An interrupt is the most likely reason this could occur. If two 100 Hz clocks occur between these two reads, the REG_CLK_GEN_CTRUP_CTRERR bit will be set. Software should check this bit after any Calendar Counter read, and perform the read again if it is set. Any read of the upper counter word will clear the CTRERR bit.

©2017 Ambiq Micro, Inc.
All rights reserved.

9.3.4 Alarms

There are seven Alarm Registers which may be used to generate an Alarm interrupt at a specific time. These registers correspond to the 100th of a second (REG_CLK_GEN_ALMLOW_ALM100), second (REG_CLK_GEN_ALMLOW_ALMSEC), minute (REG_CLK_GEN_ALMLOW_ALMMIN), hour (REG_CLK_GEN_ALMLOW_ALMHR), day of the month (REG_CLK_GEN_ALMUP_ALMDATE), day of the week (REG_CLK_GEN_ALMUP_ALMWKDY) and month (REG_CLK_GEN_ALMUP_ALMMO) Calendar Counters. The comparison is controlled by the REG_CLK_GEN_RTCCTL_RPT field and the REG_CLK_GEN_ALMLOW_ALM100 Register as shown in 12/24 Hour Mode. In the ALM100 Register, n indicates any digit 0-9. When all selected Counters match their corresponding Alarm Register, the ALM interrupt flag is set (see the Clock Generator section for the ALM interrupt control).

Table 534: Alarm RPT Function

RPT Value	Interval	Comparison
000	Disabled	None
001	Every year	100th, second, minute, hour, day, month
010	Every month	100th, second, minute, hour, day
011	Every week	100th, second, minute, hour, weekday
100	Every day	100th, second, minute, hour
101	Every hour	100th, second, minute
110	Every minute	100th, second
111	Every second	100th

All alarm interrupts are asserted on the next 100 Hz clock cycle after the counters match the alarm register, except for 100ths of a second. To get an interrupt that occurs precisely at a certain time, the comparison value in the corresponding alarm register should be set 10 ms (one 100 Hz count) earlier than the desired interrupt time.

For the 100ths of a second interrupt, the first 100 Hz clock sets the comparison with the alarm register and the next clock asserts the interrupt. Therefore, the first 100ths interrupt will be asserted after 20 ms, not 10 ms. This occurs each and every time the 100ths of a second counter with interrupts is enabled if the RTC is stopped. If the RTC is already running when configured, then the first interrupt will occur between 10 and 20 ms after configuration.

9.3.5 12/24 Hour Mode

If the REG_CLK_GEN_RTCCTL_HR1224 bit is 0, the RTC is in 24-hour mode, and the Hours and Hours Alarm Registers hold a 6-bit BCD value which is the 24-hour time (values 0 to 23). If the HR1224 bit is 1, the RTC is in 12-hour mode, and the Hours and Hours Alarm Registers hold a 5-bit BCD value which is the 12-hour time (values 1 to 12) , and bit 5 is the AP bit which is 0 for an AM time and 1 for a PM time. If the HR1224 bit is modified the Hours and Hours Alarm fields must be updated.

9.3.6 Century Control and Leap Year Management

The REG_CLK_GEN_CTRUP_CB bit indicates the current century. A value of 0 indicates the 20th century, and a value of 1 indicates the 19th or 21st century. The CB value will toggle when the Years counter rolls over from 99 to 0 if the REG_CLK_GEN_CTRUP_CEB bit is set, and will remain constant if CEB is clear. The century value is used to control the Leap Year functions, which create the correct insertion of February 29 in years which are divisible by 4 and not divisible by 100, and also the year 2000.

©2017 Ambiq Micro, Inc.
All rights reserved.

9.3.7 Weekday Function

The Weekday Counter is simply a 3-bit counter which counts up to 6 and then resets to 0. It is the responsibility of software to assign particular days of the week to each counter value.

9.4 RTC Registers

Table 535: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED
3	ALM	0x0	RW	RTC Alarm interrupt
2	OF	0x0	RW	XT Oscillator Fail interrupt
1	ACC	0x0	RW	Autocalibration Complete interrupt
0	ACF	0x0	RW	Autocalibration Fail interrupt

Real Time Clock

INSTANCE 0 BASE ADDRESS:0x40004000

9.4.1 Register Memory Map

Table 536: RTC Register Map

Address(s)	Register Name	Description
0x40004040	CTRLOW	RTC Counters Lower
0x40004044	CTRUP	RTC Counters Upper
0x40004048	ALMLOW	RTC Alarms Lower
0x4000404C	ALMUP	RTC Alarms Upper
0x40004050	RTCCTL	RTC Control Register
0x40004100	INTEN	RTC Interrupt Register: Enable
0x40004104	INTSTAT	RTC Interrupt Register: Status
0x40004108	INTCLR	RTC Interrupt Register: Clear
0x4000410C	INTSET	RTC Interrupt Register: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

9.4.2 RTC Registers

9.4.2.1 CTRLOW Register

RTC Counters Lower

OFFSET: 0x00000040

INSTANCE 0 ADDRESS: 0x40004040

RTC Counters Lower

Table 537: CTRLOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		CTRHR						RSVD		CTRMIN						RSVD		CTRSEC						CTR100							

Table 538: CTRLOW Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:24	CTRHR	0x1	RW	Hours Counter
23	RSVD	0x0	RO	RESERVED
22:16	CTRMIN	0x0	RW	Minutes Counter
15	RSVD	0x0	RO	RESERVED
14:8	CTRSEC	0x0	RW	Seconds Counter
7:0	CTR100	0x0	RW	100ths of a second Counter

9.4.2.2 CTRUP Register

RTC Counters Upper

OFFSET: 0x00000044

INSTANCE 0 ADDRESS: 0x40004044

RTC Counters Upper

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 539: CTRUP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTERR	RSVD		CEB	CB	CTRWKDY			CTRYR								RSVD			CTRMO					RSVD		CTRDATE					

Table 540: CTRUP Register Bits

Bit	Name	Reset	RW	Description
31	CTERR	0x0	RO	Counter read error status NOERR = 0x0 - No read error occurred RDERR = 0x1 - Read error occurred
30:29	RSVD	0x0	RO	RESERVED
28	CEB	0x0	RW	Century enable DIS = 0x0 - Disable the Century bit from changing EN = 0x1 - Enable the Century bit to change
27	CB	0x0	RW	Century 2000 = 0x0 - Century is 2000s 1900_2100 = 0x1 - Century is 1900s/2100s
26:24	CTRWKDY	0x0	RW	Weekdays Counter
23:16	CTRYR	0x0	RW	Years Counter
15:13	RSVD	0x0	RO	RESERVED
12:8	CTRMO	0x0	RW	Months Counter
7:6	RSVD	0x0	RO	RESERVED
5:0	CTRDATE	0x0	RW	Date Counter

9.4.2.3 ALMLOW Register

RTC Alarms Lower

OFFSET: 0x00000048

INSTANCE 0 ADDRESS: 0x40004048

RTC Alarms Lower

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 541: ALMLOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD		ALMHR						RSVD		ALMMIN						RSVD		ALMSEC						ALM100							

Table 542: ALMLOW Register Bits

Bit	Name	Reset	RW	Description
31:30	RSVD	0x0	RO	RESERVED
29:24	ALMHR	0x0	RW	Hours Alarm
23	RSVD	0x0	RO	RESERVED
22:16	ALMMIN	0x0	RW	Minutes Alarm
15	RSVD	0x0	RO	RESERVED
14:8	ALMSEC	0x0	RW	Seconds Alarm
7:0	ALM100	0x0	RW	100ths of a second Alarm

9.4.2.4 ALMUP Register

RTC Alarms Upper

OFFSET: 0x0000004C

INSTANCE 0 ADDRESS: 0x4000404C

RTC Alarms Upper

Table 543: ALMUP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD													ALMWKDY			RSVD			ALMMO					RSVD		ALMDATE					

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 544: ALMUP Register Bits

Bit	Name	Reset	RW	Description
31:19	RSVD	0x0	RO	RESERVED
18:16	ALMWKDY	0x0	RW	Weekdays Alarm
15:13	RSVD	0x0	RO	RESERVED
12:8	ALMMO	0x0	RW	Months Alarm
7:6	RSVD	0x0	RO	RESERVED
5:0	ALMDATE	0x0	RW	Date Alarm

9.4.2.5 RTCCTL Register

RTC Control Register

OFFSET: 0x00000050

INSTANCE 0 ADDRESS: 0x40004050

RTC Control Register

Table 545: RTCCTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										HR1224	RSTOP	RPT			WRTC

Table 546: RTCCTL Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED
5	HR1224	0x0	RW	Hours Counter mode 24HR = 0x0 - Hours in 24 hour mode 12HR = 0x1 - Hours in 12 hour mode
4	RSTOP	0x0	RW	RTC input clock control RUN = 0x0 - Allow the RTC input clock to run STOP = 0x1 - Stop the RTC input clock

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 546: RTCCTL Register Bits

Bit	Name	Reset	RW	Description
3:1	RPT	0x0	RW	Alarm repeat interval DIS = 0x0 - Alarm interrupt disabled YEAR = 0x1 - Interrupt every year MONTH = 0x2 - Interrupt every month WEEK = 0x3 - Interrupt every week DAY = 0x4 - Interrupt every day HR = 0x5 - Interrupt every hour MIN = 0x6 - Interrupt every minute SEC = 0x7 - Interrupt every second/10th/100th
0	WRTC	0x0	RW	Counter write control DIS = 0x0 - Counter writes are disabled EN = 0x1 - Counter writes are enabled

9.4.2.6 INTEN Register

RTC Interrupt Register: Enable

OFFSET: 0x00000100

INSTANCE 0 ADDRESS: 0x40004100

Set bits in this register to allow this module to generate the corresponding interrupt.

Table 547: INTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												ALM	OF	ACC	ACF

Table 548: INTEN Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED
3	ALM	0x0	RW	RTC Alarm interrupt
2	OF	0x0	RW	XT Oscillator Fail interrupt
1	ACC	0x0	RW	Autocalibration Complete interrupt
0	ACF	0x0	RW	Autocalibration Fail interrupt

©2017 Ambiq Micro, Inc.
All rights reserved.

9.4.2.7 INTSTAT Register

RTC Interrupt Register: Status

OFFSET: 0x00000104

INSTANCE 0 ADDRESS: 0x40004104

Read bits from this register to discover the cause of a recent interrupt.

Table 549: INTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												ALM	OF	ACC	ACF

Table 550: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED
3	ALM	0x0	RW	RTC Alarm interrupt
2	OF	0x0	RW	XT Oscillator Fail interrupt
1	ACC	0x0	RW	Autocalibration Complete interrupt
0	ACF	0x0	RW	Autocalibration Fail interrupt

9.4.2.8 INTCLR Register

RTC Interrupt Register: Clear

OFFSET: 0x00000108

INSTANCE 0 ADDRESS: 0x40004108

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 551: INTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												ALM	OF	ACC	ACF

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 552: INTCLR Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED
3	ALM	0x0	RW	RTC Alarm interrupt
2	OF	0x0	RW	XT Oscillator Fail interrupt
1	ACC	0x0	RW	Autocalibration Complete interrupt
0	ACF	0x0	RW	Autocalibration Fail interrupt

9.4.2.9 INTSET Register

RTC Interrupt Register: Set

OFFSET: 0x0000010C

INSTANCE 0 ADDRESS: 0x4000410C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 553: INTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												ALM	OF	ACC	ACF

Table 554: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED
3	ALM	0x0	RW	RTC Alarm interrupt
2	OF	0x0	RW	XT Oscillator Fail interrupt
1	ACC	0x0	RW	Autocalibration Complete interrupt
0	ACF	0x0	RW	Autocalibration Fail interrupt

©2017 Ambiq Micro, Inc.
All rights reserved.

10. Counter/Timer Module

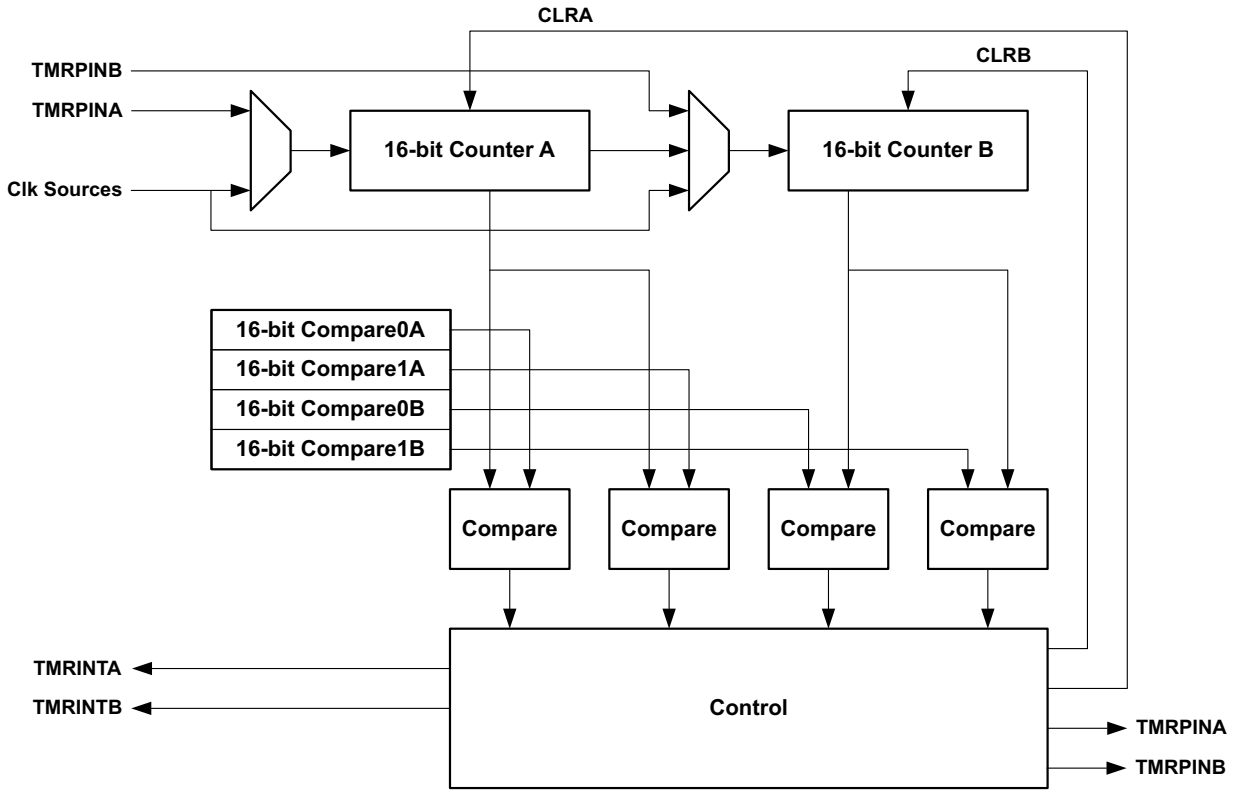


Figure 57. Block Diagram for One General Purpose Counter/Timer Pair

10.1 Functional Overview

The Apollo2 Blue Timer/Counter module includes four general purpose Timer/Counter pairs, one of which is shown in Figure 57, as well as a system timer shown in Figure 63 in the System Timer chapter. Each general purpose Timer/Counter pair includes two very low power asynchronous 16-bit counters, which may be combined to provide a 32-bit counter. Four registers contain reset values for the counters and/or comparison values to allow the generation of complex signals. Each Timer/Counter has an external pin connection, and can be configured to provide a variety of functions:

- Interrupt after a specified delay
- Interrupt periodically with a specified period
- Determine the time between events
- Generate an external pulse of a specified width, configurable after a specified delay
- Generate an external PWM signal with a specified period and duty cycle
- Count edges on an external input

10.2 Counter/Timer Functions

Each Counter/Timer operates in a mode controlled by the REG_CTIMER_CTCTRLx_TMRxyFN bit field (x=0 to 3, y=A or B). The mode affects both the generation of interrupts and the control of an external pin. Each mode is described in the following sections. Note that for all functions, a REG_CTIMER_CMPR0/1 value of zero (a count of 1) is invalid, and that the first measured period will be between the

©2017 Ambiq Micro, Inc.
All rights reserved.

REG_CTIMER_CMPR0 value plus 2 and the specified value plus 3. Subsequent repeated cycles will be correctly of length (CMPR value + 1). There are five modes:

0 => Single Count: Timer counts from 0 to CMPR0 and stops, with an optional interrupt.

1 => Repeated Count: Periodic 1-clock-cycle wide pulses with optional interrupts.

2 => Single Pulse (One Shot): Timer counts from 0 to CMPR0, generates a pin transition and an optional interrupt, continues counting from CMPR0 to CMPR1, generates another pin transition (with no interrupt), and then stops.

3 => Repeated Pulse: Same as single pulse, but the timer rolls over to 0 and restarts immediately after reaching CMPR1. Often used to generate PWM signals.

4 => Continuous: The timer repeatedly counts from 0 to 2^{16} - 1 forever, regardless of what the CMPR values are. The timer can optionally generate an interrupt or pin transition the first time it reaches CMPR0, but it won't generate an interrupt or pin transition on subsequent iterations.

10.2.1 Single Count (FN = 0)

Operation in this mode is shown in Figure 58. When the Timer is enabled, the pin output is at the level selected by the POL bit and the Timer is at zero because CLR has been asserted previously. The Timer counts up on each selected clock, and when it reaches the value in the corresponding REG_CTIMER_CMPR0 Register the output pin switches polarity (if the PE bit is set) and an interrupt is generated (if the IE bit is set). At this point the Timer resets to 0 and the output pin is maintained at the selected level until the Timer is cleared with CLR. The interrupt may be cleared by writing the corresponding WC bit in the TMRWCR Register.

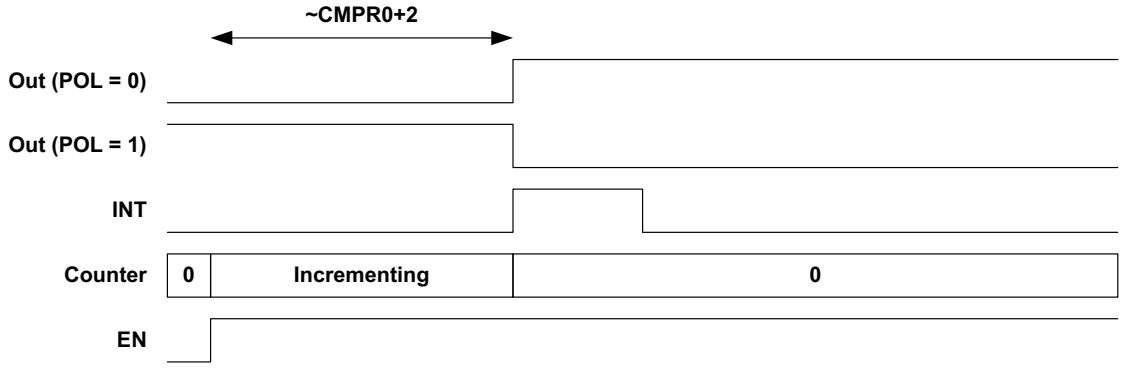


Figure 58. Counter/Timer Operation, FN = 0

10.2.2 Repeated Count (FN = 1)

Operation in this mode is shown in Figure 59. When the Timer is enabled, the pin output is at the level selected by the POL bit and the Timer is at zero because REG_CTIMER_TMRxyCLR has been asserted previously. The Timer counts up on each selected clock, and when it reaches the value in the corresponding CMPR0 Register the output pin switches polarity (if the REG_CTIMER_TMRxyPE bit is set) and an interrupt is generated (if the IE bit is set). At this point the Timer resets to 0 and the output pin is maintained at the selected level for one clock cycle, after which it returns to the original value. The Timer continues to count up and the process is repeated, creating a stream of pulses or interrupts at a fixed interval. The interrupt may be cleared by writing the corresponding WC bit in the TMRWCR Register at any point prior to the next setting pulse.

©2017 Ambiq Micro, Inc.
All rights reserved.

If the REG_CTIMER_TMRxyEN bit is cleared, the Timer will stop counting but will not be cleared, so the sequence may be paused and then resumed. Setting CLR will reset the Timer to zero. Note that CMPR0 must be at least 1 so that the repeat interval is two clock cycles.

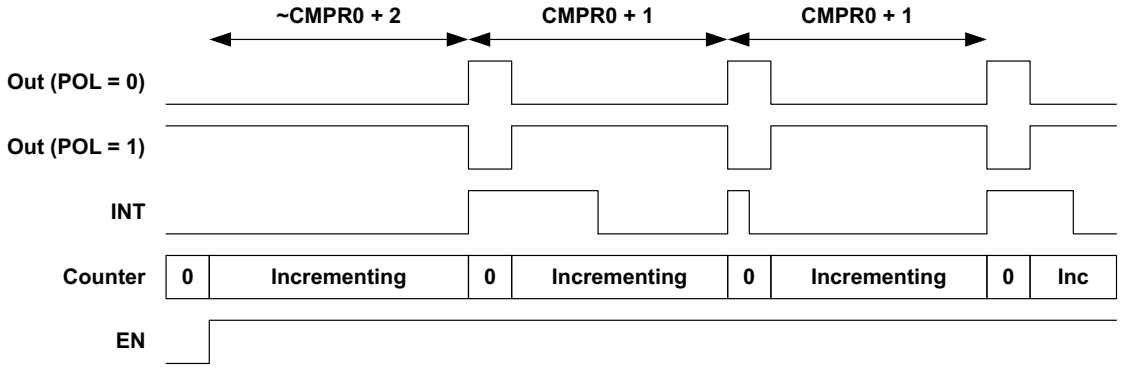


Figure 59. Counter/Timer Operation, FN = 1

10.2.3 Single Pulse (FN = 2)

Operation in this mode is shown in Figure 60. When the Timer is enabled, the pin output is at the level selected by the REG_CTIMER_TMRxyPOL bit and the Timer is at zero because CLR has been asserted previously. The Timer counts up on each selected clock, and when it reaches the value in the corresponding CMPR0 Register the output pin switches polarity (if the REG_CTIMER_TMRxyPE bit is set) and an interrupt is generated (if the REG_CTIMER_TMRxyIE bit is set). At this point the Timer continues to increment and the output pin is maintained at the selected level until the Timer reaches the value in the CMPR1 Register, at which point it switches back to the original level. This allows the creation of a pulse of a specified width. The Timer is reset to 0 so that a single pulse is created. The interrupt may be cleared by writing the corresponding WC bit in the TMRWCR Register.

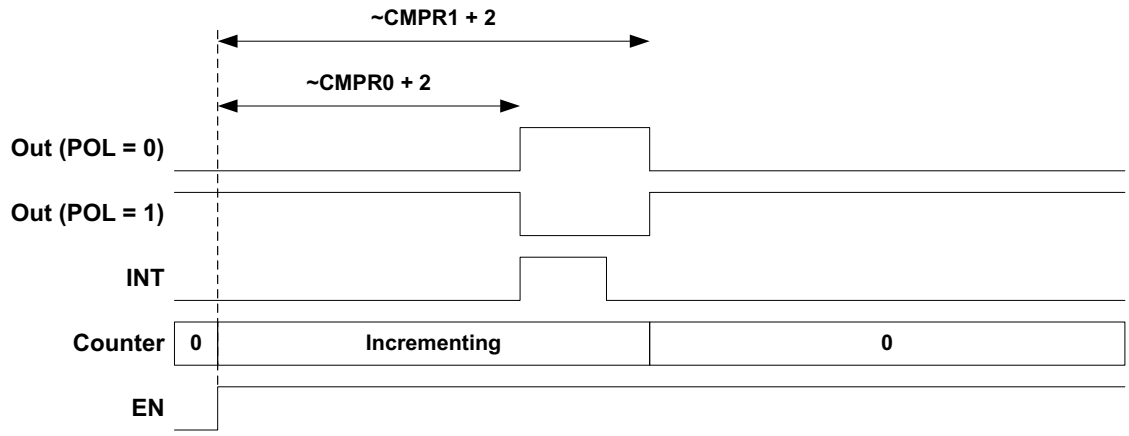


Figure 60. Counter/Timer Operation, FN = 2

10.2.4 Repeated Pulse (FN = 3)

Operation in this mode is shown in Figure 61. When the Timer is enabled, the pin output is at the level selected by the POL bit and the Timer is at zero because CLR has been asserted previously. The Timer

©2017 Ambiq Micro, Inc.
All rights reserved.

counts up on each selected clock, and when it reaches the value in the corresponding CMPR0 Register the output pin switches polarity (if the PE bit is set) and an interrupt is generated (if the IE bit is set). At this point the Timer continues to increment and the output pin is maintained at the selected level until the Timer reaches the value in the CMPR1 Register, at which point it switches back to the original level. This allows the creation of a pulse of a specified width. The interrupt may be cleared by writing the corresponding WC bit in the TMRWCR Register. Note that CMPR1 must be at least 1 so that the repeat interval is two clock cycles.

The Timer is reset to 0 and continues to increment, so that a stream of pulses of the specified width and period is generated. If the EN bit is cleared, the Timer stops counting, but is not cleared, so the sequence may be paused and restarted. This mode is particularly valuable for creating a PWM (Pulse Width Modulation) output on the pin which may be used, for example, to vary the brightness of an LED.

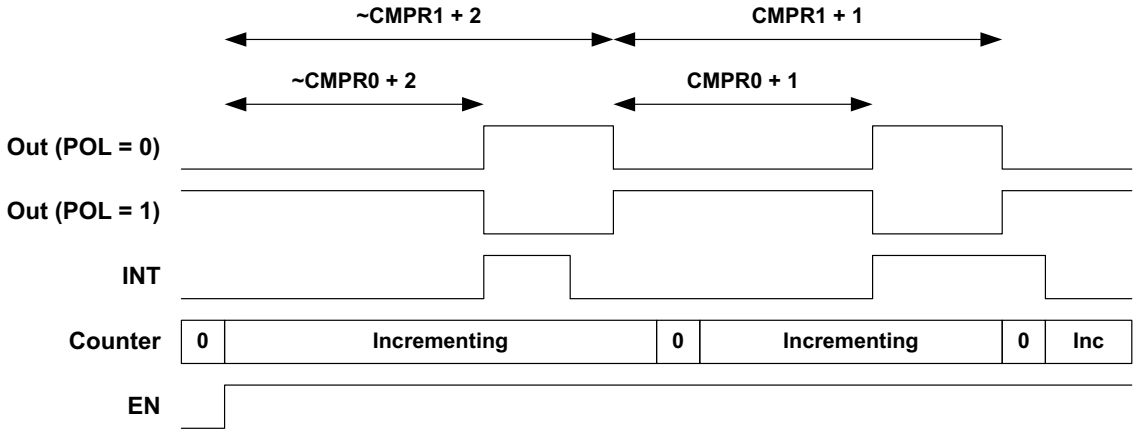


Figure 61. Counter/Timer Operation, FN = 3

10.2.5 Continuous (FN = 4)

Operation in this mode is shown in Figure 62. When the Timer is enabled, the pin output is at the level selected by the POL bit and the Timer is at zero because CLR has been asserted previously. The Timer counts up on each selected clock, and when it reaches the value in the corresponding CMPR0 Register the output pin switches polarity (if the PE bit is set) and an interrupt is generated (if the IE bit is set). The Timer continues to count and is never automatically reset. If the Timer rolls over to zero and reaches the CMPR0 value again, an interrupt will not be generated and the output pin will not change.

This mode is primarily used for two functions. The first is counting transitions on the external input pin, and it may be valuable to generate an interrupt when a specified number of transitions have been detected. The second is as a general timer which software reads in order to measure time periods. In this second case an interrupt is often not used and will not be enabled.

©2017 Ambiq Micro, Inc.
All rights reserved.

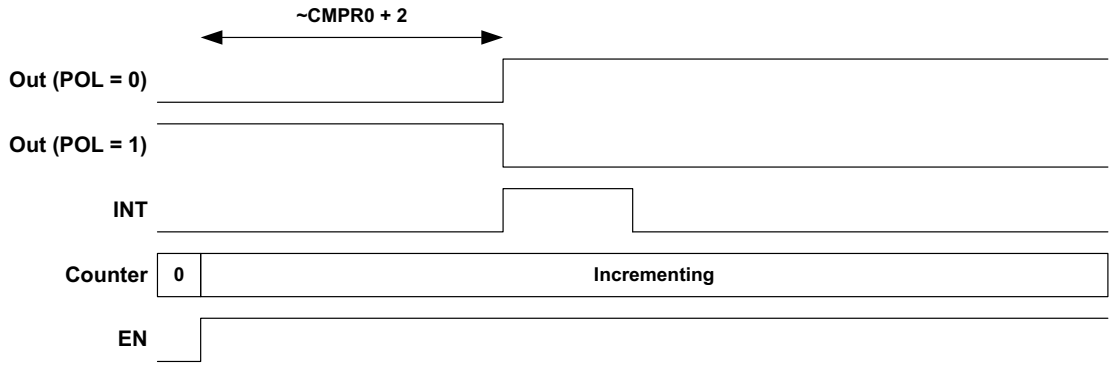


Figure 62. Counter/Timer Operation, FN = 4

10.3 Creating 32-bit Counters

Each pair (A/B) of 16-bit counters may be combined to create a 32-bit counter. This configuration is created by setting the REG_CTIMER_CTCTRLx_CTRLINKx bit for the pair. The control bits for the A counter of the pair are used to control the 32-bit counter, and the B control bits are ignored. The CMPR0 and CMPR1 registers for each 16-bit counter are concatenated to provide the 32-bit comparison values, and all timer modes are supported.

10.4 Power Optimization by Measuring HCLK

Each timer has the capability to select the processor clock HCLK as the counter clock input. This allows a very straightforward measurement of how much of the time the processor is in a Sleep or Deep Sleep mode. Two counters are configured with FN = 4 so that they count continuously. One is supplied HCLK as its clock, and the other is supplied with a divided version of the HFRC clock. The two counters are enabled simultaneously, and after some period of system operation they are disabled and read. The HFRC count value defines how much real time has elapsed and how many HCLKs could have occurred in that time, and the HCLK count value defines how many actual HCLKs were received in that time. The ratio is an accurate measurement of the percentage of time the CPU is asleep, and is an effective tool for power optimization.

10.5 Generating the Sample Rate for the ADC

Timer CTTMRA3 has a special function which allows it to be used as the sample trigger generator for the ADC. If the ADCEN and TMRA3PE bits are set, the output of the timer is sent to the ADC which uses it as a trigger. Note that, while the TMRA3PE bit must be set, the TCTA3 GPIO output for the Ctimer should not be enabled to prevent unexpected transitions on the corresponding package pin.

Typically, Ctimer3 is configured in Repeated Count (FN =1) mode. TMRA3IE may be set to generate an interrupt whenever the trigger occurs, but typically the ADC interrupt will be used for this purpose.

10.6 Measuring Buck Converter Charge Insertion

Each counter may be connected to a pulse stream from one of the two Buck Converters. One pulse is generated each time the Buck Converter delivers charge onto the capacitor, and therefore the number of pulses is a good indication of the amount of energy used by the corresponding power domain in a particular time period.

Following is a possible option to determine energy consumption. Two counters could be configured with FN = 4 so that they count continuously. One is supplied a Buck Converter pulse stream as its clock, and

©2017 Ambiq Micro, Inc.
All rights reserved.

the other is supplied with a divided version of the LFRC clock to avoid creating extra power consumption due to the power measurement. Once configured such, the two counters should be enabled simultaneously, and after some period of system operation they should be disabled and read. The LFRC count value would now define how much real time has elapsed, and the Buck Converter count value would define how much energy was consumed in that time.

10.7 CTIMER Registers

Counter/Timer

INSTANCE 0 BASE ADDRESS:0x40008000

The Counter/Timer block contains 8 sixteen bit counter or timer functions. Each pair of these counters can be cascaded into 32 bit Counter/Timer functions.

10.7.1 Register Memory Map

Table 555: CTIMER Register Map

Address(s)	Register Name	Description
0x40008000	TMR0	Counter/Timer Register
0x40008004	CMPRA0	Counter/Timer A0 Compare Registers
0x40008008	CMPRB0	Counter/Timer B0 Compare Registers
0x4000800C	CTRL0	Counter/Timer Control
0x40008010	TMR1	Counter/Timer Register
0x40008014	CMPRA1	Counter/Timer A1 Compare Registers
0x40008018	CMPRB1	Counter/Timer B1 Compare Registers
0x4000801C	CTRL1	Counter/Timer Control
0x40008020	TMR2	Counter/Timer Register
0x40008024	CMPRA2	Counter/Timer A2 Compare Registers
0x40008028	CMPRB2	Counter/Timer B2 Compare Registers
0x4000802C	CTRL2	Counter/Timer Control
0x40008030	TMR3	Counter/Timer Register
0x40008034	CMPRA3	Counter/Timer A3 Compare Registers
0x40008038	CMPRB3	Counter/Timer B3 Compare Registers
0x4000803C	CTRL3	Counter/Timer Control
0x40008200	INTEN	Counter/Timer Interrupts: Enable
0x40008204	INTSTAT	Counter/Timer Interrupts: Status
0x40008208	INTCLR	Counter/Timer Interrupts: Clear
0x4000820C	INTSET	Counter/Timer Interrupts: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

10.7.2 CTIMER Registers

10.7.2.1 TMR0 Register

Counter/Timer Register

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x40008000

This register holds the running time or event count, either for each 16 bit half or for the whole 32 bit count when the pair is linked.

Table 556: TMR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTTMRB0																CTTMRA0															

Table 557: TMR0 Register Bits

Bit	Name	Reset	RW	Description
31:16	CTTMRB0	0x0	RO	Counter/Timer B0.
15:0	CTTMRA0	0x0	RO	Counter/Timer A0.

10.7.2.2 CMPRA0 Register

Counter/Timer A0 Compare Registers

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x40008004

Compare limits for timer half A.

Table 558: CMPRA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMPR1A0																CMPR0A0															

Table 559: CMPRA0 Register Bits

Bit	Name	Reset	RW	Description
31:16	CMPR1A0	0x0	RW	Counter/Timer A0 Compare Register 1. Holds the upper limit for timer half A.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 559: CMPRA0 Register Bits

Bit	Name	Reset	RW	Description
15:0	CMPR0A0	0x0	RW	Counter/Timer A0 Compare Register 0. Holds the lower limit for timer half A.

10.7.2.3 CMPRB0 Register

Counter/Timer B0 Compare Registers

OFFSET: 0x00000008

INSTANCE 0 ADDRESS: 0x40008008

Compare limits for timer half B.

Table 560: CMPRB0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMPR1B0																CMPR0B0															

Table 561: CMPRB0 Register Bits

Bit	Name	Reset	RW	Description
31:16	CMPR1B0	0x0	RW	Counter/Timer B0 Compare Register 1. Holds the upper limit for timer half B.
15:0	CMPR0B0	0x0	RW	Counter/Timer B0 Compare Register 0. Holds the lower limit for timer half B.

10.7.2.4 CTRL0 Register

Counter/Timer Control

OFFSET: 0x0000000C

INSTANCE 0 ADDRESS: 0x4000800C

Control bit fields for both halves of timer 0.

Table 562: CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTLINK0	RSVD	TMRB0PE	TMRB0POL	TMRB0CLR	TMRB0IE1	TMRB0IE0	TMRB0FN			TMRB0CLK					TMRB0EN	RSVD		TMRA0PE	TMRA0POL	TMRA0CLR	TMRA0IE1	TMRA0IE0	TMRA0FN			TMRA0CLK					TMRA0EN

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 563: CTRL0 Register Bits

Bit	Name	Reset	RW	Description
31	CTLINK0	0x0	RW	Counter/Timer A0/B0 Link bit. TWO_16BIT_TIMERS = 0x0 - Use A0/B0 timers as two independent 16-bit timers (default). 32BIT_TIMER = 0x1 - Link A0/B0 timers into a single 32-bit timer.
30	RSVD	0x0	RO	RESERVED
29	TMRB0PE	0x0	RW	Counter/Timer B0 Output Enable bit. DIS = 0x0 - Counter/Timer B holds the TMRPINB signal at the value TMRB0POL. EN = 0x1 - Enable counter/timer B0 to generate a signal on TMRPINB.
28	TMRB0POL	0x0	RW	Counter/Timer B0 output polarity. NORMAL = 0x0 - The polarity of the TMRPINB0 pin is the same as the timer output. INVERTED = 0x1 - The polarity of the TMRPINB0 pin is the inverse of the timer output.
27	TMRB0CLR	0x0	RW	Counter/Timer B0 Clear bit. RUN = 0x0 - Allow counter/timer B0 to run CLEAR = 0x1 - Holds counter/timer B0 at 0x0000.
26	TMRB0IE1	0x0	RW	Counter/Timer B0 Interrupt Enable bit for COMPR1. DIS = 0x0 - Disable counter/timer B0 from generating an interrupt based on COMPR1. EN = 0x1 - Enable counter/timer B0 to generate an interrupt based on COMPR1.
25	TMRB0IE0	0x0	RW	Counter/Timer B0 Interrupt Enable bit for COMPR0. DIS = 0x0 - Disable counter/timer B0 from generating an interrupt based on COMPR0. EN = 0x1 - Enable counter/timer B0 to generate an interrupt based on COMPR0
24:22	TMRB0FN	0x0	RW	Counter/Timer B0 Function Select. SINGLECOUNT = 0x0 - Single count (output toggles and sticks). Count to CMPR0B0, stop. REPEATEDCOUNT = 0x1 - Repeated count (periodic 1-clock-cycle-wide pulses). Count to CMPR0B0, restart. PULSE_ONCE = 0x2 - Pulse once (aka one-shot). Count to CMPR0B0, assert, count to CMPR1B0, deassert, stop. PULSE_CONT = 0x3 - Pulse continously. Count to CMPR0B0, assert, count to CMPR1B0, deassert, restart. CONTINUOUS = 0x4 - Continuous run (aka Free Run). Count continuously.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 563: CTRL0 Register Bits

Bit	Name	Reset	RW	Description
21:17	TMRB0CLK	0x0	RW	Counter/Timer B0 Clock Select. TMRPIN = 0x0 - Clock source is TMRPINB. HFRC_DIV4 = 0x1 - Clock source is HFRC / 4 HFRC_DIV16 = 0x2 - Clock source is HFRC / 16 HFRC_DIV256 = 0x3 - Clock source is HFRC / 256 HFRC_DIV1024 = 0x4 - Clock source is HFRC / 1024 HFRC_DIV4K = 0x5 - Clock source is HFRC / 4096 XT = 0x6 - Clock source is the XT (uncalibrated). XT_DIV2 = 0x7 - Clock source is XT / 2 XT_DIV16 = 0x8 - Clock source is XT / 16 XT_DIV256 = 0x9 - Clock source is XT / 256 LFRC_DIV2 = 0xA - Clock source is LFRC / 2 LFRC_DIV32 = 0xB - Clock source is LFRC / 32 LFRC_DIV1K = 0xC - Clock source is LFRC / 1024 LFRC = 0xD - Clock source is LFRC RTC_100HZ = 0xE - Clock source is 100 Hz from the current RTC oscillator. HCLK = 0xF - Clock source is HCLK. BUCKB = 0x10 - Clock source is buck converter stream from CORE Buck.
16	TMRB0EN	0x0	RW	Counter/Timer B0 Enable bit. DIS = 0x0 - Counter/Timer B0 Disable. EN = 0x1 - Counter/Timer B0 Enable.
15:14	RSVD	0x0	RO	RESERVED
13	TMRA0PE	0x0	RW	Counter/Timer A0 Output Enable bit. DIS = 0x0 - Counter/Timer A holds the TMRPINA signal at the value TMRA0POL. EN = 0x1 - Enable counter/timer A0 to generate a signal on TMRPINA.
12	TMRA0POL	0x0	RW	Counter/Timer A0 output polarity. NORMAL = 0x0 - The polarity of the TMRPINA0 pin is the same as the timer output. INVERTED = 0x1 - The polarity of the TMRPINA0 pin is the inverse of the timer output.
11	TMRA0CLR	0x0	RW	Counter/Timer A0 Clear bit. RUN = 0x0 - Allow counter/timer A0 to run CLEAR = 0x1 - Holds counter/timer A0 at 0x0000.
10	TMRA0IE1	0x0	RW	Counter/Timer A0 Interrupt Enable bit based on COMPR1. DIS = 0x0 - Disable counter/timer A0 from generating an interrupt based on COMPR1. EN = 0x1 - Enable counter/timer A0 to generate an interrupt based on COMPR1.
9	TMRA0IE0	0x0	RW	Counter/Timer A0 Interrupt Enable bit based on COMPR0. DIS = 0x0 - Disable counter/timer A0 from generating an interrupt based on COMPR0. EN = 0x1 - Enable counter/timer A0 to generate an interrupt based on COMPR0.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 563: CTRL0 Register Bits

Bit	Name	Reset	RW	Description
8:6	TMRA0FN	0x0	RW	Counter/Timer A0 Function Select. SINGLECOUNT = 0x0 - Single count (output toggles and sticks). Count to CMPR0A0, stop. REPEATEDCOUNT = 0x1 - Repeated count (periodic 1-clock-cycle-wide pulses). Count to CMPR0A0, restart. PULSE_ONCE = 0x2 - Pulse once (aka one-shot). Count to CMPR0A0, assert, count to CMPR1A0, deassert, stop. PULSE_CONT = 0x3 - Pulse continously. Count to CMPR0A0, assert, count to CMPR1A0, deassert, restart. CONTINUOUS = 0x4 - Continuous run (aka Free Run). Count continuously.
5:1	TMRA0CLK	0x0	RW	Counter/Timer A0 Clock Select. TMRPIN = 0x0 - Clock source is TMRPINA. HFRC_DIV4 = 0x1 - Clock source is HFRC / 4 HFRC_DIV16 = 0x2 - Clock source is HFRC / 16 HFRC_DIV256 = 0x3 - Clock source is HFRC / 256 HFRC_DIV1024 = 0x4 - Clock source is HFRC / 1024 HFRC_DIV4K = 0x5 - Clock source is HFRC / 4096 XT = 0x6 - Clock source is the XT (uncalibrated). XT_DIV2 = 0x7 - Clock source is XT / 2 XT_DIV16 = 0x8 - Clock source is XT / 16 XT_DIV256 = 0x9 - Clock source is XT / 256 LFRC_DIV2 = 0xA - Clock source is LFRC / 2 LFRC_DIV32 = 0xB - Clock source is LFRC / 32 LFRC_DIV1K = 0xC - Clock source is LFRC / 1024 LFRC = 0xD - Clock source is LFRC RTC_100HZ = 0xE - Clock source is 100 Hz from the current RTC oscillator. HCLK_DIV4 = 0xF - Clock source is HCLK / 4. BUCKA = 0x10 - Clock source is buck converter stream from MEM Buck.
0	TMRA0EN	0x0	RW	Counter/Timer A0 Enable bit. DIS = 0x0 - Counter/Timer A0 Disable. EN = 0x1 - Counter/Timer A0 Enable.

10.7.2.5 TMR1 Register

Counter/Timer Register

OFFSET: 0x00000010

INSTANCE 0 ADDRESS: 0x40008010

This register holds the running time or event count, either for each 16 bit half or for the whole 32 bit count when the pair is linked.

Table 564: TMR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTTMRB1																CTTMRA1															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 565: TMR1 Register Bits

Bit	Name	Reset	RW	Description
31:16	CTTMRB1	0x0	RO	Counter/Timer B1.
15:0	CTTMRA1	0x0	RO	Counter/Timer A1.

10.7.2.6 CMPRA1 Register

Counter/Timer A1 Compare Registers

OFFSET: 0x00000014

INSTANCE 0 ADDRESS: 0x40008014

This register holds the compare limits for timer half A.

Table 566: CMPRA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMPR1A1																CMPR0A1															

Table 567: CMPRA1 Register Bits

Bit	Name	Reset	RW	Description
31:16	CMPR1A1	0x0	RW	Counter/Timer A1 Compare Register 1.
15:0	CMPR0A1	0x0	RW	Counter/Timer A1 Compare Register 0.

10.7.2.7 CMPRB1 Register

Counter/Timer B1 Compare Registers

OFFSET: 0x00000018

INSTANCE 0 ADDRESS: 0x40008018

This register holds the compare limits for timer half B.

Table 568: CMPRB1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMPR1B1																CMPR0B1															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 569: CMPRB1 Register Bits

Bit	Name	Reset	RW	Description
31:16	CMPR1B1	0x0	RW	Counter/Timer B1 Compare Register 1.
15:0	CMPR0B1	0x0	RW	Counter/Timer B1 Compare Register 0.

10.7.2.8 CTRL1 Register

Counter/Timer Control

OFFSET: 0x0000001C

INSTANCE 0 ADDRESS: 0x4000801C

Control bit fields for both halves of timer 0.

Table 570: CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTLINK1	RSVD	TMRB1PE	TMRB1POL	TMRB1CLR	TMRB1IE1	TMRB1IE0	TMRB1FN			TMRB1CLK					TMRB1EN	RSVD		TMRA1PE	TMRA1POL	TMRA1CLR	TMRA1IE1	TMRA1IE0	TMRA1FN			TMRA1CLK					TMRA1EN

Table 571: CTRL1 Register Bits

Bit	Name	Reset	RW	Description
31	CTLINK1	0x0	RW	Counter/Timer A1/B1 Link bit. TWO_16BIT_TIMERS = 0x0 - Use A1/B1 timers as two independent 16-bit timers (default). 32BIT_TIMER = 0x1 - Link A1/B1 timers into a single 32-bit timer.
30	RSVD	0x0	RO	RESERVED
29	TMRB1PE	0x0	RW	Counter/Timer B1 Output Enable bit. DIS = 0x0 - Counter/Timer B holds the TMRPINB signal at the value TMRB1POL. EN = 0x1 - Enable counter/timer B1 to generate a signal on TMRPINB.
28	TMRB1POL	0x0	RW	Counter/Timer B1 output polarity. NORMAL = 0x0 - The polarity of the TMRPINB1 pin is the same as the timer output. INVERTED = 0x1 - The polarity of the TMRPINB1 pin is the inverse of the timer output.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 571: CTRL1 Register Bits

Bit	Name	Reset	RW	Description
27	TMRB1CLR	0x0	RW	Counter/Timer B1 Clear bit. RUN = 0x0 - Allow counter/timer B1 to run CLEAR = 0x1 - Holds counter/timer B1 at 0x0000.
26	TMRB1IE1	0x0	RW	Counter/Timer B1 Interrupt Enable bit for COMPR1. DIS = 0x0 - Disable counter/timer B1 from generating an interrupt based on COMPR1. EN = 0x1 - Enable counter/timer B1 to generate an interrupt based on COMPR1.
25	TMRB1IE0	0x0	RW	Counter/Timer B1 Interrupt Enable bit for COMPR0. DIS = 0x0 - Disable counter/timer B1 from generating an interrupt based on COMPR0. EN = 0x1 - Enable counter/timer B1 to generate an interrupt based on COMPR0
24:22	TMRB1FN	0x0	RW	Counter/Timer B1 Function Select. SINGLECOUNT = 0x0 - Single count (output toggles and sticks). Count to CMPR0B1, stop. REPEATEDCOUNT = 0x1 - Repeated count (periodic 1-clock-cycle-wide pulses). Count to CMPR0B1, restart. PULSE_ONCE = 0x2 - Pulse once (aka one-shot). Count to CMPR0B1, assert, count to CMPR1B1, deassert, stop. PULSE_CONT = 0x3 - Pulse continously. Count to CMPR0B1, assert, count to CMPR1B1, deassert, restart. CONTINUOUS = 0x4 - Continuous run (aka Free Run). Count continuously.
21:17	TMRB1CLK	0x0	RW	Counter/Timer B1 Clock Select. TMRPIN = 0x0 - Clock source is TMRPINB. HFRC_DIV4 = 0x1 - Clock source is HFRC / 4 HFRC_DIV16 = 0x2 - Clock source is HFRC / 16 HFRC_DIV256 = 0x3 - Clock source is HFRC / 256 HFRC_DIV1024 = 0x4 - Clock source is HFRC / 1024 HFRC_DIV4K = 0x5 - Clock source is HFRC / 4096 XT = 0x6 - Clock source is the XT (uncalibrated). XT_DIV2 = 0x7 - Clock source is XT / 2 XT_DIV16 = 0x8 - Clock source is XT / 16 XT_DIV256 = 0x9 - Clock source is XT / 256 LFRC_DIV2 = 0xA - Clock source is LFRC / 2 LFRC_DIV32 = 0xB - Clock source is LFRC / 32 LFRC_DIV1K = 0xC - Clock source is LFRC / 1024 LFRC = 0xD - Clock source is LFRC RTC_100HZ = 0xE - Clock source is 100 Hz from the current RTC oscillator. HCLK = 0xF - Clock source is HCLK. BUCKB = 0x10 - Clock source is buck converter stream from CORE Buck.
16	TMRB1EN	0x0	RW	Counter/Timer B1 Enable bit. DIS = 0x0 - Counter/Timer B1 Disable. EN = 0x1 - Counter/Timer B1 Enable.
15:14	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 571: CTRL1 Register Bits

Bit	Name	Reset	RW	Description
13	TMRA1PE	0x0	RW	Counter/Timer A1 Output Enable bit. DIS = 0x0 - Counter/Timer A holds the TMRPINA signal at the value TMRA1POL. EN = 0x1 - Enable counter/timer A1 to generate a signal on TMRPINA.
12	TMRA1POL	0x0	RW	Counter/Timer A1 output polarity. NORMAL = 0x0 - The polarity of the TMRPINA1 pin is the same as the timer output. INVERTED = 0x1 - The polarity of the TMRPINA1 pin is the inverse of the timer output.
11	TMRA1CLR	0x0	RW	Counter/Timer A1 Clear bit. RUN = 0x0 - Allow counter/timer A1 to run CLEAR = 0x1 - Holds counter/timer A1 at 0x0000.
10	TMRA1IE1	0x0	RW	Counter/Timer A1 Interrupt Enable bit based on COMPR1. DIS = 0x0 - Disable counter/timer A1 from generating an interrupt based on COMPR1. EN = 0x1 - Enable counter/timer A1 to generate an interrupt based on COMPR1.
9	TMRA1IE0	0x0	RW	Counter/Timer A1 Interrupt Enable bit based on COMPR0. DIS = 0x0 - Disable counter/timer A1 from generating an interrupt based on COMPR0. EN = 0x1 - Enable counter/timer A1 to generate an interrupt based on COMPR0.
8:6	TMRA1FN	0x0	RW	Counter/Timer A1 Function Select. SINGLECOUNT = 0x0 - Single count (output toggles and sticks). Count to CMPR0A1, stop. REPEATEDCOUNT = 0x1 - Repeated count (periodic 1-clock-cycle-wide pulses). Count to CMPR0A1, restart. PULSE_ONCE = 0x2 - Pulse once (aka one-shot). Count to CMPR0A1, assert, count to CMPR1A1, deassert, stop. PULSE_CONT = 0x3 - Pulse continously. Count to CMPR0A1, assert, count to CMPR1A1, deassert, restart. CONTINUOUS = 0x4 - Continuous run (aka Free Run). Count continuously.
5:1	TMRA1CLK	0x0	RW	Counter/Timer A1 Clock Select. TMRPIN = 0x0 - Clock source is TMRPINA. HFRC_DIV4 = 0x1 - Clock source is HFRC / 4 HFRC_DIV16 = 0x2 - Clock source is HFRC / 16 HFRC_DIV256 = 0x3 - Clock source is HFRC / 256 HFRC_DIV1024 = 0x4 - Clock source is HFRC / 1024 HFRC_DIV4K = 0x5 - Clock source is HFRC / 4096 XT = 0x6 - Clock source is the XT (uncalibrated). XT_DIV2 = 0x7 - Clock source is XT / 2 XT_DIV16 = 0x8 - Clock source is XT / 16 XT_DIV256 = 0x9 - Clock source is XT / 256 LFRC_DIV2 = 0xA - Clock source is LFRC / 2 LFRC_DIV32 = 0xB - Clock source is LFRC / 32 LFRC_DIV1K = 0xC - Clock source is LFRC / 1024 LFRC = 0xD - Clock source is LFRC RTC_100HZ = 0xE - Clock source is 100 Hz from the current RTC oscillator. HCLK = 0xF - Clock source is HCLK. BUCKA = 0x10 - Clock source is buck converter stream from MEM Buck.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 571: CTRL1 Register Bits

Bit	Name	Reset	RW	Description
0	TMRA1EN	0x0	RW	Counter/Timer A1 Enable bit. DIS = 0x0 - Counter/Timer A1 Disable. EN = 0x1 - Counter/Timer A1 Enable.

10.7.2.9 TMR2 Register

Counter/Timer Register

OFFSET: 0x00000020

INSTANCE 0 ADDRESS: 0x40008020

Counter/Timer Register

Table 572: TMR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTTMRB2																CTTMRA2															

Table 573: TMR2 Register Bits

Bit	Name	Reset	RW	Description
31:16	CTTMRB2	0x0	RO	Counter/Timer B2.
15:0	CTTMRA2	0x0	RO	Counter/Timer A2.

10.7.2.10CMPRA2 Register

Counter/Timer A2 Compare Registers

OFFSET: 0x00000024

INSTANCE 0 ADDRESS: 0x40008024

This register holds the compare limits for timer half A.

Table 574: CMPRA2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMPR1A2																CMPR0A2															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 575: CMPRA2 Register Bits

Bit	Name	Reset	RW	Description
31:16	CMPR1A2	0x0	RW	Counter/Timer A2 Compare Register 1.
15:0	CMPR0A2	0x0	RW	Counter/Timer A2 Compare Register 0.

10.7.2.11CMPRB2 Register

Counter/Timer B2 Compare Registers

OFFSET: 0x00000028

INSTANCE 0 ADDRESS: 0x40008028

This register holds the compare limits for timer half B.

Table 576: CMPRB2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMPR1B2																CMPR0B2															

Table 577: CMPRB2 Register Bits

Bit	Name	Reset	RW	Description
31:16	CMPR1B2	0x0	RW	Counter/Timer B2 Compare Register 1.
15:0	CMPR0B2	0x0	RW	Counter/Timer B2 Compare Register 0.

10.7.2.12CTRL2 Register

Counter/Timer Control

OFFSET: 0x0000002C

INSTANCE 0 ADDRESS: 0x4000802C

This register holds the control bit fields for both halves of timer 2.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 578: CTRL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTLINK2	RSVD	TMRB2PE	TMRB2POL	TMRB2CLR	TMRB2IE1	TMRB2IE0	TMRB2FN			TMRB2CLK					TMRB2EN	RSVD		TMRA2PE	TMRA2POL	TMRA2CLR	TMRA2IE1	TMRA2IE0	TMRA2FN			TMRA2CLK					TMRA2EN

Table 579: CTRL2 Register Bits

Bit	Name	Reset	RW	Description
31	CTLINK2	0x0	RW	Counter/Timer A2/B2 Link bit. TWO_16BIT_TIMERS = 0x0 - Use A2/B2 timers as two independent 16-bit timers (default). 32BIT_TIMER = 0x1 - Link A2/B2 timers into a single 32-bit timer.
30	RSVD	0x0	RO	RESERVED
29	TMRB2PE	0x0	RW	Counter/Timer B2 Output Enable bit. DIS = 0x0 - Counter/Timer B holds the TMRPINB signal at the value TMRB2POL. EN = 0x1 - Enable counter/timer B2 to generate a signal on TMRPINB.
28	TMRB2POL	0x0	RW	Counter/Timer B2 output polarity. NORMAL = 0x0 - The polarity of the TMRPINB2 pin is the same as the timer output. INVERTED = 0x1 - The polarity of the TMRPINB2 pin is the inverse of the timer output.
27	TMRB2CLR	0x0	RW	Counter/Timer B2 Clear bit. RUN = 0x0 - Allow counter/timer B2 to run CLEAR = 0x1 - Holds counter/timer B2 at 0x0000.
26	TMRB2IE1	0x0	RW	Counter/Timer B2 Interrupt Enable bit for COMPR1. DIS = 0x0 - Disable counter/timer B2 from generating an interrupt based on COMPR1. EN = 0x1 - Enable counter/timer B2 to generate an interrupt based on COM-PR1.
25	TMRB2IE0	0x0	RW	Counter/Timer B2 Interrupt Enable bit for COMPR0. DIS = 0x0 - Disable counter/timer B2 from generating an interrupt based on COMPR0. EN = 0x1 - Enable counter/timer B2 to generate an interrupt based on COM-PR0

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 579: CTRL2 Register Bits

Bit	Name	Reset	RW	Description
24:22	TMRB2FN	0x0	RW	Counter/Timer B2 Function Select. SINGLECOUNT = 0x0 - Single count (output toggles and sticks). Count to CMPR0B2, stop. REPEATEDCOUNT = 0x1 - Repeated count (periodic 1-clock-cycle-wide pulses). Count to CMPR0B2, restart. PULSE_ONCE = 0x2 - Pulse once (aka one-shot). Count to CMPR0B2, assert, count to CMPR1B2, deassert, stop. PULSE_CONT = 0x3 - Pulse continously. Count to CMPR0B2, assert, count to CMPR1B2, deassert, restart. CONTINUOUS = 0x4 - Continuous run (aka Free Run). Count continuously.
21:17	TMRB2CLK	0x0	RW	Counter/Timer B2 Clock Select. TMRPIN = 0x0 - Clock source is TMRPINB. HFRC_DIV4 = 0x1 - Clock source is HFRC / 4 HFRC_DIV16 = 0x2 - Clock source is HFRC / 16 HFRC_DIV256 = 0x3 - Clock source is HFRC / 256 HFRC_DIV1024 = 0x4 - Clock source is HFRC / 1024 HFRC_DIV4K = 0x5 - Clock source is HFRC / 4096 XT = 0x6 - Clock source is the XT (uncalibrated). XT_DIV2 = 0x7 - Clock source is XT / 2 XT_DIV16 = 0x8 - Clock source is XT / 16 XT_DIV256 = 0x9 - Clock source is XT / 256 LFRC_DIV2 = 0xA - Clock source is LFRC / 2 LFRC_DIV32 = 0xB - Clock source is LFRC / 32 LFRC_DIV1K = 0xC - Clock source is LFRC / 1024 LFRC = 0xD - Clock source is LFRC RTC_100HZ = 0xE - Clock source is 100 Hz from the current RTC oscillator. HCLK = 0xF - Clock source is HCLK. BUCKA = 0x10 - Clock source is buck converter stream from MEM Buck.
16	TMRB2EN	0x0	RW	Counter/Timer B2 Enable bit. DIS = 0x0 - Counter/Timer B2 Disable. EN = 0x1 - Counter/Timer B2 Enable.
15:14	RSVD	0x0	RO	RESERVED
13	TMRA2PE	0x0	RW	Counter/Timer A2 Output Enable bit. DIS = 0x0 - Counter/Timer A holds the TMRPINA signal at the value TMRA2POL. EN = 0x1 - Enable counter/timer A2 to generate a signal on TMRPINA.
12	TMRA2POL	0x0	RW	Counter/Timer A2 output polarity. NORMAL = 0x0 - The polarity of the TMRPINA2 pin is the same as the timer output. INVERTED = 0x1 - The polarity of the TMRPINA2 pin is the inverse of the timer output.
11	TMRA2CLR	0x0	RW	Counter/Timer A2 Clear bit. RUN = 0x0 - Allow counter/timer A2 to run CLEAR = 0x1 - Holds counter/timer A2 at 0x0000.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 579: CTRL2 Register Bits

Bit	Name	Reset	RW	Description
10	TMRA2IE1	0x0	RW	Counter/Timer A2 Interrupt Enable bit based on COMPR1. DIS = 0x0 - Disable counter/timer A2 from generating an interrupt based on COMPR1. EN = 0x1 - Enable counter/timer A2 to generate an interrupt based on COMPR1.
9	TMRA2IE0	0x0	RW	Counter/Timer A2 Interrupt Enable bit based on COMPR0. DIS = 0x0 - Disable counter/timer A2 from generating an interrupt based on COMPR0. EN = 0x1 - Enable counter/timer A2 to generate an interrupt based on COMPR0.
8:6	TMRA2FN	0x0	RW	Counter/Timer A2 Function Select. SINGLECOUNT = 0x0 - Single count (output toggles and sticks). Count to CMPR0A2, stop. REPEATEDCOUNT = 0x1 - Repeated count (periodic 1-clock-cycle-wide pulses). Count to CMPR0A2, restart. PULSE_ONCE = 0x2 - Pulse once (aka one-shot). Count to CMPR0A2, assert, count to CMPR1A2, deassert, stop. PULSE_CONT = 0x3 - Pulse continously. Count to CMPR0A2, assert, count to CMPR1A2, deassert, restart. CONTINUOUS = 0x4 - Continuous run (aka Free Run). Count continuously.
5:1	TMRA2CLK	0x0	RW	Counter/Timer A2 Clock Select. TMRPIN = 0x0 - Clock source is TMRPINA. HFRC_DIV4 = 0x1 - Clock source is HFRC / 4 HFRC_DIV16 = 0x2 - Clock source is HFRC / 16 HFRC_DIV256 = 0x3 - Clock source is HFRC / 256 HFRC_DIV1024 = 0x4 - Clock source is HFRC / 1024 HFRC_DIV4K = 0x5 - Clock source is HFRC / 4096 XT = 0x6 - Clock source is the XT (uncalibrated). XT_DIV2 = 0x7 - Clock source is XT / 2 XT_DIV16 = 0x8 - Clock source is XT / 16 XT_DIV256 = 0x9 - Clock source is XT / 256 LFRC_DIV2 = 0xA - Clock source is LFRC / 2 LFRC_DIV32 = 0xB - Clock source is LFRC / 32 LFRC_DIV1K = 0xC - Clock source is LFRC / 1024 LFRC = 0xD - Clock source is LFRC RTC_100HZ = 0xE - Clock source is 100 Hz from the current RTC oscillator. HCLK = 0xF - Clock source is HCLK. BUCKB = 0x10 - Clock source is buck converter stream from CORE Buck.
0	TMRA2EN	0x0	RW	Counter/Timer A2 Enable bit. DIS = 0x0 - Counter/Timer A2 Disable. EN = 0x1 - Counter/Timer A2 Enable.

10.7.2.13TMR3 Register

Counter/Timer Register

OFFSET: 0x00000030

INSTANCE 0 ADDRESS: 0x40008030

Counter/Timer Register

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 580: TMR3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTTMRB3																CTTMRA3															

Table 581: TMR3 Register Bits

Bit	Name	Reset	RW	Description
31:16	CTTMRB3	0x0	RO	Counter/Timer B3.
15:0	CTTMRA3	0x0	RO	Counter/Timer A3.

10.7.2.14CMPRA3 Register

Counter/Timer A3 Compare Registers

OFFSET: 0x00000034

INSTANCE 0 ADDRESS: 0x40008034

This register holds the compare limits for timer half A.

Table 582: CMPRA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMPR1A3																CMPR0A3															

Table 583: CMPRA3 Register Bits

Bit	Name	Reset	RW	Description
31:16	CMPR1A3	0x0	RW	Counter/Timer A3 Compare Register 1.
15:0	CMPR0A3	0x0	RW	Counter/Timer A3 Compare Register 0.

10.7.2.15CMPRB3 Register

Counter/Timer B3 Compare Registers

OFFSET: 0x00000038

INSTANCE 0 ADDRESS: 0x40008038

This register holds the compare limits for timer half B.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 584: CMPRB3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMPR1B3																CMPR0B3															

Table 585: CMPRB3 Register Bits

Bit	Name	Reset	RW	Description
31:16	CMPR1B3	0x0	RW	Counter/Timer B3 Compare Register 1.
15:0	CMPR0B3	0x0	RW	Counter/Timer B3 Compare Register 0.

10.7.2.16CTRL3 Register

Counter/Timer Control

OFFSET: 0x0000003C

INSTANCE 0 ADDRESS: 0x4000803C

This register holds the control bit fields for both halves of timer 3.

Table 586: CTRL3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTLINK3	RSVD	TMRB3PE	TMRB3POL	TMRB3CLR	TMRB3IE1	TMRB3IE0	TMRB3FN			TMRB3CLK					TMRB3EN	ADCEN	RSVD	TMRA3PE	TMRA3POL	TMRA3CLR	TMRA3IE1	TMRA3IE0	TMRA3FN			TMRA3CLK					TMRA3EN

Table 587: CTRL3 Register Bits

Bit	Name	Reset	RW	Description
31	CTLINK3	0x0	RW	Counter/Timer A3/B3 Link bit. TWO_16BIT_TIMERS = 0x0 - Use A3/B3 timers as two independent 16-bit timers (default). 32BIT_TIMER = 0x1 - Link A3/B3 timers into a single 32-bit timer.
30	RSVD	0x0	RO	RESERVED

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 587: CTRL3 Register Bits

Bit	Name	Reset	RW	Description
29	TMRB3PE	0x0	RW	Counter/Timer B3 Output Enable bit. DIS = 0x0 - Counter/Timer B holds the TMRPINB signal at the value TMRB3POL. EN = 0x1 - Enable counter/timer B3 to generate a signal on TMRPINB.
28	TMRB3POL	0x0	RW	Counter/Timer B3 output polarity. NORMAL = 0x0 - The polarity of the TMRPINB3 pin is the same as the timer output. INVERTED = 0x1 - The polarity of the TMRPINB3 pin is the inverse of the timer output.
27	TMRB3CLR	0x0	RW	Counter/Timer B3 Clear bit. RUN = 0x0 - Allow counter/timer B3 to run CLEAR = 0x1 - Holds counter/timer B3 at 0x0000.
26	TMRB3IE1	0x0	RW	Counter/Timer B3 Interrupt Enable bit for COMPR1. DIS = 0x0 - Disable counter/timer B3 from generating an interrupt based on COMPR1. EN = 0x1 - Enable counter/timer B3 to generate an interrupt based on COMPR1.
25	TMRB3IE0	0x0	RW	Counter/Timer B3 Interrupt Enable bit for COMPR0. DIS = 0x0 - Disable counter/timer B3 from generating an interrupt based on COMPR0. EN = 0x1 - Enable counter/timer B3 to generate an interrupt based on COMPR0
24:22	TMRB3FN	0x0	RW	Counter/Timer B3 Function Select. SINGLECOUNT = 0x0 - Single count (output toggles and sticks). Count to CMPR0B3, stop. REPEATEDCOUNT = 0x1 - Repeated count (periodic 1-clock-cycle-wide pulses). Count to CMPR0B3, restart. PULSE_ONCE = 0x2 - Pulse once (aka one-shot). Count to CMPR0B3, assert, count to CMPR1B3, deassert, stop. PULSE_CONT = 0x3 - Pulse continously. Count to CMPR0B3, assert, count to CMPR1B3, deassert, restart. CONTINUOUS = 0x4 - Continuous run (aka Free Run). Count continuously.
21:17	TMRB3CLK	0x0	RW	Counter/Timer B3 Clock Select. TMRPIN = 0x0 - Clock source is TMRPINB. HFRC_DIV4 = 0x1 - Clock source is HFRC / 4 HFRC_DIV16 = 0x2 - Clock source is HFRC / 16 HFRC_DIV256 = 0x3 - Clock source is HFRC / 256 HFRC_DIV1024 = 0x4 - Clock source is HFRC / 1024 HFRC_DIV4K = 0x5 - Clock source is HFRC / 4096 XT = 0x6 - Clock source is the XT (uncalibrated). XT_DIV2 = 0x7 - Clock source is XT / 2 XT_DIV16 = 0x8 - Clock source is XT / 16 XT_DIV256 = 0x9 - Clock source is XT / 256 LFRC_DIV2 = 0xA - Clock source is LFRC / 2 LFRC_DIV32 = 0xB - Clock source is LFRC / 32 LFRC_DIV1K = 0xC - Clock source is LFRC / 1024 LFRC = 0xD - Clock source is LFRC RTC_100HZ = 0xE - Clock source is 100 Hz from the current RTC oscillator. HCLK = 0xF - Clock source is HCLK. BUCKA = 0x10 - Clock source is buck converter stream from MEM Buck.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 587: CTRL3 Register Bits

Bit	Name	Reset	RW	Description
16	TMRB3EN	0x0	RW	Counter/Timer B3 Enable bit. DIS = 0x0 - Counter/Timer B3 Disable. EN = 0x1 - Counter/Timer B3 Enable.
15	ADCEN	0x0	RW	Special Timer A3 enable for ADC function.
14	RSVD	0x0	RO	RESERVED
13	TMRA3PE	0x0	RW	Counter/Timer A3 Output Enable bit. DIS = 0x0 - Counter/Timer A holds the TMRPINA signal at the value TMRA3POL. EN = 0x1 - Enable counter/timer A3 to generate a signal on TMRPINA.
12	TMRA3POL	0x0	RW	Counter/Timer A3 output polarity. NORMAL = 0x0 - The polarity of the TMRPINA3 pin is the same as the timer output. INVERTED = 0x1 - The polarity of the TMRPINA3 pin is the inverse of the timer output.
11	TMRA3CLR	0x0	RW	Counter/Timer A3 Clear bit. RUN = 0x0 - Allow counter/timer A3 to run CLEAR = 0x1 - Holds counter/timer A3 at 0x0000.
10	TMRA3IE1	0x0	RW	Counter/Timer A3 Interrupt Enable bit based on COMPR1. DIS = 0x0 - Disable counter/timer A3 from generating an interrupt based on COMPR1. EN = 0x1 - Enable counter/timer A3 to generate an interrupt based on COMPR1.
9	TMRA3IE0	0x0	RW	Counter/Timer A3 Interrupt Enable bit based on COMPR0. DIS = 0x0 - Disable counter/timer A3 from generating an interrupt based on COMPR0. EN = 0x1 - Enable counter/timer A3 to generate an interrupt based on COMPR0.
8:6	TMRA3FN	0x0	RW	Counter/Timer A3 Function Select. SINGLECOUNT = 0x0 - Single count (output toggles and sticks). Count to CMPR0A3, stop. REPEATEDCOUNT = 0x1 - Repeated count (periodic 1-clock-cycle-wide pulses). Count to CMPR0A3, restart. PULSE_ONCE = 0x2 - Pulse once (aka one-shot). Count to CMPR0A3, assert, count to CMPR1A3, deassert, stop. PULSE_CONT = 0x3 - Pulse continously. Count to CMPR0A3, assert, count to CMPR1A3, deassert, restart. CONTINUOUS = 0x4 - Continuous run (aka Free Run). Count continuously.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 587: CTRL3 Register Bits

Bit	Name	Reset	RW	Description
5:1	TMRA3CLK	0x0	RW	Counter/Timer A3 Clock Select. TMRPIN = 0x0 - Clock source is TMRPINA. HFRC_DIV4 = 0x1 - Clock source is HFRC / 4 HFRC_DIV16 = 0x2 - Clock source is HFRC / 16 HFRC_DIV256 = 0x3 - Clock source is HFRC / 256 HFRC_DIV1024 = 0x4 - Clock source is HFRC / 1024 HFRC_DIV4K = 0x5 - Clock source is HFRC / 4096 XT = 0x6 - Clock source is the XT (uncalibrated). XT_DIV2 = 0x7 - Clock source is XT / 2 XT_DIV16 = 0x8 - Clock source is XT / 16 XT_DIV256 = 0x9 - Clock source is XT / 256 LFRC_DIV2 = 0xA - Clock source is LFRC / 2 LFRC_DIV32 = 0xB - Clock source is LFRC / 32 LFRC_DIV1K = 0xC - Clock source is LFRC / 1024 LFRC = 0xD - Clock source is LFRC RTC_100HZ = 0xE - Clock source is 100 Hz from the current RTC oscillator. HCLK = 0xF - Clock source is HCLK. BUCKB = 0x10 - Clock source is buck converter stream from CORE Buck.
0	TMRA3EN	0x0	RW	Counter/Timer A3 Enable bit. DIS = 0x0 - Counter/Timer A3 Disable. EN = 0x1 - Counter/Timer A3 Enable.

10.7.2.17INTEN Register

Counter/Timer Interrupts: Enable

OFFSET: 0x00000200

INSTANCE 0 ADDRESS: 0x40008200

Set bits in this register to allow this module to generate the corresponding interrupt.

Table 588: INTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																CTMRB3C1INT	CTMRA3C1INT	CTMRB2C1INT	CTMRA2C1INT	CTMRB1C1INT	CTMRA1C1INT	CTMRB0C1INT	CTMRA0C1INT	CTMRB3C0INT	CTMRA3C0INT	CTMRB2C0INT	CTMRA2C0INT	CTMRB1C0INT	CTMRA1C0INT	CTMRB0C0INT	CTMRA0C0INT

Table 589: INTEN Register Bits

Bit	Name	Reset	RW	Description
31:16	RSVD	0x0	RO	RESERVED
15	CTMRB3C1INT	0x0	RW	Counter/Timer B3 interrupt based on COMPR1.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 589: INTEN Register Bits

Bit	Name	Reset	RW	Description
14	CTMRA3C1INT	0x0	RW	Counter/Timer A3 interrupt based on COMPR1.
13	CTMRB2C1INT	0x0	RW	Counter/Timer B2 interrupt based on COMPR1.
12	CTMRA2C1INT	0x0	RW	Counter/Timer A2 interrupt based on COMPR1.
11	CTMRB1C1INT	0x0	RW	Counter/Timer B1 interrupt based on COMPR1.
10	CTMRA1C1INT	0x0	RW	Counter/Timer A1 interrupt based on COMPR1.
9	CTMRB0C1INT	0x0	RW	Counter/Timer B0 interrupt based on COMPR1.
8	CTMRA0C1INT	0x0	RW	Counter/Timer A0 interrupt based on COMPR1.
7	CTMRB3C0INT	0x0	RW	Counter/Timer B3 interrupt based on COMPR0.
6	CTMRA3C0INT	0x0	RW	Counter/Timer A3 interrupt based on COMPR0.
5	CTMRB2C0INT	0x0	RW	Counter/Timer B2 interrupt based on COMPR0.
4	CTMRA2C0INT	0x0	RW	Counter/Timer A2 interrupt based on COMPR0.
3	CTMRB1C0INT	0x0	RW	Counter/Timer B1 interrupt based on COMPR0.
2	CTMRA1C0INT	0x0	RW	Counter/Timer A1 interrupt based on COMPR0.
1	CTMRB0C0INT	0x0	RW	Counter/Timer B0 interrupt based on COMPR0.
0	CTMRA0C0INT	0x0	RW	Counter/Timer A0 interrupt based on COMPR0.

10.7.2.18INTSTAT Register

Counter/Timer Interrupts: Status

OFFSET: 0x00000204

INSTANCE 0 ADDRESS: 0x40008204

Read bits from this register to discover the cause of a recent interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 590: INTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																CTMRB3C1INT	CTMRA3C1INT	CTMRB2C1INT	CTMRA2C1INT	CTMRB1C1INT	CTMRA1C1INT	CTMRB0C1INT	CTMRA0C1INT	CTMRB3C0INT	CTMRA3C0INT	CTMRB2C0INT	CTMRA2C0INT	CTMRB1C0INT	CTMRA1C0INT	CTMRB0C0INT	CTMRA0C0INT

Table 591: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:16	RSVD	0x0	RO	RESERVED
15	CTMRB3C1INT	0x0	RW	Counter/Timer B3 interrupt based on COMPR1.
14	CTMRA3C1INT	0x0	RW	Counter/Timer A3 interrupt based on COMPR1.
13	CTMRB2C1INT	0x0	RW	Counter/Timer B2 interrupt based on COMPR1.
12	CTMRA2C1INT	0x0	RW	Counter/Timer A2 interrupt based on COMPR1.
11	CTMRB1C1INT	0x0	RW	Counter/Timer B1 interrupt based on COMPR1.
10	CTMRA1C1INT	0x0	RW	Counter/Timer A1 interrupt based on COMPR1.
9	CTMRB0C1INT	0x0	RW	Counter/Timer B0 interrupt based on COMPR1.
8	CTMRA0C1INT	0x0	RW	Counter/Timer A0 interrupt based on COMPR1.
7	CTMRB3C0INT	0x0	RW	Counter/Timer B3 interrupt based on COMPR0.
6	CTMRA3C0INT	0x0	RW	Counter/Timer A3 interrupt based on COMPR0.
5	CTMRB2C0INT	0x0	RW	Counter/Timer B2 interrupt based on COMPR0.
4	CTMRA2C0INT	0x0	RW	Counter/Timer A2 interrupt based on COMPR0.
3	CTMRB1C0INT	0x0	RW	Counter/Timer B1 interrupt based on COMPR0.
2	CTMRA1C0INT	0x0	RW	Counter/Timer A1 interrupt based on COMPR0.
1	CTMRB0C0INT	0x0	RW	Counter/Timer B0 interrupt based on COMPR0.
0	CTMRA0C0INT	0x0	RW	Counter/Timer A0 interrupt based on COMPR0.

©2017 Ambiq Micro, Inc.
All rights reserved.

10.7.2.19INTCLR Register

Counter/Timer Interrupts: Clear

OFFSET: 0x00000208

INSTANCE 0 ADDRESS: 0x40008208

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 592: INTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																CTMRB3C1INT	CTMRA3C1INT	CTMRB2C1INT	CTMRA2C1INT	CTMRB1C1INT	CTMRA1C1INT	CTMRB0C1INT	CTMRA0C1INT	CTMRB3C0INT	CTMRA3C0INT	CTMRB2C0INT	CTMRA2C0INT	CTMRB1C0INT	CTMRA1C0INT	CTMRB0C0INT	CTMRA0C0INT

Table 593: INTCLR Register Bits

Bit	Name	Reset	RW	Description
31:16	RSVD	0x0	RO	RESERVED
15	CTMRB3C1INT	0x0	RW	Counter/Timer B3 interrupt based on COMPR1.
14	CTMRA3C1INT	0x0	RW	Counter/Timer A3 interrupt based on COMPR1.
13	CTMRB2C1INT	0x0	RW	Counter/Timer B2 interrupt based on COMPR1.
12	CTMRA2C1INT	0x0	RW	Counter/Timer A2 interrupt based on COMPR1.
11	CTMRB1C1INT	0x0	RW	Counter/Timer B1 interrupt based on COMPR1.
10	CTMRA1C1INT	0x0	RW	Counter/Timer A1 interrupt based on COMPR1.
9	CTMRB0C1INT	0x0	RW	Counter/Timer B0 interrupt based on COMPR1.
8	CTMRA0C1INT	0x0	RW	Counter/Timer A0 interrupt based on COMPR1.
7	CTMRB3C0INT	0x0	RW	Counter/Timer B3 interrupt based on COMPR0.
6	CTMRA3C0INT	0x0	RW	Counter/Timer A3 interrupt based on COMPR0.
5	CTMRB2C0INT	0x0	RW	Counter/Timer B2 interrupt based on COMPR0.
4	CTMRA2C0INT	0x0	RW	Counter/Timer A2 interrupt based on COMPR0.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 593: INTCLR Register Bits

Bit	Name	Reset	RW	Description
3	CTMRB1C0INT	0x0	RW	Counter/Timer B1 interrupt based on COMPR0.
2	CTMRA1C0INT	0x0	RW	Counter/Timer A1 interrupt based on COMPR0.
1	CTMRB0C0INT	0x0	RW	Counter/Timer B0 interrupt based on COMPR0.
0	CTMRA0C0INT	0x0	RW	Counter/Timer A0 interrupt based on COMPR0.

10.7.2.20INTSET Register

Counter/Timer Interrupts: Set

OFFSET: 0x0000020C

INSTANCE 0 ADDRESS: 0x4000820C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 594: INTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																CTMRB3C1INT	CTMRA3C1INT	CTMRB2C1INT	CTMRA2C1INT	CTMRB1C1INT	CTMRA1C1INT	CTMRB0C1INT	CTMRA0C1INT	CTMRB3C0INT	CTMRA3C0INT	CTMRB2C0INT	CTMRA2C0INT	CTMRB1C0INT	CTMRA1C0INT	CTMRB0C0INT	CTMRA0C0INT

Table 595: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:16	RSVD	0x0	RO	RESERVED
15	CTMRB3C1INT	0x0	RW	Counter/Timer B3 interrupt based on COMPR1.
14	CTMRA3C1INT	0x0	RW	Counter/Timer A3 interrupt based on COMPR1.
13	CTMRB2C1INT	0x0	RW	Counter/Timer B2 interrupt based on COMPR1.
12	CTMRA2C1INT	0x0	RW	Counter/Timer A2 interrupt based on COMPR1.
11	CTMRB1C1INT	0x0	RW	Counter/Timer B1 interrupt based on COMPR1.
10	CTMRA1C1INT	0x0	RW	Counter/Timer A1 interrupt based on COMPR1.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 595: INTSET Register Bits

Bit	Name	Reset	RW	Description
9	CTMRB0C1INT	0x0	RW	Counter/Timer B0 interrupt based on COMPR1.
8	CTMRA0C1INT	0x0	RW	Counter/Timer A0 interrupt based on COMPR1.
7	CTMRB3C0INT	0x0	RW	Counter/Timer B3 interrupt based on COMPR0.
6	CTMRA3C0INT	0x0	RW	Counter/Timer A3 interrupt based on COMPR0.
5	CTMRB2C0INT	0x0	RW	Counter/Timer B2 interrupt based on COMPR0.
4	CTMRA2C0INT	0x0	RW	Counter/Timer A2 interrupt based on COMPR0.
3	CTMRB1C0INT	0x0	RW	Counter/Timer B1 interrupt based on COMPR0.
2	CTMRA1C0INT	0x0	RW	Counter/Timer A1 interrupt based on COMPR0.
1	CTMRB0C0INT	0x0	RW	Counter/Timer B0 interrupt based on COMPR0.
0	CTMRA0C0INT	0x0	RW	Counter/Timer A0 interrupt based on COMPR0.

©2017 Ambiq Micro, Inc.
All rights reserved.

11. System Timer Module

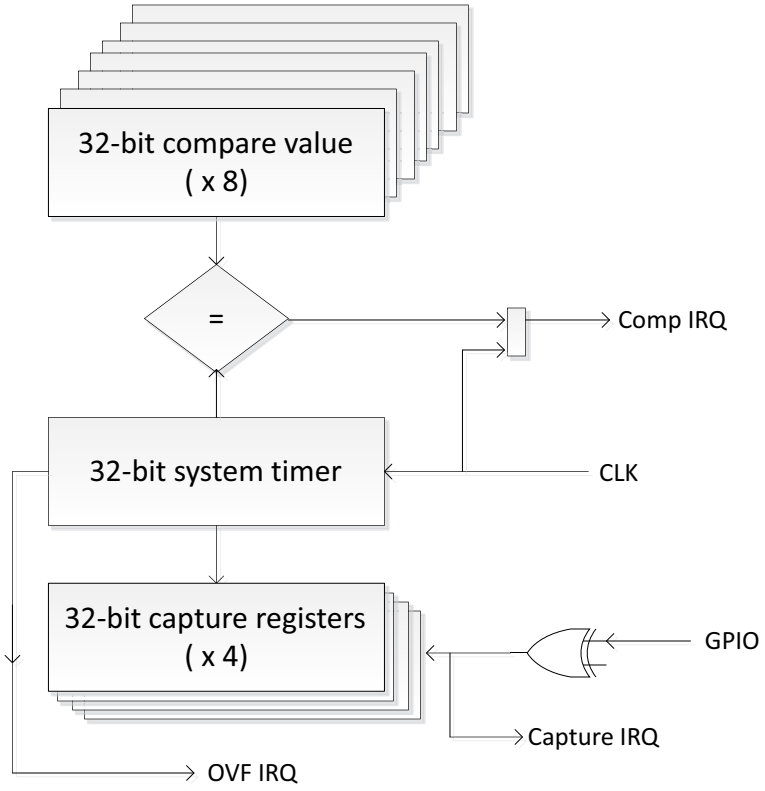


Figure 63. Block Diagram for the System Timer

11.1 Functional Overview

The Apollo2 Blue System Timer (STIMER), shown above in Figure 63, tracks the global synchronized counter. It can be used for RTOS scheduling and real-time system tracking. This timer is provided in addition to the other timer peripherals to enable software/firmware to have a simple, globally synchronized timer source.

The System Timer (STIMER) Module provides real time measurement for all task scheduling, sensor sample rate calibration, and tracking of real time and calendar maintenance. Key features are:

- 32-bit binary counter used for RTOS scheduling decisions.
- Eight 32-bit compare and interrupt registers to facilitate light weight scheduling (designs without RTOS).
- Accurate scheduling of comparator interrupts
- Only offsets from “NOW” are written to comparator registers.
- Maintains real time epoch for applications.
- Overflow interrupt to allow firmware to keep the extended part (more than 32-bits) of real time epoch.
- Time stamping hardware for multiple sensor streams (4 capture registers).
- Firmware handling of odd calculations such as Leap Second. It also handles things like surprise/legislated changes to the daylight savings time transition dates.
- Firmware handling of 1024 versus 1000 scaling of real time conversions.
- Only reset by POA (system cold reset) so that it retains time across all POI and POR (system warm reset) events except full power cycles.
- Contains three 32-bit NVRAM registers that are only reset by POA to maintain real time offset from epoch.

©2017 Ambiq Micro, Inc.
All rights reserved.

The heart of the STIMER is a single 32-bit counter that keeps track of current time for the application running on the Apollo2 Blue. This counter is reset at the actual power cycle reset of the MCU. It is generally never reset or changed again. Up to eight 32-bit comparator registers can be loaded each of which can generate an interrupt signal to the NVIC. Comparators A through H generate interrupt A through H while capture registers A through D and the overflow event generate interrupt I, all the way to the NVIC. Thus the scheduler can run these 9 interrupts at different priorities in the NVIC.

The comparator interrupts are each used to schedule a function (task) to run for the application. Thus these tasks run on interrupt levels at priorities lower than the I/O interrupts.

The overflow interrupt allows firmware to keep track of real time beyond that maintained in the 32-bit timer.

11.2 STIMER Registers

System Timer

INSTANCE 0 BASE ADDRESS:0x40008000

The System Timer block contains a 32-bit counter for system timer functions. This counter is the source for time-stamping events when performing capture or compare functions.

©2017 Ambiq Micro, Inc.
All rights reserved.

11.2.1 Register Memory Map

Table 596: STIMER Register Map

Address	Register Name	Description
0x40008100	STCFG	Configuration Register
0x40008104	STTMR	System Timer Count Register (Real Time Counter)
0x40008108	CAPTURE_CONTROL	Capture Control Register
0x40008110	SCMPR0	Compare Register A
0x40008114	SCMPR1	Compare Register B
0x40008118	SCMPR2	Compare Register C
0x4000811C	SCMPR3	Compare Register D
0x40008120	SCMPR4	Compare Register E
0x40008124	SCMPR5	Compare Register F
0x40008128	SCMPR6	Compare Register G
0x4000812C	SCMPR7	Compare Register H
0x400081E0	SCAPT0	Capture Register A
0x400081E4	SCAPT1	Capture Register B
0x400081E8	SCAPT2	Capture Register C
0x400081EC	SCAPT3	Capture Register D
0x400081F0	SNVR0	System Timer NVRAM_A Register
0x400081F4	SNVR1	System Timer NVRAM_B Register
0x400081F8	SNVR2	System Timer NVRAM_C Register
0x40008300	STMINTEN	STIMER Interrupt registers: Enable
0x40008304	STMINTSTAT	STIMER Interrupt registers: Status
0x40008308	STMINTCLR	STIMER Interrupt registers: Clear
0x4000830C	STMINTSET	STIMER Interrupt registers: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

11.2.2 STIMER Registers

11.2.2.1 STCFG Register

Configuration Register

OFFSET: 0x00000100

INSTANCE 0 ADDRESS: 0x40008100

The STIMER Configuration Register contains the software control for selecting the clock divider and source feeding the system timer.

Table 597: STCFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FREEZE	CLEAR	RSVD														COMPARE_H_EN	COMPARE_G_EN	COMPARE_F_EN	COMPARE_E_EN	COMPARE_D_EN	COMPARE_C_EN	COMPARE_B_EN	COMPARE_A_EN	RSVD				CLKSEL			

Table 598: STCFG Register Bits

Bit	Name	Reset	RW	Description
31	FREEZE	0x1	RW	Set this bit to one to freeze the clock input to the COUNTER register. Once frozen, the value can be safely written from the MCU. Unfreeze to resume. THAW = 0x0 - Let the COUNTER register run on its input clock. FREEZE = 0x1 - Stop the COUNTER register for loading.
30	CLEAR	0x0	RW	Set this bit to one to clear the System Timer register. If this bit is set to '1', the system timer register will stay cleared. It needs to be set to '0' for the system timer to start running. RUN = 0x0 - Let the COUNTER register run on its input clock. CLEAR = 0x1 - Stop the COUNTER register for loading.
29:16	RSVD	0x0	RO	RESERVED.
15	COMPARE_H_EN	0x0	RW	Selects whether compare is enabled for the corresponding SCMPR register. If compare is enabled, the interrupt status is set once the comparison is met. DISABLE = 0x0 - Compare H disabled. ENABLE = 0x1 - Compare H enabled.
14	COMPARE_G_EN	0x0	RW	Selects whether compare is enabled for the corresponding SCMPR register. If compare is enabled, the interrupt status is set once the comparison is met. DISABLE = 0x0 - Compare G disabled. ENABLE = 0x1 - Compare G enabled.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 598: STCFG Register Bits

Bit	Name	Reset	RW	Description
13	COMPARE_F_EN	0x0	RW	Selects whether compare is enabled for the corresponding SCMPR register. If compare is enabled, the interrupt status is set once the comparison is met. DISABLE = 0x0 - Compare F disabled. ENABLE = 0x1 - Compare F enabled.
12	COMPARE_E_EN	0x0	RW	Selects whether compare is enabled for the corresponding SCMPR register. If compare is enabled, the interrupt status is set once the comparison is met. DISABLE = 0x0 - Compare E disabled. ENABLE = 0x1 - Compare E enabled.
11	COMPARE_D_EN	0x0	RW	Selects whether compare is enabled for the corresponding SCMPR register. If compare is enabled, the interrupt status is set once the comparison is met. DISABLE = 0x0 - Compare D disabled. ENABLE = 0x1 - Compare D enabled.
10	COMPARE_C_EN	0x0	RW	Selects whether compare is enabled for the corresponding SCMPR register. If compare is enabled, the interrupt status is set once the comparison is met. DISABLE = 0x0 - Compare C disabled. ENABLE = 0x1 - Compare C enabled.
9	COMPARE_B_EN	0x0	RW	Selects whether compare is enabled for the corresponding SCMPR register. If compare is enabled, the interrupt status is set once the comparison is met. DISABLE = 0x0 - Compare B disabled. ENABLE = 0x1 - Compare B enabled.
8	COMPARE_A_EN	0x0	RW	Selects whether compare is enabled for the corresponding SCMPR register. If compare is enabled, the interrupt status is set once the comparison is met. DISABLE = 0x0 - Compare A disabled. ENABLE = 0x1 - Compare A enabled.
7:4	RSVD	0x0	RO	RESERVED.
3:0	CLKSEL	0x0	RW	Selects an appropriate clock source and divider to use for the System Timer clock. NOCLK = 0x0 - No clock enabled. HFRC_DIV16 = 0x1 - 3MHz from the HFRC clock divider. HFRC_DIV256 = 0x2 - 187.5KHz from the HFRC clock divider. XTAL_DIV1 = 0x3 - 32768Hz from the crystal oscillator. XTAL_DIV2 = 0x4 - 16384Hz from the crystal oscillator. XTAL_DIV32 = 0x5 - 1024Hz from the crystal oscillator. LFRC_DIV1 = 0x6 - Approximately 1KHz from the LFRC oscillator (uncalibrated). CTIMER0A = 0x7 - Use CTIMER 0 section A as a prescaler for the clock source. CTIMER0B = 0x8 - Use CTIMER 0 section B (or A and B linked together) as a prescaler for the clock source.

11.2.2.2 STTMR Register

System Timer Count Register (Real Time Counter)

OFFSET: 0x00000104

INSTANCE 0 ADDRESS: 0x40008104

©2017 Ambiq Micro, Inc.
All rights reserved.

The System Timer Count Register (STTMR) stores a running count of time as determined by its count being incremented on every rising clock edge of the clock source selected in the CLKSEL field of the REG_STIMER_STCFG register. It is this counter value that is captured in the capture registers and it is this counter value that is compared against the various compare registers. This register cannot be written, but can be cleared to 0 for a deterministic value, by setting the REG_STIMER_STCFG_FREEZE bit to stop the counter from incrementing, and then setting the REG_STIMER_STCFG_CLEAR bit. Clear the REG_STIMER_STCFG_FREEZE bit to restart the counter.

Table 599: STTMR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 600: STTMR Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RO	Value of the 32-bit counter as it ticks over.

11.2.2.3 CAPTURE_CONTROL Register

Capture Control Register

OFFSET: 0x00000108

INSTANCE 0 ADDRESS: 0x40008108

The STIMER Capture Control Register controls each of the 4 capture registers. It selects their GPIO pin number for a trigger source, enables a capture operation and sets the input polarity for the capture. NOTE: 8-bit writes can control individual capture registers atomically.

Table 601: CAPTURE_CONTROL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												CAPTURE_D	CAPTURE_C	CAPTURE_B	CAPTURE_A

Table 602: CAPTURE_CONTROL Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 602: CAPTURE_CONTROL Register Bits

Bit	Name	Reset	RW	Description
3	CAPTURE_D	0x0	RW	Selects whether capture is enabled for the specified capture register. DISABLE = 0x0 - Capture function disabled. ENABLE = 0x1 - Capture function enabled.
2	CAPTURE_C	0x0	RW	Selects whether capture is enabled for the specified capture register. DISABLE = 0x0 - Capture function disabled. ENABLE = 0x1 - Capture function enabled.
1	CAPTURE_B	0x0	RW	Selects whether capture is enabled for the specified capture register. DISABLE = 0x0 - Capture function disabled. ENABLE = 0x1 - Capture function enabled.
0	CAPTURE_A	0x0	RW	Selects whether capture is enabled for the specified capture register. DISABLE = 0x0 - Capture function disabled. ENABLE = 0x1 - Capture function enabled.

11.2.2.4 SCMPR0 Register

Compare Register A

OFFSET: 0x00000110

INSTANCE 0 ADDRESS: 0x40008110

The VALUE in this bit field is used to compare against the VALUE in the COUNTER register. If the match criterion in the configuration register is met then a corresponding interrupt status bit is set. The match criterion is defined as COUNTER equal to COMPARE. To establish a desired value in this COMPARE register, write the number of ticks in the future to this register to indicate when to interrupt. The hardware does the addition to the COUNTER value in the STIMER clock domain so that the math is precise. Reading this register shows the COUNTER value at which this interrupt will occur.

Table 603: SCMPR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 604: SCMPR0 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Compare this value to the value in the COUNTER register according to the match criterion, as selected in the COMPARE_A_EN bit in the REG_CTIMER_STCGF register.

©2017 Ambiq Micro, Inc.
All rights reserved.

11.2.2.5 SCMPR1 Register

Compare Register B

OFFSET: 0x00000114

INSTANCE 0 ADDRESS: 0x40008114

The VALUE in this bit field is used to compare against the VALUE in the COUNTER register. If the match criterion in the configuration register is met then a corresponding interrupt status bit is set. The match criterion is defined as COUNTER equal to COMPARE. To establish a desired value in this COMPARE register, write the number of ticks in the future to this register to indicate when to interrupt. The hardware does the addition to the COUNTER value in the STIMER clock domain so that the math is precise. Reading this register shows the COUNTER value at which this interrupt will occur.

Table 605: SCMPR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 606: SCMPR1 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Compare this value to the value in the COUNTER register according to the match criterion, as selected in the COMPARE_B_EN bit in the REG_CTIMER_STCGF register.

11.2.2.6 SCMPR2 Register

Compare Register C

OFFSET: 0x00000118

INSTANCE 0 ADDRESS: 0x40008118

The VALUE in this bit field is used to compare against the VALUE in the COUNTER register. If the match criterion in the configuration register is met then a corresponding interrupt status bit is set. The match criterion is defined as COUNTER equal to COMPARE. To establish a desired value in this COMPARE register, write the number of ticks in the future to this register to indicate when to interrupt. The hardware does the addition to the COUNTER value in the STIMER clock domain so that the math is precise. Reading this register shows the COUNTER value at which this interrupt will occur.

Table 607: SCMPR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 608: SCMPR2 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Compare this value to the value in the COUNTER register according to the match criterion, as selected in the COMPARE_C_EN bit in the REG_CTIMER_STCGF register.

11.2.2.7 SCMPR3 Register

Compare Register D

OFFSET: 0x0000011C

INSTANCE 0 ADDRESS: 0x4000811C

The VALUE in this bit field is used to compare against the VALUE in the COUNTER register. If the match criterion in the configuration register is met then a corresponding interrupt status bit is set. The match criterion is defined as COUNTER equal to COMPARE. To establish a desired value in this COMPARE register, write the number of ticks in the future to this register to indicate when to interrupt. The hardware does the addition to the COUNTER value in the STIMER clock domain so that the math is precise. Reading this register shows the COUNTER value at which this interrupt will occur.

Table 609: SCMPR3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 610: SCMPR3 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Compare this value to the value in the COUNTER register according to the match criterion, as selected in the COMPARE_D_EN bit in the REG_CTIMER_STCGF register.

11.2.2.8 SCMPR4 Register

Compare Register E

OFFSET: 0x00000120

INSTANCE 0 ADDRESS: 0x40008120

The VALUE in this bit field is used to compare against the VALUE in the COUNTER register. If the match criterion in the configuration register is met then a corresponding interrupt status bit is set. The match criterion is defined as COUNTER equal to COMPARE. To establish a desired value in this COMPARE register, write the number of ticks in the future to this register to indicate when to interrupt. The hardware does the addition to the COUNTER value in the STIMER clock domain so that the math is precise. Reading this register shows the COUNTER value at which this interrupt will occur.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 611: SCMPR4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 612: SCMPR4 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Compare this value to the value in the COUNTER register according to the match criterion, as selected in the COMPARE_E_EN bit in the REG_CTIMER_STCGF register.

11.2.2.9 SCMPR5 Register

Compare Register F

OFFSET: 0x00000124

INSTANCE 0 ADDRESS: 0x40008124

The VALUE in this bit field is used to compare against the VALUE in the COUNTER register. If the match criterion in the configuration register is met then a corresponding interrupt status bit is set. The match criterion is defined as COUNTER equal to COMPARE. To establish a desired value in this COMPARE register, write the number of ticks in the future to this register to indicate when to interrupt. The hardware does the addition to the COUNTER value in the STIMER clock domain so that the math is precise. Reading this register shows the COUNTER value at which this interrupt will occur.

Table 613: SCMPR5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 614: SCMPR5 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Compare this value to the value in the COUNTER register according to the match criterion, as selected in the COMPARE_F_EN bit in the REG_CTIMER_STCGF register.

11.2.2.10SCMPR6 Register

Compare Register G

OFFSET: 0x00000128

©2017 Ambiq Micro, Inc.
All rights reserved.

INSTANCE 0 ADDRESS: 0x40008128

The VALUE in this bit field is used to compare against the VALUE in the COUNTER register. If the match criterion in the configuration register is met then a corresponding interrupt status bit is set. The match criterion is defined as COUNTER equal to COMPARE. To establish a desired value in this COMPARE register, write the number of ticks in the future to this register to indicate when to interrupt. The hardware does the addition to the COUNTER value in the STIMER clock domain so that the math is precise. Reading this register shows the COUNTER value at which this interrupt will occur.

Table 615: SCMPR6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 616: SCMPR6 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Compare this value to the value in the COUNTER register according to the match criterion, as selected in the COMPARE_G_EN bit in the REG_CTIMER_STCGF register.

11.2.2.11 SCMPR7 Register

Compare Register H

OFFSET: 0x0000012C

INSTANCE 0 ADDRESS: 0x4000812C

The VALUE in this bit field is used to compare against the VALUE in the COUNTER register. If the match criterion in the configuration register is met then a corresponding interrupt status bit is set. The match criterion is defined as COUNTER equal to COMPARE. To establish a desired value in this COMPARE register, write the number of ticks in the future to this register to indicate when to interrupt. The hardware does the addition to the COUNTER value in the STIMER clock domain so that the math is precise.

Table 617: SCMPR7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 618: SCMPR7 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Compare this value to the value in the COUNTER register according to the match criterion, as selected in the COMPARE_H_EN bit in the REG_CTIMER_STCGF register.

11.2.2.12SCAPT0 Register

Capture Register A

OFFSET: 0x000001E0

INSTANCE 0 ADDRESS: 0x400081E0

The STIMER capture Register A grabs the VALUE in the COUNTER register whenever capture condition (event) A is asserted. This register holds a time stamp for the event.

Table 619: SCAPT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 620: SCAPT0 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RO	Whenever the event is detected, the value in the COUNTER is copied into this register and the corresponding interrupt status bit is set.

11.2.2.13SCAPT1 Register

Capture Register B

OFFSET: 0x000001E4

INSTANCE 0 ADDRESS: 0x400081E4

The STIMER capture Register B grabs the VALUE in the COUNTER register whenever capture condition (event) B is asserted. This register holds a time stamp for the event.

Table 621: SCAPT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 622: SCAPT1 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RO	Whenever the event is detected, the value in the COUNTER is copied into this register and the corresponding interrupt status bit is set.

11.2.2.14SCAPT2 Register

Capture Register C

OFFSET: 0x000001E8

INSTANCE 0 ADDRESS: 0x400081E8

The STIMER capture Register C grabs the VALUE in the COUNTER register whenever capture condition (event) C is asserted. This register holds a time stamp for the event.

Table 623: SCAPT2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 624: SCAPT2 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RO	Whenever the event is detected, the value in the COUNTER is copied into this register and the corresponding interrupt status bit is set.

11.2.2.15SCAPT3 Register

Capture Register D

OFFSET: 0x000001EC

INSTANCE 0 ADDRESS: 0x400081EC

The STIMER capture Register D grabs the VALUE in the COUNTER register whenever capture condition (event) D is asserted. This register holds a time stamp for the event.

Table 625: SCAPT3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 626: SCAPT3 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RO	Whenever the event is detected, the value in the COUNTER is copied into this register and the corresponding interrupt status bit is set.

11.2.2.16SNVR0 Register

System Timer NVRAM_A Register

OFFSET: 0x000001F0

INSTANCE 0 ADDRESS: 0x400081F0

The NVRAM_A Register contains a portion of the stored epoch offset associated with the time in the COUNTER register. This register is only reset by POI not by HRESETn. Its contents are intended to survive all reset level except POI and full power cycles.

Table 627: SNVR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 628: SNVR0 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Value of the 32-bit counter as it ticks over.

11.2.2.17SNVR1 Register

System Timer NVRAM_B Register

OFFSET: 0x000001F4

INSTANCE 0 ADDRESS: 0x400081F4

The NVRAM_B Register contains a portion of the stored epoch offset associated with the time in the COUNTER register. This register is only reset by POI not by HRESETn. Its contents are intended to survive all reset level except POI and full power cycles.

Table 629: SNVR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 630: SNVR1 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Value of the 32-bit counter as it ticks over.

11.2.2.18SNVR2 Register

System Timer NVRAM_C Register

OFFSET: 0x000001F8

INSTANCE 0 ADDRESS: 0x400081F8

The NVRAM_C Register contains a portion of the stored epoch offset associated with the time in the COUNTER register. This register is only reset by POI not by HRESETn. Its contents are intended to survive all reset level except POI and full power cycles.

Table 631: SNVR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALUE																															

Table 632: SNVR2 Register Bits

Bit	Name	Reset	RW	Description
31:0	VALUE	0x0	RW	Value of the 32-bit counter as it ticks over.

11.2.2.19STMINTEN Register

STIMER Interrupt registers: Enable

OFFSET: 0x00000300

INSTANCE 0 ADDRESS: 0x40008300

Set bits in this register to allow this module to generate the corresponding interrupt.

Table 633: STMINTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																			CAPTURED	CAPTUREC	CAPTUREB	CAPTUREA	OVERFLOW	COMPAREH	COMPAREG	COMPAREF	COMPAREE	COMPARED	COMPAREC	COMPAREB	COMPAREA

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 634: STMINTEN Register Bits

Bit	Name	Reset	RW	Description
31:13	RSVD	0x0	RO	RESERVED.
12	CAPTURED	0x0	RW	CAPTURE register D has grabbed the value in the counter CAPD_INT = 0x1 - Capture D interrupt status bit was set.
11	CAPTUREC	0x0	RW	CAPTURE register C has grabbed the value in the counter CAPC_INT = 0x1 - CAPTURE C interrupt status bit was set.
10	CAPTUREB	0x0	RW	CAPTURE register B has grabbed the value in the counter CAPB_INT = 0x1 - CAPTURE B interrupt status bit was set.
9	CAPTUREA	0x0	RW	CAPTURE register A has grabbed the value in the counter CAPA_INT = 0x1 - CAPTURE A interrupt status bit was set.
8	OVERFLOW	0x0	RW	COUNTER over flowed from 0xFFFFFFFF back to 0x00000000. OFLOW_INT = 0x1 - Overflow interrupt status bit was set.
7	COMPAREH	0x0	RW	COUNTER is greater than or equal to COMPARE register H. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
6	COMPAREG	0x0	RW	COUNTER is greater than or equal to COMPARE register G. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
5	COMPAREF	0x0	RW	COUNTER is greater than or equal to COMPARE register F. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
4	COMPAREE	0x0	RW	COUNTER is greater than or equal to COMPARE register E. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
3	COMPARED	0x0	RW	COUNTER is greater than or equal to COMPARE register D. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
2	COMPAREC	0x0	RW	COUNTER is greater than or equal to COMPARE register C. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
1	COMPAREB	0x0	RW	COUNTER is greater than or equal to COMPARE register B. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
0	COMPAREA	0x0	RW	COUNTER is greater than or equal to COMPARE register A. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.

©2017 Ambiq Micro, Inc.
All rights reserved.

11.2.2.20STMINTSTAT Register

STIMER Interrupt registers: Status

OFFSET: 0x00000304

INSTANCE 0 ADDRESS: 0x40008304

Read bits from this register to discover the cause of a recent interrupt.

Table 635: STMINTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																			CAPTURED	CAPTUREC	CAPTUREB	CAPTUREA	OVERFLOW	COMPAREH	COMPAREG	COMPAREF	COMPAREE	COMPARED	COMPAREC	COMPAREB	COMPAREA

Table 636: STMINTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:13	RSVD	0x0	RO	RESERVED.
12	CAPTURED	0x0	RW	CAPTURE register D has grabbed the value in the counter CAPD_INT = 0x1 - Capture D interrupt status bit was set.
11	CAPTUREC	0x0	RW	CAPTURE register C has grabbed the value in the counter CAPC_INT = 0x1 - CAPTURE C interrupt status bit was set.
10	CAPTUREB	0x0	RW	CAPTURE register B has grabbed the value in the counter CAPB_INT = 0x1 - CAPTURE B interrupt status bit was set.
9	CAPTUREA	0x0	RW	CAPTURE register A has grabbed the value in the counter CAPA_INT = 0x1 - CAPTURE A interrupt status bit was set.
8	OVERFLOW	0x0	RW	COUNTER over flowed from 0xFFFFFFFF back to 0x00000000. OFLOW_INT = 0x1 - Overflow interrupt status bit was set.
7	COMPAREH	0x0	RW	COUNTER is greater than or equal to COMPARE register H. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
6	COMPAREG	0x0	RW	COUNTER is greater than or equal to COMPARE register G. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
5	COMPAREF	0x0	RW	COUNTER is greater than or equal to COMPARE register F. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 636: STMINTSTAT Register Bits

Bit	Name	Reset	RW	Description
4	COMPAREE	0x0	RW	COUNTER is greater than or equal to COMPARE register E. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
3	COMPARED	0x0	RW	COUNTER is greater than or equal to COMPARE register D. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
2	COMPAREC	0x0	RW	COUNTER is greater than or equal to COMPARE register C. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
1	COMPAREB	0x0	RW	COUNTER is greater than or equal to COMPARE register B. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
0	COMPAREA	0x0	RW	COUNTER is greater than or equal to COMPARE register A. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.

11.2.2.21STMINTCLR Register

STIMER Interrupt registers: Clear

OFFSET: 0x00000308

INSTANCE 0 ADDRESS: 0x40008308

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 637: STMINTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																			CAPTURED	CAPTUREC	CAPTUREB	CAPTUREA	OVERFLOW	COMPAREH	COMPAREG	COMPAREF	COMPAREE	COMPARED	COMPAREC	COMPAREB	COMPAREA

Table 638: STMINTCLR Register Bits

Bit	Name	Reset	RW	Description
31:13	RSVD	0x0	RO	RESERVED.
12	CAPTURED	0x0	RW	CAPTURE register D has grabbed the value in the counter CAPD_INT = 0x1 - Capture D interrupt status bit was set.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 638: STMINTCLR Register Bits

Bit	Name	Reset	RW	Description
11	CAPTUREC	0x0	RW	CAPTURE register C has grabbed the value in the counter CAPC_INT = 0x1 - CAPTURE C interrupt status bit was set.
10	CAPTUREB	0x0	RW	CAPTURE register B has grabbed the value in the counter CAPB_INT = 0x1 - CAPTURE B interrupt status bit was set.
9	CAPTUREA	0x0	RW	CAPTURE register A has grabbed the value in the counter CAPA_INT = 0x1 - CAPTURE A interrupt status bit was set.
8	OVERFLOW	0x0	RW	COUNTER over flowed from 0xFFFFFFFF back to 0x00000000. OFLOW_INT = 0x1 - Overflow interrupt status bit was set.
7	COMPAREH	0x0	RW	COUNTER is greater than or equal to COMPARE register H. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
6	COMPAREG	0x0	RW	COUNTER is greater than or equal to COMPARE register G. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
5	COMPAREF	0x0	RW	COUNTER is greater than or equal to COMPARE register F. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
4	COMPAREE	0x0	RW	COUNTER is greater than or equal to COMPARE register E. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
3	COMPARED	0x0	RW	COUNTER is greater than or equal to COMPARE register D. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
2	COMPAREC	0x0	RW	COUNTER is greater than or equal to COMPARE register C. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
1	COMPAREB	0x0	RW	COUNTER is greater than or equal to COMPARE register B. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
0	COMPAREA	0x0	RW	COUNTER is greater than or equal to COMPARE register A. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.

11.2.2.22STMINTSET Register

STIMER Interrupt registers: Set

OFFSET: 0x0000030C

INSTANCE 0 ADDRESS: 0x4000830C

©2017 Ambiq Micro, Inc.
All rights reserved.

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 639: STMINTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																			CAPTURED	CAPTUREC	CAPTUREB	CAPTUREA	OVERFLOW	COMPAREH	COMPAREG	COMPAREF	COMPAREE	COMPARED	COMPAREC	COMPAREB	COMPAREA

Table 640: STMINTSET Register Bits

Bit	Name	Reset	RW	Description
31:13	RSVD	0x0	RO	RESERVED.
12	CAPTURED	0x0	RW	CAPTURE register D has grabbed the value in the counter CAPD_INT = 0x1 - Capture D interrupt status bit was set.
11	CAPTUREC	0x0	RW	CAPTURE register C has grabbed the value in the counter CAPC_INT = 0x1 - CAPTURE C interrupt status bit was set.
10	CAPTUREB	0x0	RW	CAPTURE register B has grabbed the value in the counter CAPB_INT = 0x1 - CAPTURE B interrupt status bit was set.
9	CAPTUREA	0x0	RW	CAPTURE register A has grabbed the value in the counter CAPA_INT = 0x1 - CAPTURE A interrupt status bit was set.
8	OVERFLOW	0x0	RW	COUNTER over flowed from 0xFFFFFFFF back to 0x00000000. OFLOW_INT = 0x1 - Overflow interrupt status bit was set.
7	COMPAREH	0x0	RW	COUNTER is greater than or equal to COMPARE register H. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
6	COMPAREG	0x0	RW	COUNTER is greater than or equal to COMPARE register G. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
5	COMPAREF	0x0	RW	COUNTER is greater than or equal to COMPARE register F. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
4	COMPAREE	0x0	RW	COUNTER is greater than or equal to COMPARE register E. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 640: STMINTSET Register Bits

Bit	Name	Reset	RW	Description
3	COMPARED	0x0	RW	COUNTER is greater than or equal to COMPARE register D. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
2	COMPAREC	0x0	RW	COUNTER is greater than or equal to COMPARE register C. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
1	COMPAREB	0x0	RW	COUNTER is greater than or equal to COMPARE register B. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.
0	COMPAREA	0x0	RW	COUNTER is greater than or equal to COMPARE register A. COMPARED = 0x1 - COUNTER greater than or equal to COMPARE register.

©2017 Ambiq Micro, Inc.
All rights reserved.

12. Watchdog Timer Module

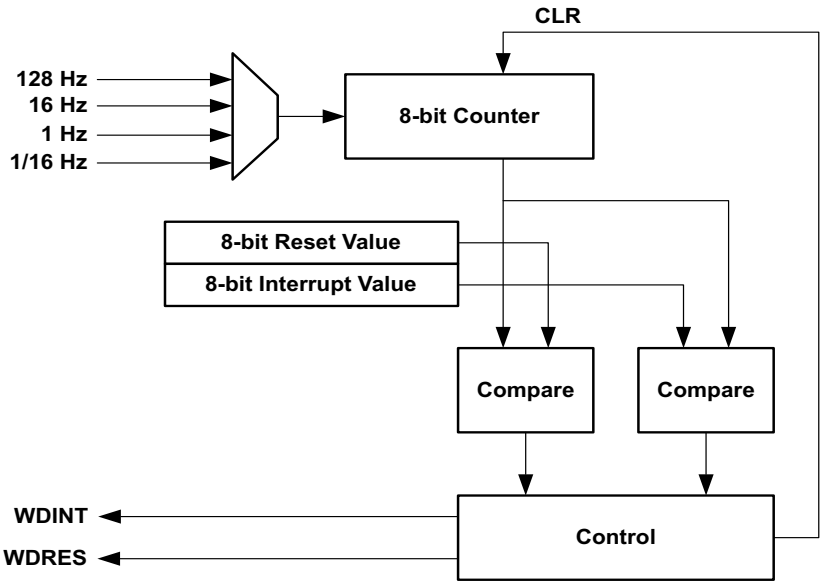


Figure 64. Block diagram for the Watchdog Timer Module

12.1 Functional Overview

The Watchdog Timer (WDT), shown in Figure 64, is used to insure that software is operational, by resetting the Apollo2 Blue if the WDT reaches a configurable value before being cleared by software. The WDT can be clocked by one of four selectable prescalers of the always active low-power LFRC clock, but is nominally clocked at 128 Hz. The WDT may be locked to ensure that software cannot disable its functionality, in which case the WDTCFG register cannot be updated. An interrupt can also be generated at a different counter value to implement an early warning function. Note: The RESEN bit in the WDTCFG register must be set and the WDREN bit in the RSTCFG register must be set to enable a watchdog timer reset condition.

12.2 WDT Registers

Watchdog Timer

INSTANCE 0 BASE ADDRESS:0x40024000

©2017 Ambiq Micro, Inc.
All rights reserved.

12.2.1 Register Memory Map

Table 641: WDT Register Map

Address(s)	Register Name	Description
0x40024000	CFG	Configuration Register
0x40024004	RSTRT	Restart the watchdog timer
0x40024008	LOCK	Locks the WDT
0x4002400C	COUNT	Current Counter Value for WDT
0x40024200	INTEN	WDT Interrupt register: Enable
0x40024204	INTSTAT	WDT Interrupt register: Status
0x40024208	INTCLR	WDT Interrupt register: Clear
0x4002420C	INTSET	WDT Interrupt register: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

12.2.2 WDT Registers

12.2.2.1 CFG Register

Configuration Register

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x40024000

Configuration Register

Table 642: CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD					CLKSEL			INTVAL								RESVAL								RSVD						RESEN	INTEN	WDTEN

Table 643: CFG Register Bits

Bit	Name	Reset	RW	Description
31:27	RSVD	0x0	RO	This bitfield is reserved for future use.
26:24	CLKSEL	0x0	RW	Select the frequency for the WDT. All values not enumerated below are undefined. OFF = 0x0 - Low Power Mode. 128HZ = 0x1 - 128 Hz LFRC clock. 16HZ = 0x2 - 16 Hz LFRC clock. 1HZ = 0x3 - 1 Hz LFRC clock. 1_16HZ = 0x4 - 1/16th Hz LFRC clock.
23:16	INTVAL	0xff	RW	This bitfield is the compare value for counter bits 7:0 to generate a watchdog interrupt.
15:8	RESVAL	0xff	RW	This bitfield is the compare value for counter bits 7:0 to generate a watchdog reset.
7:3	RSVD	0x0	RO	This bitfield is reserved for future use.
2	RESEN	0x0	RW	This bitfield enables the WDT reset.
1	INTEN	0x0	RW	This bitfield enables the WDT interrupt. Note : This bit must be set before the interrupt status bit will reflect a watchdog timer expiration. The IER interrupt register must also be enabled for a WDT interrupt to be sent to the NVIC.
0	WDTEN	0x0	RW	This bitfield enables the WDT.

©2017 Ambiq Micro, Inc.
All rights reserved.

12.2.2.2 RSTRT Register

Restart the watchdog timer

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x40024004

Restart the watchdog timer

Table 644: RSTRT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								RSTRT							

Table 645: RSTRT Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	This bitfield is reserved for future use.
7:0	RSTRT	0x0	WO	Writing 0xB2 to WDTRSTRT restarts the watchdog timer. KEYVALUE = 0xB2 - This is the key value to write to WDTRSTRT to restart the WDT.

12.2.2.3 LOCK Register

Locks the WDT

OFFSET: 0x00000008

INSTANCE 0 ADDRESS: 0x40024008

Locks the WDT

Table 646: LOCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								LOCK							

Table 647: LOCK Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	This bitfield is reserved for future use.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 647: LOCK Register Bits

Bit	Name	Reset	RW	Description
7:0	LOCK	0x0	WO	Writing 0x3A locks the watchdog timer. Once locked, the WDTCFG reg cannot be written and WDTEN is set. KEYVALUE = 0x3A - This is the key value to write to WDTLOCK to lock the WDT.

12.2.2.4 COUNT Register

Current Counter Value for WDT

OFFSET: 0x0000000C

INSTANCE 0 ADDRESS: 0x4002400C

Current Counter Value for WDT

Table 648: COUNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								COUNT							

Table 649: COUNT Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	This bitfield is reserved for future use.
7:0	COUNT	0x0	RO	Read-Only current value of the WDT counter

12.2.2.5 INTEN Register

WDT Interrupt register: Enable

OFFSET: 0x00000200

INSTANCE 0 ADDRESS: 0x40024200

Set bits in this register to allow this module to generate the corresponding interrupt.

Table 650: INTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															WDT

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 651: INTEN Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	This bitfield is reserved for future use.
0	WDT	0x0	RW	Watchdog Timer Interrupt.

12.2.2.6 INTSTAT Register

WDT Interrupt register: Status

OFFSET: 0x00000204

INSTANCE 0 ADDRESS: 0x40024204

Read bits from this register to discover the cause of a recent interrupt.

Table 652: INTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															WDT

Table 653: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	This bitfield is reserved for future use.
0	WDT	0x0	RW	Watchdog Timer Interrupt.

12.2.2.7 INTCLR Register

WDT Interrupt register: Clear

OFFSET: 0x00000208

INSTANCE 0 ADDRESS: 0x40024208

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 654: INTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															WDT

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 655: INTCLR Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	This bitfield is reserved for future use.
0	WDT	0x0	RW	Watchdog Timer Interrupt.

12.2.2.8 INTSET Register

WDT Interrupt register: Set

OFFSET: 0x0000020C

INSTANCE 0 ADDRESS: 0x4002420C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 656: INTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															WDT

Table 657: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	This bitfield is reserved for future use.
0	WDT	0x0	RW	Watchdog Timer Interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

13. Reset Generator Module

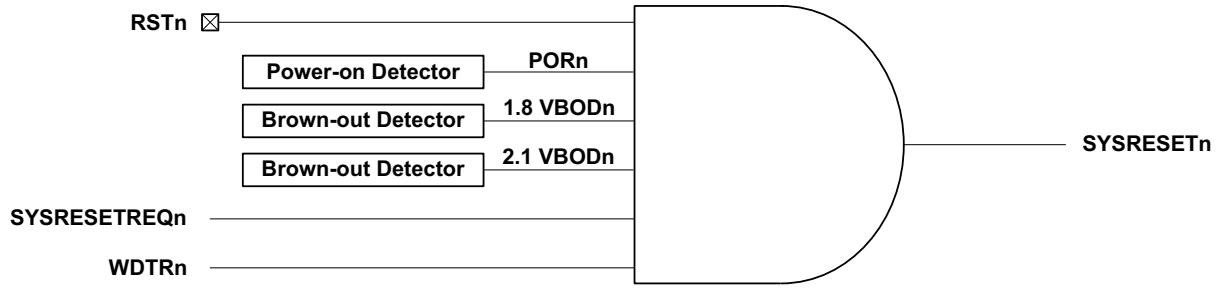


Figure 65. Block diagram for the Reset Generator Module

13.1 Functional Overview

The Reset Generator Module (RSTGEN) monitors a variety of reset signals and asserts the active low system reset (SYSRESETn) accordingly. A reset causes the entire system to be re-initialized, and the cause of the most recent reset is indicated by the STAT register.

Reset sources are described in the subsequent sections and include:

- External reset pin (RSTn)
- Power-on event
- Brown-out event
- Software request (SYSRESETREQn)
- Watchdog expiration

13.2 External Reset Pin

The active-low RSTn pin can be used to generate a reset using an off-chip component (e.g., a push-button). An internal pull-up resistor in the RSTn pad enables optional floating of the RSTn pin, and a de-bounce circuit ensures that bounce glitches on RSTn does not cause unintentional resets. The RSTn pin is not maskable. An internal pull-down device will be active during a brownout event pulling the RSTn pin low. See Figure 66..

©2017 Ambiq Micro, Inc.
All rights reserved.

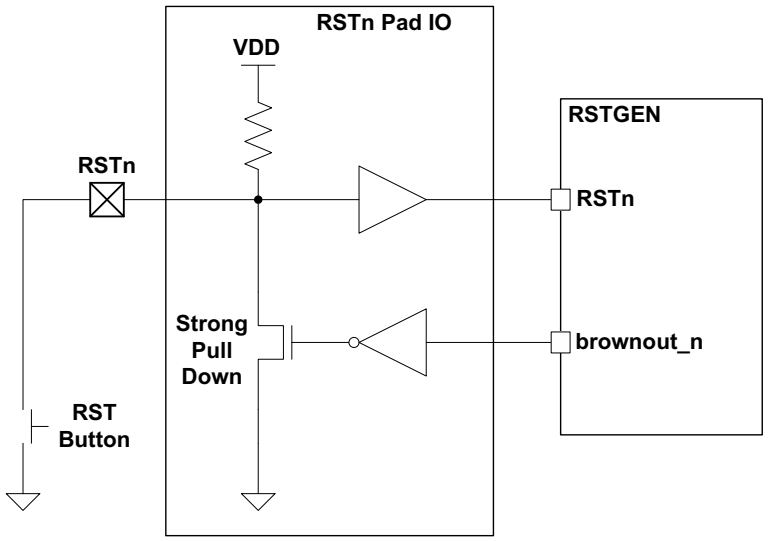


Figure 66. Block diagram of circuitry for Reset pin

13.3 Power-on Event

An integrated power-on detector monitors the supply voltage and keeps SYSRESETn asserted while VDD is below the rising power-on voltage, V_{POR+} (1.755 V). When VDD rises above V_{POR} at initial power on, the reset module will initialize the low power analog circuitry followed by de-assertion of SYSRESETn, and normal operation proceeds. SYSRESETn is re-asserted as soon as VDD falls below the falling power-on voltage, V_{POR-} (1.755 V). The power-on reset signal, PORn, is not maskable.

13.4 Brown-out Event

An integrated brown-out detector monitors the supply voltage and causes an automatic and non-configurable reset when the voltage has fallen below the 1.755 V threshold. An optional reset or interrupt can be enabled when the brown-out detector indicates the supply voltage has fallen below the 2.1 V threshold. In the event the supply voltage falls below the 1.755 V threshold, or 2.1 V threshold if enabled, the reset module will initiate a system reset, enabling the RSTn pull-down and driving the reset pin low. A 1.755 V or 2.1 V BOD reset will be reflected by the setting of the BORSTAT bit in the RSTGEN's STAT Register after reset.

13.5 Software Reset

A reset may be generated via software using the Application Interrupt and Reset Control Register (AIRCR) defined in the Cortex-M4. For additional information on the AIRCR, see the ARM document titled “Cortex-M4 Devices Generic User Guide.” The software reset request is not maskable. A second source for the identical software reset functionality is made available through the SWPOR register in the RSTGEN peripheral module.

©2017 Ambiq Micro, Inc.
All rights reserved.

13.6 Software Power On Initialization

The SWPOI register enables the capability for software to perform a substantial reset that includes reloading the low power analog circuitry trim settings set in the flash information space. These values are not re-loaded from flash info space for Software Reset or External Reset events.

13.7 Watchdog Expiration

The Watchdog Timer sub-module generates an interrupt if it has not been properly managed by software within a pre-defined time. The watchdog reset is maskable.

13.8 RSTGEN Registers

MCU Reset Generator

INSTANCE 0 BASE ADDRESS:0x40000000

13.8.1 Register Memory Map

Table 658: RSTGEN Register Map

Address(s)	Register Name	Description
0x40000000	CFG	Configuration Register
0x40000004	SWPOI	Software POI Reset
0x40000008	SWPOR	Software POR Reset
0x4000000C	STAT	Status Register
0x40000010	CLRSTAT	Clear the status register
0x40000014	TPIU_RST	TPIU reset
0x40000200	INTEN	Reset Interrupt register: Enable
0x40000204	INTSTAT	Reset Interrupt register: Status
0x40000208	INTCLR	Reset Interrupt register: Clear
0x4000020C	INTSET	Reset Interrupt register: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

13.8.2 RSTGEN Registers

13.8.2.1 CFG Register

Configuration Register

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x40000000

Configuration Register

Table 659: CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														WDREN	BODHREN

Table 660: CFG Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	RESERVED.
1	WDREN	0x0	RW	Watchdog Timer Reset Enable. NOTE: The WDT module must also be configured for WDT reset.
0	BODHREN	0x0	RW	Brown out high (2.1v) reset enable.

13.8.2.2 SWPOI Register

Software POI Reset

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x40000004

Software POI Reset

Table 661: SWPOI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								SWPOIKEY							

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 662: SWPOI Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	RESERVED.
7:0	SWPOIKEY	0x0	WO	0x1B generates a software POI reset. KEYVALUE = 0x1B - Writing 0x1B key value generates a software POI reset.

13.8.2.3 SWPOR Register

Software POR Reset

OFFSET: 0x00000008

INSTANCE 0 ADDRESS: 0x40000008

Software POR Reset

Table 663: SWPOR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								SWPORKEY							

Table 664: SWPOR Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	RESERVED.
7:0	SWPORKEY	0x0	WO	0xD4 generates a software POR reset. KEYVALUE = 0xD4 - Writing 0xD4 key value generates a software POR reset.

13.8.2.4 STAT Register

Status Register

OFFSET: 0x0000000C

INSTANCE 0 ADDRESS: 0x4000000C

Status Register

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 665: STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																									WDRSTAT	DBGRSTAT	POIRSTAT	SWRSTAT	BORSTAT	PORSTAT	EXRSTAT

Table 666: STAT Register Bits

Bit	Name	Reset	RW	Description
31:7	RSVD	0x0	RO	RESERVED.
6	WDRSTAT	0x0	RO	Reset was initiated by a Watchdog Timer Reset.
5	DBGRSTAT	0x0	RO	Reset was a initiated by Debugger Reset.
4	POIRSTAT	0x0	RO	Reset was a initiated by Software POI Reset.
3	SWRSTAT	0x0	RO	Reset was a initiated by SW POR or AIRCR Reset.
2	BORSTAT	0x0	RO	Reset was initiated by a Brown-Out Reset.
1	PORSTAT	0x0	RO	Reset was initiated by a Power-On Reset.
0	EXRSTAT	0x0	RO	Reset was initiated by an External Reset.

13.8.2.5 CLRSTAT Register

Clear the status register

OFFSET: 0x00000010

INSTANCE 0 ADDRESS: 0x40000010

Clear the status register

Table 667: CLRSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															CLRSTAT

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 668: CLRSTAT Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED.
0	CLRSTAT	0x0	WO	Writing a 1 to this bit clears all bits in the RST_STAT.

13.8.2.6 TPIU_RST Register

TPIU reset

OFFSET: 0x00000014

INSTANCE 0 ADDRESS: 0x40000014

TPIU reset

Table 669: TPIU_RST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															TPIURST

Table 670: TPIU_RST Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RW	RESERVED.
0	TPIURST	0x0	RW	Static reset for the TPIU. Write to '1' to assert reset to TPIU. Write to '0' to clear the reset.

13.8.2.7 INTEN Register

Reset Interrupt register: Enable

OFFSET: 0x00000200

INSTANCE 0 ADDRESS: 0x40000200

Set bits in this register to allow this module to generate the corresponding interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 671: INTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															BODH

Table 672: INTEN Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED.
0	BODH	0x0	RW	Enables an interrupt that triggers when VCC is below BODH level.

13.8.2.8 INTSTAT Register

Reset Interrupt register: Status

OFFSET: 0x00000204

INSTANCE 0 ADDRESS: 0x40000204

Read bits from this register to discover the cause of a recent interrupt.

Table 673: INTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															BODH

Table 674: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED.
0	BODH	0x0	RW	Enables an interrupt that triggers when VCC is below BODH level.

13.8.2.9 INTCLR Register

Reset Interrupt register: Clear

OFFSET: 0x00000208

INSTANCE 0 ADDRESS: 0x40000208

©2017 Ambiq Micro, Inc.
All rights reserved.

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 675: INTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															BODH

Table 676: INTCLR Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED.
0	BODH	0x0	RW	Enables an interrupt that triggers when VCC is below BODH level.

13.8.2.10INTSET Register

Reset Interrupt register: Set

OFFSET: 0x0000020C

INSTANCE 0 ADDRESS: 0x4000020C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 677: INTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															BODH

Table 678: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED.
0	BODH	0x0	RW	Enables an interrupt that triggers when VCC is below BODH level.

©2017 Ambiq Micro, Inc.
All rights reserved.

14. UART Module

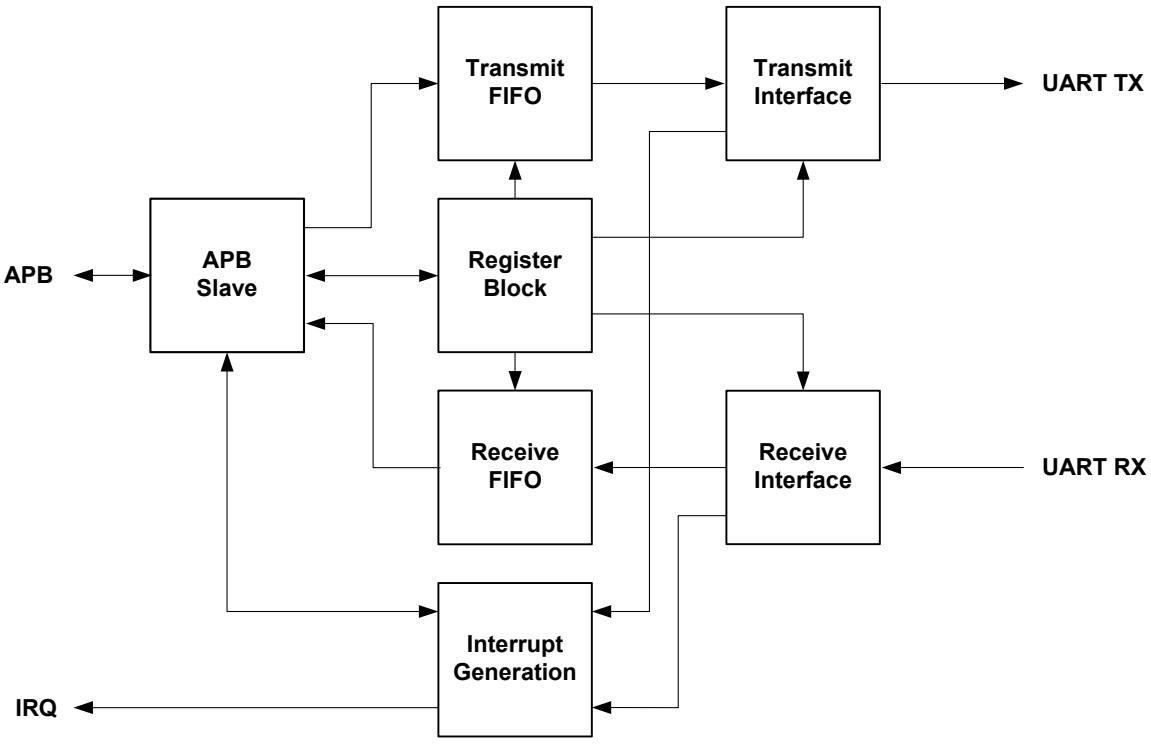


Figure 67. Block Diagram for the UART Module

14.1 Features

The UART Module includes the following key features:

- Operates independently, allowing the MCU to enter a low power sleep mode during communication
- 32 x 8 transmit FIFO and 32 x 12 receive FIFO to reduce MCU computational load
- Programmable baud rate generator capable of a maximum rate of 921,600 bits per second
- Fully programmable data size, parity, and stop bit length
- Programmable hardware flow control
- Support for full-duplex and half-duplex communication
- Loopback functionality for diagnostics and testing

14.2 Functional Overview

Shown in Figure 67, the UART Module converts parallel data written through the APB Slave port into serial data which is transmitted to an external device. It also receives serial data from an external device and converts it to parallel data, which is then stored in a buffer until the CPU reads the data.

The UART Module includes a programmable baud rate generator which is capable of operating at a maximum of 921,600 bits per second. An interrupt generator will optionally send interrupts to the CPU core for transmit, receive and error events.

Internally, the UART Module maintains two FIFOs. The transmit FIFO is 1-byte wide with 32 locations. The receive FIFO is 12-bits wide with 32 locations. The extra four bits in the receive FIFO are used to capture any error status information that the MCU needs to analyze.

©2017 Ambiq Micro, Inc.
All rights reserved.

Clocking to the UART serial logic is generated by a dedicated UARTCLK from the Clock Generator Module. The frequency of this clock is determined by the desired baud rate. For maximum baud rates, this clock would be clocked at the 24 MHz maximum as generated from the HFRC.

The major functional blocks of the UART are discussed briefly in the subsequent sections.

14.3 Enabling and Selecting the UART Clock

The UART module receives two clocks - UART_clk which is used to derive the UART serial clock and UART_hclk, which is the bus interface clock of the UART module. Unlike other Apollo2 Blue modules, the UART requires a bus clock whenever it is transmitting or receiving, so special controls are required when the UART is to transfer data while the Apollo2 Blue is in a sleep mode and its normal bus clocks are not operating.

UART_clk is selected in the UARTx_CR_CLKSEL field, with values from 24 MHz to 3 MHz plus a disabled value NOCLK, and is enabled by the UARTx_CR_CLKEN bit. If the UART is inactive, CLKSEL should be set to the NOCLK value (0) to minimize power, and the CLKEN bit should be 0. When the UART is active, the serial clock is created by the baud rate generator based on UART_clk. A higher UART_clk frequency can produce more precise serial clock frequencies, but will cause the UART to use more power. It is thus recommended that UART_clk be set to the minimum frequency which produces acceptable serial clocks.

When software is accessing the UART, UART_hclk must be equivalent to the Apollo2 Blue bus clock frequency of 48 MHz, but for transmit and receive purposes UART_hclk is only required to be at least as fast as UART_clk. It is thus possible to manage the frequency of UART_hclk to minimize power used by the UART. This is controlled by the CLK_GEN_UARTEN_UARTxEN fields, as defined in the table below.

UARTxEN	UART_hclk Function
0	Disable UART_hclk. Select this when the UART is inactive.
1	Force UART_hclk to 48MHz. This is not a recommended mode.
2	Force UART_hclk to match UART_clk. This mode may be used when the UART is actively transmitting or receiving, or is expected to receive a transmission. This minimizes power in the UART but does not allow software access to UART registers.
3	Automatic. In this mode, UART_hclk will be set to 48 MHz when Apollo2 Blue is awake and set to match UART_clk when Apollo2 Blue is in a sleep mode. This is a normal safe mode of operation.

In general, it is safe to leave the UARTxEN field at 3, which will minimize UART power in sleep modes but always allow UART register access. Power will be improved if UARTxEN is normally left at 2, and shifted to 3 whenever UART register access is required. Note that the UARTEN register is in the CLK_GEN module which always has bus access enabled.

14.4 Configuration

The UART Register Block in Figure 67 may be set to configure the UART Module. The data width, number of stop bits, and parity may all be configured using the UART_LCRH register.

The baud rate is configured using the integer UART_IBRD and UART_FBRD registers. The correct values for UART_IBRD and UART_FBRD may be determined according to the following equation:

$F_{UART}/(16 \cdot BR) = IBRD + FBRD$

F_{UART} is the frequency of the UART clock. BR is the desired baud rate. IBRD is the integer portion of the baud rate divisor. FBRD is the fractional portion of the baud rate divisor.

©2017 Ambiq Micro, Inc.
All rights reserved.

The UART Module supports independent CTS and RTS hardware flow control. All flow control configuration may be set using the UART_CR register.

14.5 Transmit FIFO and Receive FIFO

The transmit and receive FIFOs may both be accessed via the same 8-bit word in the UART_DR register. The transmit FIFO stores up to 32 8-bit words and can be written using writes to UART_DR. The receive FIFO stores up to 32 12-bit words and can be read using reads to UART_DR. Note that each 12-bit receive FIFO word includes an 8-bit data word and a 4-bit error status word.

14.6 UART Registers

Serial UART

INSTANCE 0 BASE ADDRESS:0x4001C000

INSTANCE 1 BASE ADDRESS:0x4001D000

14.6.1 Register Memory Map

Table 679: UART Register Map

Address(s)	Register Name	Description
0x4001C000 0x4001D000	DR	UART Data Register
0x4001C004 0x4001D004	RSR	UART Status Register
0x4001C018 0x4001D018	FR	Flag Register
0x4001C020 0x4001D020	ILPR	IrDA Counter
0x4001C024 0x4001D024	IBRD	Integer Baud Rate Divisor
0x4001C028 0x4001D028	FBRD	Fractional Baud Rate Divisor
0x4001C02C 0x4001D02C	LCRH	Line Control High
0x4001C030 0x4001D030	CR	Control Register
0x4001C034 0x4001D034	IFLS	FIFO Interrupt Level Select
0x4001C038 0x4001D038	IER	Interrupt Enable
0x4001C03C 0x4001D03C	IES	Interrupt Status
0x4001C040 0x4001D040	MIS	Masked Interrupt Status
0x4001C044 0x4001D044	IEC	Interrupt Clear

©2017 Ambiq Micro, Inc.
All rights reserved.

14.6.2 UART Registers

14.6.2.1 DR Register

UART Data Register

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x4001C000

INSTANCE 1 ADDRESS: 0x4001D000

UART Data Register

Table 680: DR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																				OEDATA	BEDATA	PEDATA	FEDATA	DATA								

Table 681: DR Register Bits

Bit	Name	Reset	RW	Description
31:12	RSVD	0x0	RO	This bitfield is reserved for future use.
11	OEDATA	0x0	RO	This is the overrun error indicator. NOERR = 0x0 - No error on UART OEDATA, overrun error indicator. ERR = 0x1 - Error on UART OEDATA, overrun error indicator.
10	BEDATA	0x0	RO	This is the break error indicator. NOERR = 0x0 - No error on UART BEDATA, break error indicator. ERR = 0x1 - Error on UART BEDATA, break error indicator.
9	PEDATA	0x0	RO	This is the parity error indicator. NOERR = 0x0 - No error on UART PEDATA, parity error indicator. ERR = 0x1 - Error on UART PEDATA, parity error indicator.
8	FEDATA	0x0	RO	This is the framing error indicator. NOERR = 0x0 - No error on UART FEDATA, framing error indicator. ERR = 0x1 - Error on UART FEDATA, framing error indicator.
7:0	DATA	0x0	RW	This is the UART data port.

14.6.2.2 RSR Register

UART Status Register

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x4001C004

©2017 Ambiq Micro, Inc.
All rights reserved.

INSTANCE 1 ADDRESS: 0x4001D004

UART Status Register

Table 682: RSR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																												OESTAT	BESTAT	PESTAT	FESTAT

Table 683: RSR Register Bits

Bit	Name	Reset	RW	Description
31:4	RSVD	0x0	RO	This bitfield is reserved for future use.
3	OESTAT	0x0	RW	This is the overrun error indicator. NOERR = 0x0 - No error on UART OESTAT, overrun error indicator. ERR = 0x1 - Error on UART OESTAT, overrun error indicator.
2	BESTAT	0x0	RW	This is the break error indicator. NOERR = 0x0 - No error on UART BESTAT, break error indicator. ERR = 0x1 - Error on UART BESTAT, break error indicator.
1	PESTAT	0x0	RW	This is the parity error indicator. NOERR = 0x0 - No error on UART PESTAT, parity error indicator. ERR = 0x1 - Error on UART PESTAT, parity error indicator.
0	FESTAT	0x0	RW	This is the framing error indicator. NOERR = 0x0 - No error on UART FESTAT, framing error indicator. ERR = 0x1 - Error on UART FESTAT, framing error indicator.

14.6.2.3 FR Register

Flag Register

OFFSET: 0x00000018

INSTANCE 0 ADDRESS: 0x4001C018

INSTANCE 1 ADDRESS: 0x4001D018

Flag Register

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 684: FR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																							TXBUSY	TXFE	RXFF	TXFF	RXFE	BUSY	DCD	DSR	CTS

Table 685: FR Register Bits

Bit	Name	Reset	RW	Description
31:9	RSVD	0x0	RO	This bitfield is reserved for future use.
8	TXBUSY	0x0	RO	This bit holds the transmit BUSY indicator.
7	TXFE	0x0	RO	This bit holds the transmit FIFO empty indicator. XMTFIFO_EMPTY = 0x1 - Transmit fifo is empty.
6	RXFF	0x0	RO	This bit holds the receive FIFO full indicator. RCVFIFO_FULL = 0x1 - Receive fifo is full.
5	TXFF	0x0	RO	This bit holds the transmit FIFO full indicator. XMTFIFO_FULL = 0x1 - Transmit fifo is full.
4	RXFE	0x0	RO	This bit holds the receive FIFO empty indicator. RCVFIFO_EMPTY = 0x1 - Receive fifo is empty.
3	BUSY	0x0	RO	This bit holds the busy indicator. BUSY = 0x1 - UART busy indicator.
2	DCD	0x0	RO	This bit holds the data carrier detect indicator. DETECTED = 0x1 - Data carrier detect detected.
1	DSR	0x0	RO	This bit holds the data set ready indicator. READY = 0x1 - Data set ready.
0	CTS	0x0	RO	This bit holds the clear to send indicator. CLEARTOSEND = 0x1 - Clear to send is indicated.

14.6.2.4 ILPR Register

IrDA Counter

OFFSET: 0x00000020

INSTANCE 0 ADDRESS: 0x4001C020

INSTANCE 1 ADDRESS: 0x4001D020

IrDA Counter

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 686: ILPR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								ILPDVSR							

Table 687: ILPR Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	This bitfield is reserved for future use.
7:0	ILPDVSR	0x0	RW	These bits hold the IrDA counter divisor.

14.6.2.5 IBRD Register

Integer Baud Rate Divisor

OFFSET: 0x00000024

INSTANCE 0 ADDRESS: 0x4001C024

INSTANCE 1 ADDRESS: 0x4001D024

Integer Baud Rate Divisor

Table 688: IBRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																DIVINT															

Table 689: IBRD Register Bits

Bit	Name	Reset	RW	Description
31:16	RSVD	0x0	RO	This bitfield is reserved for future use.
15:0	DIVINT	0x0	RW	These bits hold the baud integer divisor.

14.6.2.6 FBRD Register

Fractional Baud Rate Divisor

OFFSET: 0x00000028

INSTANCE 0 ADDRESS: 0x4001C028

INSTANCE 1 ADDRESS: 0x4001D028

©2017 Ambiq Micro, Inc.
All rights reserved.

Fractional Baud Rate Divisor

Table 690: FBRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										DIVFRAC					

Table 691: FBRD Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	This bitfield is reserved for future use.
5:0	DIVFRAC	0x0	RW	These bits hold the baud fractional divisor.

14.6.2.7 LCRH Register

Line Control High

OFFSET: 0x0000002C

INSTANCE 0 ADDRESS: 0x4001C02C

INSTANCE 1 ADDRESS: 0x4001D02C

Line Control High

Table 692: LCRH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								SPS	WLEN		FEN	STP2	EPS	PEN	BRK

Table 693: LCRH Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	This bitfield is reserved for future use.
7	SPS	0x0	RW	This bit holds the stick parity select.
6:5	WLEN	0x0	RW	These bits hold the write length.
4	FEN	0x0	RW	This bit holds the FIFO enable.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 693: LCRH Register Bits

Bit	Name	Reset	RW	Description
3	STP2	0x0	RW	This bit holds the two stop bits select.
2	EPS	0x0	RW	This bit holds the even parity select.
1	PEN	0x0	RW	This bit holds the parity enable.
0	BRK	0x0	RW	This bit holds the break set.

14.6.2.8 CR Register

Control Register

OFFSET: 0x00000030

INSTANCE 0 ADDRESS: 0x4001C030

INSTANCE 1 ADDRESS: 0x4001D030

Control Register

Table 694: CR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																CTSEN	RTSEN	OUT2	OUT1	RTS	DTR	RXE	TXE	LBE	CLKSEL			CLKEN	SIRLP	SIREN	UARTEN

Table 695: CR Register Bits

Bit	Name	Reset	RW	Description
31:16	RSVD	0x0	RO	This bitfield is reserved for future use.
15	CTSEN	0x0	RW	This bit enables CTS hardware flow control.
14	RTSEN	0x0	RW	This bit enables RTS hardware flow control.
13	OUT2	0x0	RW	This bit holds modem Out2.
12	OUT1	0x0	RW	This bit holds modem Out1.
11	RTS	0x0	RW	This bit enables request to send.
10	DTR	0x0	RW	This bit enables data transmit ready.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 695: CR Register Bits

Bit	Name	Reset	RW	Description
9	RXE	0x1	RW	This bit is the receive enable.
8	TXE	0x1	RW	This bit is the transmit enable.
7	LBE	0x0	RW	This bit is the loopback enable.
6:4	CLKSEL	0x0	RW	This bitfield is the UART clock select. NOCLK = 0x0 - No UART clock. This is the low power default. 24MHZ = 0x1 - 24 MHz clock. 12MHZ = 0x2 - 12 MHz clock. 6MHZ = 0x3 - 6 MHz clock. 3MHZ = 0x4 - 3 MHz clock. RSVD5 = 0x5 - Reserved. RSVD6 = 0x6 - Reserved. RSVD7 = 0x7 - Reserved.
3	CLKEN	0x0	RW	This bit is the UART clock enable.
2	SIRLP	0x0	RW	This bit is the SIR low power select.
1	SIREN	0x0	RW	This bit is the SIR ENDEC enable.
0	UARTEN	0x0	RW	This bit is the UART enable.

14.6.2.9 IFLS Register

FIFO Interrupt Level Select

OFFSET: 0x00000034

INSTANCE 0 ADDRESS: 0x4001C034

INSTANCE 1 ADDRESS: 0x4001D034

FIFO Interrupt Level Select

Table 696: IFLS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										RXIFLSEL			TXIFLSEL		

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 697: IFLS Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	This bitfield is reserved for future use.
5:3	RXIFLSEL	0x2	RW	These bits hold the receive FIFO interrupt level.
2:0	TXIFLSEL	0x2	RW	These bits hold the transmit FIFO interrupt level.

14.6.2.10IER Register

Interrupt Enable

OFFSET: 0x00000038

INSTANCE 0 ADDRESS: 0x4001C038

INSTANCE 1 ADDRESS: 0x4001D038

Interrupt Enable

Table 698: IER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					OEIM	BEIM	PEIM	FEIM	RTIM	TXIM	RXIM	DSRMIM	DCDMIM	CTSMIM	TXCMPMIM

Table 699: IER Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	This bitfield is reserved for future use.
10	OEIM	0x0	RW	This bit holds the overflow interrupt enable.
9	BEIM	0x0	RW	This bit holds the break error interrupt enable.
8	PEIM	0x0	RW	This bit holds the parity error interrupt enable.
7	FEIM	0x0	RW	This bit holds the framing error interrupt enable.
6	RTIM	0x0	RW	This bit holds the receive timeout interrupt enable.
5	TXIM	0x0	RW	This bit holds the transmit interrupt enable.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 699: IER Register Bits

Bit	Name	Reset	RW	Description
4	RXIM	0x0	RW	This bit holds the receive interrupt enable.
3	DSRMIM	0x0	RW	This bit holds the modem DSR interrupt enable.
2	DCDMIM	0x0	RW	This bit holds the modem DCD interrupt enable.
1	CTSMIM	0x0	RW	This bit holds the modem CTS interrupt enable.
0	TXCMPMIM	0x0	RW	This bit holds the modem TXCMP interrupt enable.

14.6.2.11IES Register

Interrupt Status

OFFSET: 0x0000003C

INSTANCE 0 ADDRESS: 0x4001C03C

INSTANCE 1 ADDRESS: 0x4001D03C

Interrupt Status

Table 700: IES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					OERIS	BERIS	PERIS	FERIS	RTRIS	TXRIS	RXRIS	DSRMRIS	DCDMRIS	CTSMRIS	TXCMPMRIS

Table 701: IES Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	This bitfield is reserved for future use.
10	OERIS	0x0	RO	This bit holds the overflow interrupt status.
9	BERIS	0x0	RO	This bit holds the break error interrupt status.
8	PERIS	0x0	RO	This bit holds the parity error interrupt status.
7	FERIS	0x0	RO	This bit holds the framing error interrupt status.
6	RTRIS	0x0	RO	This bit holds the receive timeout interrupt status.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 701: IES Register Bits

Bit	Name	Reset	RW	Description
5	TXRIS	0x0	RO	This bit holds the transmit interrupt status.
4	RXRIS	0x0	RO	This bit holds the receive interrupt status.
3	DSRMRIS	0x0	RO	This bit holds the modem DSR interrupt status.
2	DCDMRIS	0x0	RO	This bit holds the modem DCD interrupt status.
1	CTSMRIS	0x0	RO	This bit holds the modem CTS interrupt status.
0	TXCMPMRIS	0x0	RO	This bit holds the modem TXCMP interrupt status.

14.6.2.12MIS Register

Masked Interrupt Status

OFFSET: 0x00000040

INSTANCE 0 ADDRESS: 0x4001C040

INSTANCE 1 ADDRESS: 0x4001D040

Masked Interrupt Status

Table 702: MIS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					OEMIS	BEMIS	PEMIS	FEMIS	RTMIS	TXMIS	RXMIS	DSRMMIS	DCDMMIS	CTSMMIS	TXCMPMMIS

Table 703: MIS Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	This bitfield is reserved for future use.
10	OEMIS	0x0	RO	This bit holds the overflow interrupt status masked.
9	BEMIS	0x0	RO	This bit holds the break error interrupt status masked.
8	PEMIS	0x0	RO	This bit holds the parity error interrupt status masked.
7	FEMIS	0x0	RO	This bit holds the framing error interrupt status masked.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 703: MIS Register Bits

Bit	Name	Reset	RW	Description
6	RTMIS	0x0	RO	This bit holds the receive timeout interrupt status masked.
5	TXMIS	0x0	RO	This bit holds the transmit interrupt status masked.
4	RXMIS	0x0	RO	This bit holds the receive interrupt status masked.
3	DSRMMIS	0x0	RO	This bit holds the modem DSR interrupt status masked.
2	DCDMMIS	0x0	RO	This bit holds the modem DCD interrupt status masked.
1	CTSMMIS	0x0	RO	This bit holds the modem CTS interrupt status masked.
0	TXCMPMMIS	0x0	RO	This bit holds the modem TXCMP interrupt status masked.

14.6.2.13IEC Register

Interrupt Clear

OFFSET: 0x00000044

INSTANCE 0 ADDRESS: 0x4001C044

INSTANCE 1 ADDRESS: 0x4001D044

Interrupt Clear

Table 704: IEC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																					OEIC	BEIC	PEIC	FEIC	RTIC	TXIC	RXIC	DSRMIC	DCDMIC	CTSMIC	TXCMPMIC

Table 705: IEC Register Bits

Bit	Name	Reset	RW	Description
31:11	RSVD	0x0	RO	This bitfield is reserved for future use.
10	OEIC	0x0	WO	This bit holds the overflow interrupt clear.
9	BEIC	0x0	WO	This bit holds the break error interrupt clear.
8	PEIC	0x0	WO	This bit holds the parity error interrupt clear.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 705: IEC Register Bits

Bit	Name	Reset	RW	Description
7	FEIC	0x0	WO	This bit holds the framing error interrupt clear.
6	RTIC	0x0	WO	This bit holds the receive timeout interrupt clear.
5	TXIC	0x0	WO	This bit holds the transmit interrupt clear.
4	RXIC	0x0	WO	This bit holds the receive interrupt clear.
3	DSRMIC	0x0	WO	This bit holds the modem DSR interrupt clear.
2	DCDMIC	0x0	WO	This bit holds the modem DCD interrupt clear.
1	CTSMIC	0x0	WO	This bit holds the modem CTS interrupt clear.
0	TXCMPMIC	0x0	WO	This bit holds the modem TXCMP interrupt clear.

©2017 Ambiq Micro, Inc.
All rights reserved.

15. ADC and Temperature Sensor Module

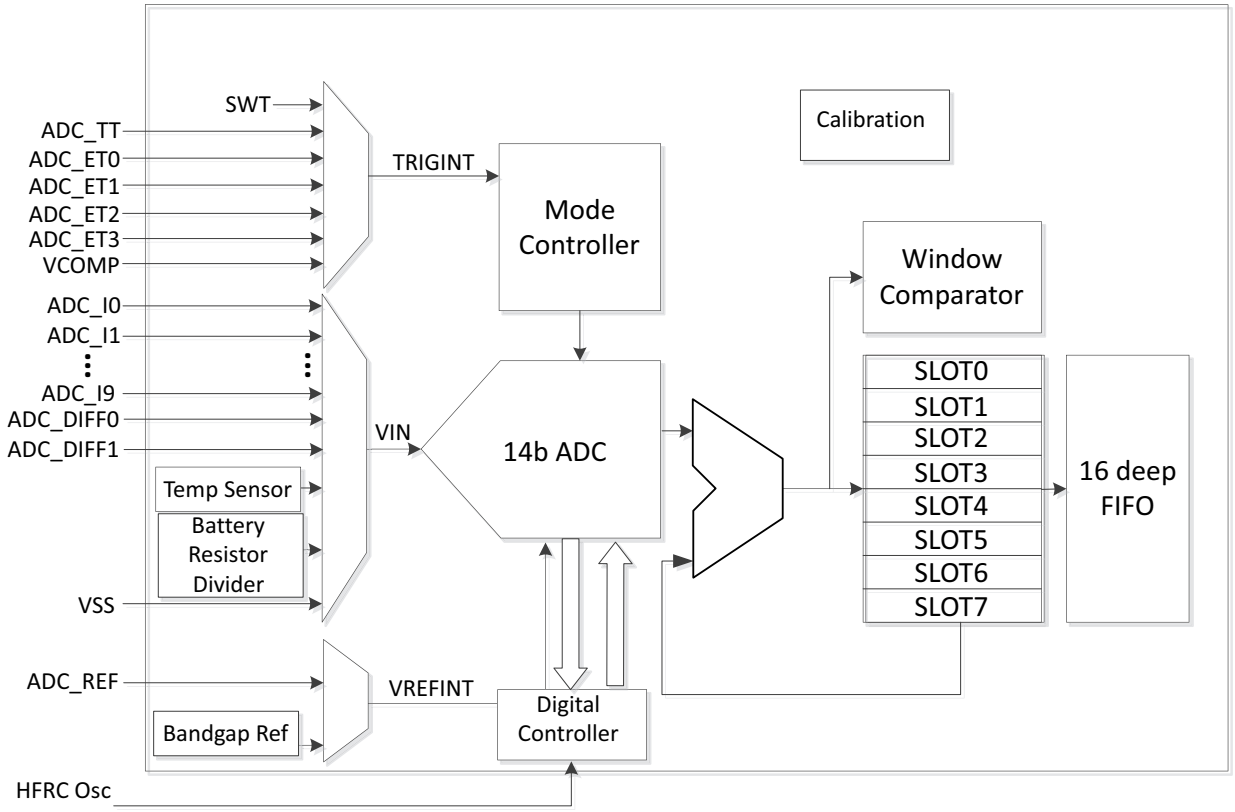


Figure 68. Block Diagram for ADC and Temperature Sensor

15.1 Features

The Analog to Digital Converter (ADC) and Temperature Sensor Module includes a 14 bit multi-channel Successive Approximation Register (SAR) ADC as shown in Figure 68.

Key features include:

- 11 user-selectable channels with sources including:
  - External pins
    - single ended
    - 2 differential pairs
  - Internal voltage (VSS)
  - Voltage divider (battery)
  - Temperature sensor
- Configurable automatic low power control between scans
- Optional Battery load enable for voltage divider measurement
- Configurable for 14 / 12 / 10 / 8 bit ADC Precision Modes
- User-selectable on-chip and off-chip reference voltages
- Single shot, repeating single shot, scan, and repeating scan modes
- User-selectable clock source for variable sampling rates
- Automatically accumulate and scale module for hardware averaging of samples
- A 16-entry FIFO for storing measurement results and maximizing MCU sleep time

©2017 Ambiq Micro, Inc.
All rights reserved.

- Window comparator for monitoring voltages excursions into or out of user-selectable thresholds
- Up to 2.67 MS/s effective continuous, multi-slot sampling rate
- Interrupts for FIFO full, FIFO almost full, Scan Complete, Conversion Complete, Window Incursion Window Excursion

15.2 Functional Overview

The Apollo2 Blue integrates a sophisticated 14 bit successive approximation Analog to Digital Converter (ADC) block for sensing both internal and external voltages. The block provides eight separately managed conversion requests, called slots. The result of each conversion requests is delivered to a 16 deep FIFO. Firmware can utilize various interrupt notifications to determine when to collect the sampled data from the FIFO. This block is extremely effective at automatically managing its power states and its clock sources.

15.2.1 Clock Source and Dividers

The ADC runs off of the HFRC clock source. When the ADC block is enabled and has an active scan in progress, it requests an HFRC clock source. There is an automatic hardware hand shake between the clock generator and the ADC. If the ADC is the only block requesting an HFRC based clock, then the HFRC will be automatically started. The ADC can be configured to completely power down the HFRC between scans if the startup latency is acceptable or it can leave the HFRC powered on between scans if THE application requires low latency between successive conversions. The ADC supports 2 clock frequency modes: 24MHz and 48MHz HFRC. 48MHz mode is the default mode of operation.

15.2.2 15 Channel Analog Mux

As shown in Figure 68, the ADC block contains a 15 channel analog multiplexer on the input port to the analog to digital converter. Twelve (12) of the GPIO pins on the Apollo2 Blue can be selected as analog inputs to the ADC through a combination of settings in the PAD configuration registers in the GPIO block and settings in the configuration registers described below.

The analog mux channels are connected as follows:

1. ADC_EXT0 external GPIO pin connection.
2. ADC_EXT1 external GPIO pin connection.
3. ADC_EXT2 external GPIO pin connection.
4. ADC_EXT7 external GPIO pin connection.
5. ADC_EXT8 external GPIO pin connection.
6. ADC_EXT9 external GPIO pin connection.
7. ADC_EXT_DIFF0P external GPIO connection (muxed with EXT8)

   ADC_EXT_DIFF0N external GPIO connection (muxed with EXT9)
8. ADC_EXT6 ADC_EXT DIFF1N external GPIO pin connection.

   ADC_EXT7 ADC_EXTDIFF1P external GPIO pin connection.
9. ADC_TEMP internal temperature sensor.
10. ADC_DIV3 internal voltage divide by 3 connection to the input power rail.
11. ADC_VSS internal ground connection.

EXT8-9 can be configured as a differential pair providing an additional differential pair or up to 2 single-ended inputs from GPIO.

Refer to the detailed register information below for the exact coding of the channel selection bit field. Also the use of the voltage divider and switchable load resistor are detailed below.

©2017 Ambiq Micro, Inc.
All rights reserved.

15.2.3 Triggering and Trigger Sources

The ADC block can be initially triggered from one of four sources. Once triggered, it can be repetitively triggered from counter/timer number three (3). Four of the GPIO pins on the Apollo2 Blue can be selected as trigger inputs to the ADC through a combination of settings in the PAD configuration registers in the GPIO block and settings in SLOT configuration registers described below. In addition, there is a software trigger and a vcomp trigger source. The trigger sources are as follows:

0. ADC_EXT0 (TRIG0) external GPIO pin connection.
1. ADC_EXT1 (TRIG1) external GPIO pin connection.
2. VCOMP Voltage Comparator trigger.
3. <Reserved>
4. <Reserved>
5. ADC_SWT software trigger.

Refer to the ADC Configuration Register in the detailed register information section below. The initial trigger source is selected in the TRIGSEL field, as shown below. In addition, one can select a trigger polarity in this register applicable for any of the trigger sources except the software trigger. A number of GPIO pin trigger sources are provided to allow pin configuration flexibility at the system definition and board layout phases of development.

The software trigger is effected by writing 0x37 to the software trigger register in the ADC block. Note that writing 0x37 to the software trigger register will initiate a scan regardless of which trigger source is selected. However, a hardware trigger source will not initiate a scan if the software trigger has been selected.

When the ADC is configured for repeat mode, the initial trigger must be initiated by a software trigger and subsequent scans will be initiated at a repeating rate set by the counter/timer3 configuration. The discussion of the use of counter/timer three as a source for repetitive triggering is deferred until later in this chapter.

Finally it is important to note that a trigger event applies to all enabled slots as a whole. Individual slots can not be separately triggered.

15.2.4 Voltage Reference Sources

The Apollo2 Blue ADC allows one of two reference sources, each with two different voltage options to be used for the analog to digital conversion step:

- Internal 2.0V reference source
- Internal 1.5V reference source
- External 2.0V reference source
- External 1.5V reference source

15.2.5 Eight Automatically Managed Conversion Slots

The ADC block contains eight conversion slot control registers, one for each of the eight slots. These can be thought of as time slots in the conversion process. When a slot is enabled, it participates in a conversion cycle. The ADC's mode controller cycles through up to eight time slots each time it is triggered. For each slot that is enabled, a conversion cycle is performed based on the settings in the slot configuration register for that slot. Slots are enabled when the LSB of the slot configuration is set to one.
See "One SLOT Configuration Register" on page 451.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 706: One SLOT Configuration Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved					# Samples to Accum.			Reserved												CHANNEL SELECT				Reserved						WINDOW_COMP	SLOT_ENABLE

The window comparator enable will be discussed in a subsequent section, below. See “Window Comparator” on page 455. The number of samples to accumulate will also be explained in a subsequent section. See “Automatic Sample Accumulation and Scaling” on page 451.

As described above, the channel select bit field specifies which one of the analog multiplexer channels will be used for the conversions requested for an individual slot. See “15 Channel Analog Mux” on page 449.

Each of the eight conversion slots can independently specify:

- Analog Multiplexer Channel Selection
- Participation in Window Comparisons
- Automatic Sample Accumulation

15.2.6 Automatic Sample Accumulation and Scaling

The ADC block offers a facility for the automatic accumulation of samples without requiring core involvement. Thus up to 128 samples per slot can be accumulated without waking the core. This facilitates averaging algorithms to smooth out the data samples. Each slot can request from 1 to 128 samples to be accumulated before producing a result in the FIFO. **NOTE:** each slot can independently specify how many samples to accumulate so results can enter the FIFO from different slots at different rates.

All slots write their accumulated results to the FIFO in exactly the same format regardless of how many samples were accumulated to produce the results. shows the format that is used by all conversions. This is a scaled integer format with a 6-bit fractional part. The precision mode for each determines the format for the FIFO data. 14-bit, 12-bit, 10-bit and 8-bit precision modes respectively correspond to 14.6, 12.6, 10.6 and 8.6 formats.

IMPORTANT: if the accumulation control for a slot is set for one sample with 14-bit precision, then the 14-bit value coming from the ADC will be inserted into bits 6 through 19 in this format and the lower 6 bits are zero'd. If the accumulation control for a slot is set for two samples with 8-bit precision, then the 8-bit average integer value will be placed in bits 6 through 13, the 1 bit fractional number is placed in bit 5 and the lower 5 fractional bits are zero'd..

Table 707: 10.6 ADC Sample Format

19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
14-bit Integer														6-bit Fraction					

Each slot contains a 21-bit accumulator as shown in Table 708, “Per Slot Sample Accumulator,” on page 452. When the ADC is triggered for the last sample of an accumulation, the accumulator is cleared

©2017 Ambiq Micro, Inc.
All rights reserved.

and the FIFO will be written with the final average value. When each active slot obtains a sample from the ADC, it is added to the value in its accumulator.

If a slot is set to accumulate 128 samples per result then the accumulator could reach a maximum value of:

$128*(2^{14}-1) = 128*16383 = 2097024 = 2^{21} - 128$, hence the 21 bit accumulator.

Table 708: Per Slot Sample Accumulator

20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Accumulator																				

Table 709 shows the maximum possible accumulated values. Note that 64 sample accumulation produces a result that is exactly correct or the 14.6 format results so it is copied unscaled in to the FIFO.

Furthermore, note that 128 sample accumulation can produce a result that is too large for the 14.6 format since it may result in 7 bits of valid fractional data. All of the remaining sample accumulation settings must have their results left shifted to produce the desired 14.6 format.

Finally, note that for the 128 sample accumulation case, the LSB of the accumulator is discarded when the results are written to the FIFO.

Most importantly, note that for the 1 sample accumulation case, the 14-bit converter value is shifted left by six to produce the 14.6 format to write into the FIFO.

Table 709: Accumulator Scaling

# Samples	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
128	14.6																				0
64	X	14.6																			
32	X	X	14.5																		
16	X	X	X	14.4																	
8	X	X	X	X	14.3																
4	X	X	X	X	X	14.2															
2	X	X	X	X	X	X	14.1														
1	X	X	X	X	X	X	X	14													

15.2.7 Sixteen Entry Result FIFO

All results written to the FIFO have exactly the same format as shown in Table 710. The properly scaled accumulation results are written the lower half word in the aforementioned 14.6 format. Since each slot can

©2017 Ambiq Micro, Inc.
All rights reserved.

produce results at a different rate, the slot number generating the result is also written to the FIFO along with the total valid entry count within the FIFO.

Table 710: FIFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSV	Slot Number.											FIFO Count																			
												FIFO DATA																			

Table 711: 14-bit FIFO Data Format

# Samples	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
128	14.6																			
64	14.6																			
32	14.5																			X
16	14.4																		X	X
8	14.3																	X	X	X
4	14.2																X	X	X	X
2	14.1															X	X	X	X	X
1	14														X	X	X	X	X	X

Table 712: 12-bit FIFO Data Format

# Samples	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
128	0	0	12.6																	
64	0	0	12.6																	
32	0	0	12.5																	X
16	0	0	12.4																X	X
8	0	0	12.3															X	X	X
4	0	0	12.2														X	X	X	X
2	0	0	12.1													X	X	X	X	X
1	0	0	12												X	X	X	X	X	X

Table 713: 10-bit FIFO Data Format

# Samples	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
128	0	0	0	0	10										6					

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 713: 10-bit FIFO Data Format

# Samples	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
64	0	0	0	0	10										6					
32	0	0	0	0	10										5					X
16	0	0	0	0	10										4				X	X
8	0	0	0	0	10										3			X	X	X
4	0	0	0	0	10										2		X	X	X	X
2	0	0	0	0	10										1	X	X	X	X	X
1	0	0	0	0	10										X	X	X	X	X	X

Table 714: 8-bit FIFO Data Format

# Samples	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
128	0	0	0	0	0	0	8.6													
64	0	0	0	0	0	0	8.6													
32	0	0	0	0	0	0	8.5													X
16	0	0	0	0	0	0	8.4												X	X
8	0	0	0	0	0	0	8.3											X	X	X
4	0	0	0	0	0	0	8.2										X	X	X	X
2	0	0	0	0	0	0	8.1									X	X	X	X	X
1	0	0	0	0	0	0	8								X	X	X	X	X	X

Software accesses the contents of the FIFO through the ADCFIFO register. This register will be written by the ADC digital controller simultaneous with the conversion complete interrupt (if enabled) after accumulating the number of samples to average configured for the slot. The ADCFIFO register contains the earliest written data, the number of valid entries within the FIFO and the slot number associated with the FIFO data. Thus the interrupt handler servicing ADC interrupts can easily distribute results to different RTOS tasks by simply looking up the target task using the slot number from the FIFO register.

Three other features greatly simplify the task faced by firmware developers of interrupt service routines for the ADC block:

1. The FIFO count bit field is not really stored in the FIFO. Instead it is a live count of the number of valid entries currently residing in the FIFO. If the interrupt service routine was entered because of a conversion then this value will be at least one. When the interrupts routine is entered it can pull successive sample values from the FIFO until this bit field goes to zero. Thus avoiding wasteful re-entry of the interrupt service routine. Note that no further I/O bus read is required to determine the FIFO depth.
2. This FIFO has no read side effects. This is important to firmware for a number of reasons. One important result is that the FIFO register can be freely read repetitively by a debugger without affecting the state of the FIFO. In order to pop this FIFO and look at the next result, if any, one simply writes any value to this register. Any time the FIFO is read, then the compiler has gone to the trouble of generating an address for the read. To pop the FIFO, one simply writes to that same address with any value. This give firmware a positive handshake mechanism to control exactly when the FIFO pops.
3. When a conversion completes resulting in hardware populating the 12th valid FIFO entry, the FIFOOVR1 (FIFO 75% full) interrupt status bit will be set. When a conversion completes resulting in

©2017 Ambiq Micro, Inc.
All rights reserved.

hardware populating the 8th valid FIFO entry, the FIFOOVR2 interrupt status bit will be set. In a FIFO full condition with 16 valid entries, the ADC will not overwrite existing valid FIFO contents. Before subsequent conversions will populate the FIFO with conversion data, software must free an open FIFO entry by writing to the FIFO Register or by resetting the ADC by disabling and enabling the ADC using the ADC_CFG register.

15.2.8 Window Comparator

A window comparator is provided which can generate an interrupt whenever a sample is determined to be inside the window limits or outside the window limits. These are two separate interrupts with separate interrupt enables. Thus one can request an interrupt any time a specified slot makes an excursion outside the window comparator limits.

The window comparison function has an option for comparing the contents of the limits registers directly with the FIFO data (default) or for scaling the limits register depending on the precision mode selected for the slots.

Firmware has to participate in the determination of whether an actual excursion occurred. The window comparator interrupts set their corresponding interrupt status bits continuously whenever the inside or outside condition is true. Thus if one enables and receives an "*excursion*" interrupt then the status bit can't be usefully cleared while the ADC slot is sampling values outside the limits. That is, if one receives an excursion interrupt and clears the status bit, it will immediately set again if the next ADC sample is still outside the limits. Thus firmware should reconfigure the interrupt enables upon receiving an excursion interrupt so that the next interrupt will occur when an ADC sample ultimately goes back inside the window limits. Firmware may also want to change the windows comparator limit at that time to utilize a little hysteresis in these window comparator decisions.

Table 715: Window Comparator Lower Limit Register

19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Lower Limit																			

Table 716: Window Comparator Upper Limit Register

19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Upper Limit																			

The determination of whether a sample is *inside* or *outside* of the window limits is made by comparing the data format of the slot result written to the FIFO with the 20 bit window limits. An ADC sample is inside if the following relation is true:

14.6 Lower Limit <= ADC SAMPLE <= 14.6 Upper Limit

Thus setting both limits to the same value, say 700.0 (0x2BC<<6 = 0xAF00), will only produce an inside interrupt when the ADC sample is exactly 700.0 (0xAF00). Furthermore, note that if the lower limit is set to zero (0x00000) and the upper limit is set to 0xFFFFF then all accumulated results from the ADC will be inside the window limits and no excursion interrupts can ever by generated. In fact, in this case, the incursion interrupt status bit will be set for every sample from any active slot with its window comparator bit enabled. If the incursion interrupt is enabled then an interrupt will be generated for every such sample written to the FIFO.

©2017 Ambiq Micro, Inc.
All rights reserved.

The window comparator limits are a shared resource and apply to all active slots which have their window comparator bits enabled. If window limits are enabled for multiple enabled slots with different precision modes, the window comparison function can be configured to automatically scale the 14.6 upper and lower limits value to match the corresponding precision mode format for the enabled slots through the ADCSCWLIM register.

15.3 Operating Modes and the Mode Controller

The mode controller of Figure 68 is a sophisticated state machine that manages not only the time slot conversions but also the power state of the ADC analog components and the hand shake with the clock generator to start the HFRC clock source if required. Thus once the various control registers are initialized, the core can go to sleep and only wake up when there are valid samples in the FIFO for the interrupt service routine to distribute. Firmware does not have to keep track of which block is using the HFRC clock source since the devices in conjunction with the clock generator manage this automatically. The ADC block's mode controller participates in this clock management protocol.

From a firmware perspective, the ADC mode controller is controlled from bit fields in the ADC configuration register and from the various bit fields in the eight slot configuration registers.

The most over-riding control is the ADC enable bit in the PWR_CTRL_DEVICE_EN register of the power control block. This bit must be set to '1' to enable power to the ADC subsystem. Furthermore, the ADCEN bit in the ADC configuration register is a global functional enable bit for general ADC operation. Setting this bit to zero has many of the effects of a software reset, such as reseting the FIFO pointers. Setting this bit to one enables the mode controller to examine its inputs and proceed to autonomously handle analog to digital conversions.

An ADC scan is the process of sampling the analog voltages at each input of the ADC of Figure 68 following a trigger event. If the ADC is enabled and one or more slots are enabled, a scan is initiated after the ADC receives a trigger through one of the configured trigger sources. The scan flowchart diagram can be found in Figure 69

An ADC conversion is the process of averaging measurements following one or more scans for each slot that is enabled.

©2017 Ambiq Micro, Inc.
All rights reserved.

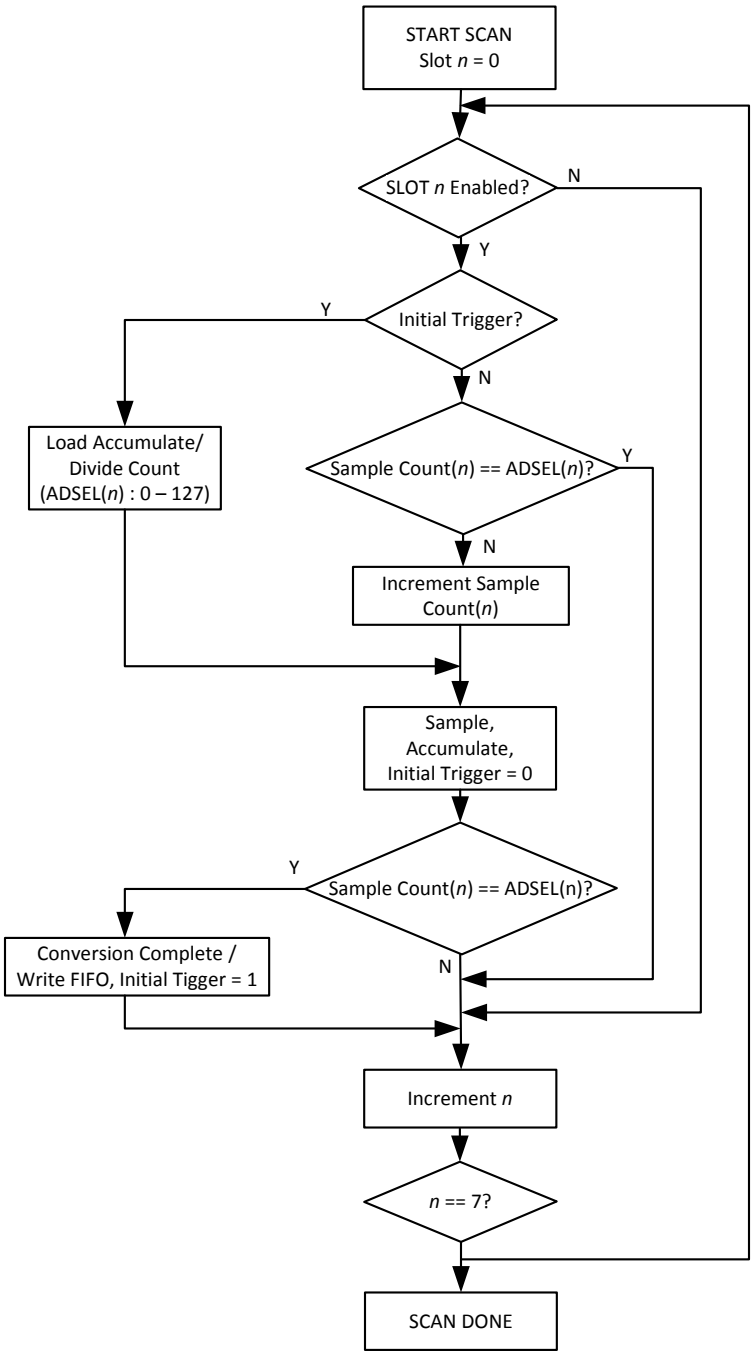


Figure 69. Scan Flowchart

15.3.1 Single Mode

In single mode, one trigger event produces one scan of all enabled slots. Depending on the settings of the accumulate and scale bit field for the active slots, this may or may not result in writing a result to the FIFO. When the trigger source is an external pin then one external pin transition of the proper polarity will result in one complete scan of all enabled slots. If the external pin is connected to a repetitive pulse source then repeating scans of all enabled slots are run at the input trigger rate.

©2017 Ambiq Micro, Inc.
All rights reserved.

15.3.2 Repeat Mode

Counter/Timer 3A has a bit in its configuration register that allows it to be a source of repetitive triggers for the ADC. If counter/timer 3 is initialized for this purpose then one only needs to turn on the RPTEN bit in the ADC configuration registers to enable this mode in the ADC.

NOTE: the mode controller does **not** process these repetitive triggers from the counter/timer until a first triggering event occurs from the normal trigger sources. Thus one can select software triggering in the TRIGSEL field and set up all of the other ADC registers for the desired sample acquisitions. Then one can write to the software trigger register and the mode controller will enter REPEAT mode. In repeat mode, the mode controller waits only for each successive counter/timer 3A input to launch a scan of all enabled slots.

15.3.3 Low Power Modes

An application may use the ADC in one of three power modes. Each mode has different implications from overall energy perspective relative to the startup latency from trigger-to-data as well as the standby power consumed. The table below is intended to provide guidance on which mode may be more effective based on latency tolerance. This table should only be used as a reference.

Table 717: ADC Power Modes

LPMODE	Definition	Entry Latency
0	ADC is kept active continuously (used in continuous sampling scenarios)	0 (requires initial calibration)
1	ADC is mostly powered off between samples, HFRC is duty cycled between samples. No calibration required after initial calibration)	<50µs (shorter for lower resolution)
2	ADC is completely powered off between samples, HFRC is duty cycled between samples. Requires recalibration for each conversion.	<600µs

15.3.3.1 Low Power Mode 0

Low Power Mode 0 (LPMODE0) enables the lowest latency from trigger to conversion data available. This mode leaves the reference buffer powered on between scans to bypass any startup latency between triggers[1].

15.3.3.2 Low Power Mode 1

Low power mode 1 (LPMODE1) is a power mode whereby the ADC Digital Controller will automatically power off the ADC clocks, analog ADC and reference buffer between scans while maintaining ADC calibration data. This mode may operate autonomously without CPU interaction, even while the CPU is in sleep or deepsleep mode for repeat mode triggers or hardware triggers. While operating in this mode, the ADC Digital Controller may be used to burst through multiple scans enabling max sample rate data collection if the triggers are running at a rate at least 2x the maximum sample rate until the final scan has completed. When a scan completes without a pending trigger latched, the ADC subsystem will enter a low power state until the next trigger event.

15.3.3.3 Low Power Mode 2

If desirable, for applications requiring infrequent conversions, software may choose to operate the ADC in LPMODE2, whereby the full ADC Analog and Digital subsystem remains completely powered off between

1. The reference buffer will not be powered on when the ADC is configured for external reference

©2017 Ambiq Micro, Inc.
All rights reserved.

samples. In this use case, the software configures the power control ADC enable register followed by configuring the ADC slots and the ADC configuration register between conversion data collections, followed by disabling the ADC in the power control ADC enable register. Although this mode provides extremely low power operation, using the ADC in this mode will result in a cold start latency including reference buffer stabilization delay and a calibration sequence 100's of microseconds, nominally. In this mode, the ADC must be reconfigured prior to any subsequent ADC operation.

15.4 Interrupts

The ADC has 6 interrupt status bits with corresponding interrupt enable bits, as follows:

1. Conversion Complete Interrupt
2. Scan Complete Interrupt
3. FIFO Overflow Level 1
4. FIFO Overflow Level 2
5. Window Comparator Excursion Interrupt (a.k.a. outside interrupt)
6. Window Comparator Incursion Interrupt (a.k.a. inside interrupt)

The window comparator interrupts are discussed above, see Section 15.2.8

There are two interrupts based on the *fullness* of the FIFO. When the respective interrupts are enabled, Overflow 1 fires when the FIFO reaches 75% full, viz. 6 entries. Overflow 2 fires when the FIFO is completely full.

When enabled, the conversion complete interrupt fires when a single slot completes its conversion and the resulting conversion data is pushed into the FIFO.

When enabled, the scan complete interrupt indicates that all enabled slots have sampled their respective channels following a trigger event.

When a single slot is enabled and programmed to average over exactly one measurement and the scan complete and conversion complete interrupts are enabled, a trigger event will result in the conversion complete and scan complete interrupts firing simultaneously upon completion of the ADC scan. Again, if both respective interrupts are enabled and a single slot is enabled and programmed to average over 128 measurements, 128 trigger events result in 128 scan complete interrupts and exactly one conversion complete interrupt following the 128 ADC scans. When multiple slots are enabled with different settings for the number of measurements to average, the conversion complete interrupt signifies that one or more of the conversions have completed and the FIFO contains valid data for one or more of the slot conversions.

©2017 Ambiq Micro, Inc.
All rights reserved.

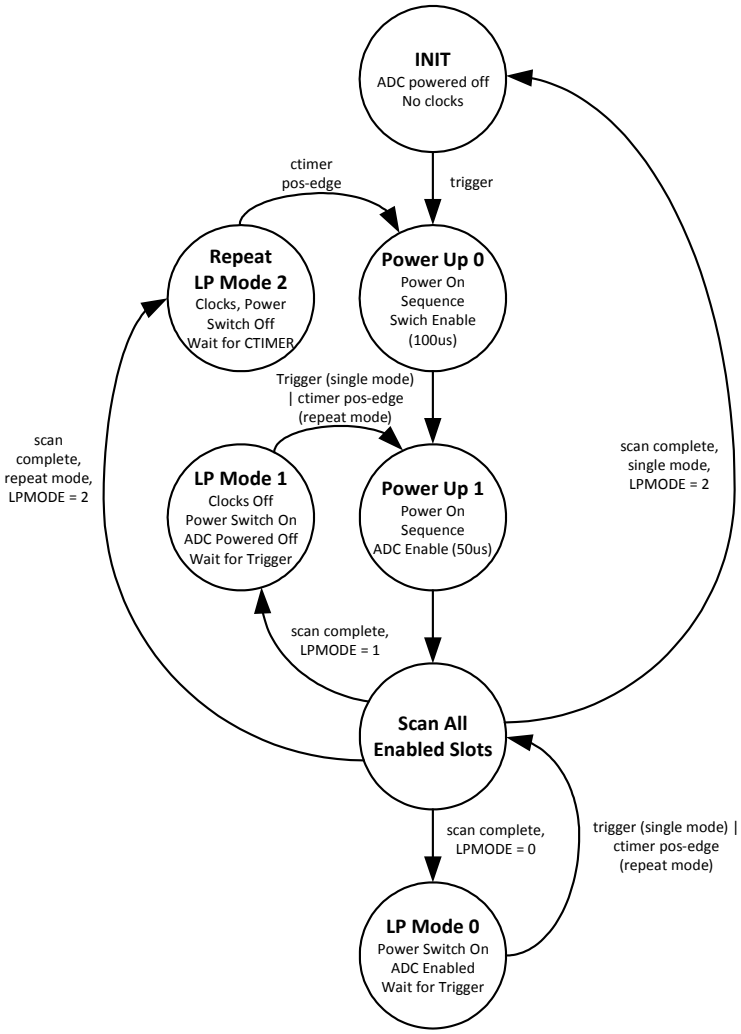


Figure 70. ADC State Diagram

15.5 Voltage Divider and Switchable Battery Load

The Apollo2 Blue's ADC includes a switchable voltage divider that enables the ADC to measure the input voltage to the VDD rail. In most systems this will be the battery voltage applied to the MCU chip. The voltage divider is only switched on when one of the active slots is selecting analog mux channel 15. That is only when the mode controller is ultimately triggered and powers up the ADC block for a conversion scan of all active slots. Otherwise, the voltage divider is turned off.

©2017 Ambiq Micro, Inc.
All rights reserved.

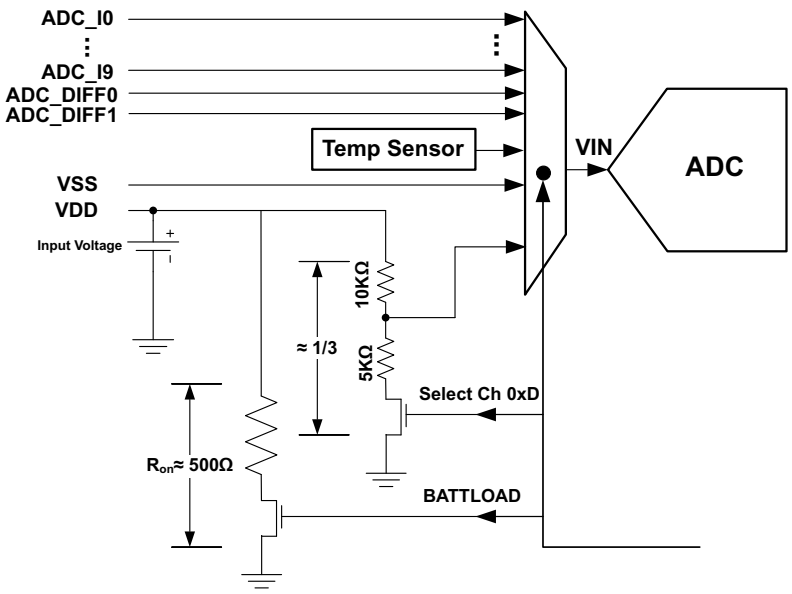


Figure 71. Switchable Battery Load

The switchable load resistor is enabled by the BATTLOAD bit as shown in the ADCBATTLOAD Register of the MCUCTRL Registers.

This feature is used to help estimate the health of the battery chemistry by estimating the internal resistance of the battery.

15.6 ADC Registers

Analog Digital Converter Control

INSTANCE 0 BASE ADDRESS:0x50010000

This is the detailed description of the Analog Digital Converter Register Block. The ADC Register Block contains the software control for enablement, slot configuration, clock configuration, trigger configuration, temperature sensor enablement, power modes, accumulate/divide, window comparison and interrupt control for the ADC functional unit.

©2017 Ambiq Micro, Inc.
All rights reserved.

15.6.1 Register Memory Map

Table 718: ADC Register Map

Address(s)	Register Name	Description
0x50010000	CFG	Configuration Register
0x50010004	STAT	ADC Power Status
0x50010008	SWT	Software trigger
0x5001000C	SL0CFG	Slot 0 Configuration Register
0x50010010	SL1CFG	Slot 1 Configuration Register
0x50010014	SL2CFG	Slot 2 Configuration Register
0x50010018	SL3CFG	Slot 3 Configuration Register
0x5001001C	SL4CFG	Slot 4 Configuration Register
0x50010020	SL5CFG	Slot 5 Configuration Register
0x50010024	SL6CFG	Slot 6 Configuration Register
0x50010028	SL7CFG	Slot 7 Configuration Register
0x5001002C	WULIM	Window Comparator Upper Limits Register
0x50010030	WLLIM	Window Comparator Lower Limits Register
0x50010038	FIFO	FIFO Data and Valid Count Register
0x50010200	INTEN	ADC Interrupt registers: Enable
0x50010204	INTSTAT	ADC Interrupt registers: Status
0x50010208	INTCLR	ADC Interrupt registers: Clear
0x5001020C	INTSET	ADC Interrupt registers: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

15.6.2 ADC Registers

15.6.2.1 CFG Register

Configuration Register

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x50010000

The ADC Configuration Register contains the software control for selecting the clock frequency used for the SAR conversions, the trigger polarity, the trigger select, the reference voltage select, the low power mode, the operating mode (single scan per trigger vs. repeating mode) and ADC enable.

Table 719: CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD						CLKSEL		RSVD				TRIGPOL	TRIGSEL			RSVD						REFSEL		RSVD			CKMODE	LPMODE	RPTEN	RSVD	ADCEN

Table 720: CFG Register Bits

Bit	Name	Reset	RW	Description
31:26	RSVD	0x0	RO	RESERVED.
25:24	CLKSEL	0x0	RW	Select the source and frequency for the ADC clock. All values not enumerated below are undefined. OFF = 0x0 - Off mode. The HFRC or HFRC_DIV2 clock must be selected for the ADC to function. The ADC controller automatically shuts off the clock in it's low power modes. When setting ADCEN to '0', the CLKSEL should remain set to one of the two clock selects for proper power down sequencing. HFRC = 0x1 - HFRC Core Clock Frequency HFRC_DIV2 = 0x2 - HFRC Core Clock / 2
23:20	RSVD	0x0	RO	RESERVED.
19	TRIGPOL	0x0	RW	This bit selects the ADC trigger polarity for external off chip triggers. RISING_EDGE = 0x0 - Trigger on rising edge. FALLING_EDGE = 0x1 - Trigger on falling edge.
18:16	TRIGSEL	0x0	RW	Select the ADC trigger source. EXT0 = 0x0 - Off chip External Trigger0 (ADC_ET0) EXT1 = 0x1 - Off chip External Trigger1 (ADC_ET1) VCOMP = 0x4 - Voltage Comparator Output SWT = 0x7 - Software Trigger
15:10	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 720: CFG Register Bits

Bit	Name	Reset	RW	Description
9:8	REFSEL	0x0	RW	Select the ADC reference voltage. INT2P0 = 0x0 - Internal 2.0V Bandgap Reference Voltage INT1P5 = 0x1 - Internal 1.5V Bandgap Reference Voltage EXT2P0 = 0x2 - Off Chip 2.0V Reference EXT1P5 = 0x3 - Off Chip 1.5V Reference
7:5	RSVD	0x0	RO	RESERVED.
4	CKMODE	0x0	RW	Clock mode register LPCKMODE = 0x0 - Disable the clock between scans for LPMODE0. Set LPCKMODE to 0x1 while configuring the ADC. LLCKMODE = 0x1 - Low Latency Clock Mode. When set, HFRC and the adc_clk will remain on while in functioning in LPMODE0.
3	LPMODE	0x0	RW	Select power mode to enter between active scans. MODE0 = 0x0 - Low Power Mode 0. Leaves the ADC fully powered between scans with minimum latency between a trigger event and sample data collection. MODE1 = 0x1 - Low Power Mode 1. Powers down all circuity and clocks associated with the ADC until the next trigger event. Between scans, the reference buffer requires up to 50us of delay from a scan trigger event before the conversion will commence while operating in this mode.
2	RPTEN	0x0	RW	This bit enables Repeating Scan Mode. SINGLE_SCAN = 0x0 - In Single Scan Mode, the ADC will complete a single scan upon each trigger event. REPEATING_SCAN = 0x1 - In Repeating Scan Mode, the ADC will complete it's first scan upon the initial trigger event and all subsequent scans will occur at regular intervals defined by the configuration programmed for the CTTMRA3 internal timer until the timer is disabled or the ADC is disabled. When disabling the ADC (setting ADCEN to '0'), the RPTEN bit should be cleared.
1	RSVD	0x0	RO	RESERVED.
0	ADCEN	0x0	RW	This bit enables the ADC module. While the ADC is enabled, the ADCCFG and SLOT Configuration regsiter settings must remain stable and unchanged. All configuration register settings, slot configuration settings and window comparison settings should be written prior to setting the ADCEN bit to '1'. DIS = 0x0 - Disable the ADC module. EN = 0x1 - Enable the ADC module.

15.6.2.2 STAT Register

ADC Power Status

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x50010004

This register indicates the basic power status for the ADC. For detailed power status, see the power control power status register. ADC power mode 0 indicates the ADC is in it's full power state and is ready to process scans. ADC Power mode 1 indicates the ADC enabled and in a low power state.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 721: STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																															PWDSTAT

Table 722: STAT Register Bits

Bit	Name	Reset	RW	Description
31:1	RSVD	0x0	RO	RESERVED.
0	PWDSTAT	0x0	RO	Indicates the power-status of the ADC. ON = 0x0 - Powered on. POWERED_DOWN = 0x1 - ADC Low Power Mode 1.

15.6.2.3 SWT Register

Software trigger

OFFSET: 0x00000008

INSTANCE 0 ADDRESS: 0x50010008

This register enables initiating an ADC scan through software.

Table 723: SWT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																								SWT							

Table 724: SWT Register Bits

Bit	Name	Reset	RW	Description
31:8	RSVD	0x0	RO	RESERVED.
7:0	SWT	0x0	RW	Writing 0x37 to this register generates a software trigger. GEN_SW_TRIGGER = 0x37 - Writing this value generates a software trigger.

©2017 Ambiq Micro, Inc.
All rights reserved.

15.6.2.4 SL0CFG Register

Slot 0 Configuration Register

OFFSET: 0x0000000C

INSTANCE 0 ADDRESS: 0x5001000C

Slot 0 Configuration Register

Table 725: SL0CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD					ADSEL0			RSVD						PRMODE0		RSVD				CHSEL0				RSVD						WCEN0	SLEN0

Table 726: SL0CFG Register Bits

Bit	Name	Reset	RW	Description
31:27	RSVD	0x0	RO	RESERVED.
26:24	ADSEL0	0x0	RW	Select the number of measurements to average in the accumulate divide module for this slot. AVG_1_MSRMT = 0x0 - Average in 1 measurement in the accumulate divide module for this slot. AVG_2_MSRMTS = 0x1 - Average in 2 measurements in the accumulate divide module for this slot. AVG_4_MSRMTS = 0x2 - Average in 4 measurements in the accumulate divide module for this slot. AVG_8_MSRMT = 0x3 - Average in 8 measurements in the accumulate divide module for this slot. AVG_16_MSRMTS = 0x4 - Average in 16 measurements in the accumulate divide module for this slot. AVG_32_MSRMTS = 0x5 - Average in 32 measurements in the accumulate divide module for this slot. AVG_64_MSRMTS = 0x6 - Average in 64 measurements in the accumulate divide module for this slot. AVG_128_MSRMTS = 0x7 - Average in 128 measurements in the accumulate divide module for this slot.
23:18	RSVD	0x0	RO	RESERVED.
17:16	PRMODE0	0x0	RW	Set the Precision Mode For Slot. P14B = 0x0 - 14-bit precision mode P12B = 0x1 - 12-bit precision mode P10B = 0x2 - 10-bit precision mode P8B = 0x3 - 8-bit precision mode
15:12	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 726: SL0CFG Register Bits

Bit	Name	Reset	RW	Description
11:8	CHSEL0	0x0	RW	Select one of the 14 channel inputs for this slot. SE0 = 0x0 - single ended external GPIO connection to pad16. SE1 = 0x1 - single ended external GPIO connection to pad29. SE2 = 0x2 - single ended external GPIO connection to pad11. SE7 = 0x7 - single ended external GPIO connection to pad35. SE8 = 0x8 - single ended external GPIO connection to pad13. SE9 = 0x9 - single ended external GPIO connection to pad12. DF0 = 0xA - differential external GPIO connections to pad12(N) and pad13(P). DF1 = 0xB - differential external GPIO connections to pad15(N) and pad14(P). TEMP = 0xC - internal temperature sensor. BATT = 0xD - internal voltage divide-by-3 connection. VSS = 0xE - Input VSS
7:2	RSVD	0x0	RO	RESERVED.
1	WCEN0	0x0	RW	This bit enables the window compare function for slot 0. WCEN = 0x1 - Enable the window compare for slot 0.
0	SLEN0	0x0	RW	This bit enables slot 0 for ADC conversions. SLEN = 0x1 - Enable slot 0 for ADC conversions.

15.6.2.5 SL1CFG Register

Slot 1 Configuration Register

OFFSET: 0x00000010

INSTANCE 0 ADDRESS: 0x50010010

Slot 1 Configuration Register

Table 727: SL1CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD					ADSEL1			RSVD						PRMODE1		RSVD				CHSEL1				RSVD						WCEN1	SLEN1

Table 728: SL1CFG Register Bits

Bit	Name	Reset	RW	Description
31:27	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 728: SL1CFG Register Bits

Bit	Name	Reset	RW	Description
26:24	ADSEL1	0x0	RW	Select the number of measurements to average in the accumulate divide module for this slot. AVG_1_MSRMT = 0x0 - Average in 1 measurement in the accumulate divide module for this slot. AVG_2_MSRMTS = 0x1 - Average in 2 measurements in the accumulate divide module for this slot. AVG_4_MSRMTS = 0x2 - Average in 4 measurements in the accumulate divide module for this slot. AVG_8_MSRMT = 0x3 - Average in 8 measurements in the accumulate divide module for this slot. AVG_16_MSRMTS = 0x4 - Average in 16 measurements in the accumulate divide module for this slot. AVG_32_MSRMTS = 0x5 - Average in 32 measurements in the accumulate divide module for this slot. AVG_64_MSRMTS = 0x6 - Average in 64 measurements in the accumulate divide module for this slot. AVG_128_MSRMTS = 0x7 - Average in 128 measurements in the accumulate divide module for this slot.
23:18	RSVD	0x0	RO	RESERVED.
17:16	PRMODE1	0x0	RW	Set the Precision Mode For Slot. P14B = 0x0 - 14-bit precision mode P12B = 0x1 - 12-bit precision mode P10B = 0x2 - 10-bit precision mode P8B = 0x3 - 8-bit precision mode
15:12	RSVD	0x0	RO	RESERVED.
11:8	CHSEL1	0x0	RW	Select one of the 14 channel inputs for this slot. SE0 = 0x0 - single ended external GPIO connection to pad16. SE1 = 0x1 - single ended external GPIO connection to pad29. SE2 = 0x2 - single ended external GPIO connection to pad11. SE7 = 0x7 - single ended external GPIO connection to pad35. SE8 = 0x8 - single ended external GPIO connection to pad13. SE9 = 0x9 - single ended external GPIO connection to pad12. DF0 = 0xA - differential external GPIO connections to pad12(N) and pad13(P). DF1 = 0xB - differential external GPIO connections to pad15(N) and pad14(P). TEMP = 0xC - internal temperature sensor. BATT = 0xD - internal voltage divide-by-3 connection. VSS = 0xE - Input VSS
7:2	RSVD	0x0	RO	RESERVED.
1	WCEN1	0x0	RW	This bit enables the window compare function for slot 1. WCEN = 0x1 - Enable the window compare for slot 1.
0	SLEN1	0x0	RW	This bit enables slot 1 for ADC conversions. SLEN = 0x1 - Enable slot 1 for ADC conversions.

©2017 Ambiq Micro, Inc.
All rights reserved.

15.6.2.6 SL2CFG Register

Slot 2 Configuration Register

OFFSET: 0x00000014

INSTANCE 0 ADDRESS: 0x50010014

Slot 2 Configuration Register

Table 729: SL2CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD					ADSEL2			RSVD						PRMODE2		RSVD				CHSEL2				RSVD						WCEN2	SLEN2

Table 730: SL2CFG Register Bits

Bit	Name	Reset	RW	Description
31:27	RSVD	0x0	RO	RESERVED.
26:24	ADSEL2	0x0	RW	Select the number of measurements to average in the accumulate divide module for this slot. AVG_1_MSRMT = 0x0 - Average in 1 measurement in the accumulate divide module for this slot. AVG_2_MSRMTS = 0x1 - Average in 2 measurements in the accumulate divide module for this slot. AVG_4_MSRMTS = 0x2 - Average in 4 measurements in the accumulate divide module for this slot. AVG_8_MSRMT = 0x3 - Average in 8 measurements in the accumulate divide module for this slot. AVG_16_MSRMTS = 0x4 - Average in 16 measurements in the accumulate divide module for this slot. AVG_32_MSRMTS = 0x5 - Average in 32 measurements in the accumulate divide module for this slot. AVG_64_MSRMTS = 0x6 - Average in 64 measurements in the accumulate divide module for this slot. AVG_128_MSRMTS = 0x7 - Average in 128 measurements in the accumulate divide module for this slot.
23:18	RSVD	0x0	RO	RESERVED.
17:16	PRMODE2	0x0	RW	Set the Precision Mode For Slot. P14B = 0x0 - 14-bit precision mode P12B = 0x1 - 12-bit precision mode P10B = 0x2 - 10-bit precision mode P8B = 0x3 - 8-bit precision mode
15:12	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 730: SL2CFG Register Bits

Bit	Name	Reset	RW	Description
11:8	CHSEL2	0x0	RW	Select one of the 14 channel inputs for this slot. SE0 = 0x0 - single ended external GPIO connection to pad16. SE1 = 0x1 - single ended external GPIO connection to pad29. SE2 = 0x2 - single ended external GPIO connection to pad11. SE7 = 0x7 - single ended external GPIO connection to pad35. SE8 = 0x8 - single ended external GPIO connection to pad13. SE9 = 0x9 - single ended external GPIO connection to pad12. DF0 = 0xA - differential external GPIO connections to pad12(N) and pad13(P). DF1 = 0xB - differential external GPIO connections to pad15(N) and pad14(P). TEMP = 0xC - internal temperature sensor. BATT = 0xD - internal voltage divide-by-3 connection. VSS = 0xE - Input VSS
7:2	RSVD	0x0	RO	RESERVED.
1	WCEN2	0x0	RW	This bit enables the window compare function for slot 2. WCEN = 0x1 - Enable the window compare for slot 2.
0	SLEN2	0x0	RW	This bit enables slot 2 for ADC conversions. SLEN = 0x1 - Enable slot 2 for ADC conversions.

15.6.2.7 SL3CFG Register

Slot 3 Configuration Register

OFFSET: 0x00000018

INSTANCE 0 ADDRESS: 0x50010018

Slot 3 Configuration Register

Table 731: SL3CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD					ADSEL3			RSVD						PRMODE3		RSVD				CHSEL3				RSVD						WCEN3	SLEN3

Table 732: SL3CFG Register Bits

Bit	Name	Reset	RW	Description
31:27	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 732: SL3CFG Register Bits

Bit	Name	Reset	RW	Description
26:24	ADSEL3	0x0	RW	Select the number of measurements to average in the accumulate divide module for this slot. AVG_1_MSRMT = 0x0 - Average in 1 measurement in the accumulate divide module for this slot. AVG_2_MSRMTS = 0x1 - Average in 2 measurements in the accumulate divide module for this slot. AVG_4_MSRMTS = 0x2 - Average in 4 measurements in the accumulate divide module for this slot. AVG_8_MSRMT = 0x3 - Average in 8 measurements in the accumulate divide module for this slot. AVG_16_MSRMTS = 0x4 - Average in 16 measurements in the accumulate divide module for this slot. AVG_32_MSRMTS = 0x5 - Average in 32 measurements in the accumulate divide module for this slot. AVG_64_MSRMTS = 0x6 - Average in 64 measurements in the accumulate divide module for this slot. AVG_128_MSRMTS = 0x7 - Average in 128 measurements in the accumulate divide module for this slot.
23:18	RSVD	0x0	RO	RESERVED.
17:16	PRMODE3	0x0	RW	Set the Precision Mode For Slot. P14B = 0x0 - 14-bit precision mode P12B = 0x1 - 12-bit precision mode P10B = 0x2 - 10-bit precision mode P8B = 0x3 - 8-bit precision mode
15:12	RSVD	0x0	RO	RESERVED.
11:8	CHSEL3	0x0	RW	Select one of the 14 channel inputs for this slot. SE0 = 0x0 - single ended external GPIO connection to pad16. SE1 = 0x1 - single ended external GPIO connection to pad29. SE2 = 0x2 - single ended external GPIO connection to pad11. SE7 = 0x7 - single ended external GPIO connection to pad35. SE8 = 0x8 - single ended external GPIO connection to pad13. SE9 = 0x9 - single ended external GPIO connection to pad12. DF0 = 0xA - differential external GPIO connections to pad12(N) and pad13(P). DF1 = 0xB - differential external GPIO connections to pad15(N) and pad14(P). TEMP = 0xC - internal temperature sensor. BATT = 0xD - internal voltage divide-by-3 connection. VSS = 0xE - Input VSS
7:2	RSVD	0x0	RO	RESERVED.
1	WCEN3	0x0	RW	This bit enables the window compare function for slot 3. WCEN = 0x1 - Enable the window compare for slot 3.
0	SLEN3	0x0	RW	This bit enables slot 3 for ADC conversions. SLEN = 0x1 - Enable slot 3 for ADC conversions.

©2017 Ambiq Micro, Inc.
All rights reserved.

15.6.2.8 SL4CFG Register

Slot 4 Configuration Register

OFFSET: 0x0000001C

INSTANCE 0 ADDRESS: 0x5001001C

Slot 4 Configuration Register

Table 733: SL4CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD					ADSEL4			RSVD						PRMODE4		RSVD				CHSEL4				RSVD						WCEN4	SLEN4

Table 734: SL4CFG Register Bits

Bit	Name	Reset	RW	Description
31:27	RSVD	0x0	RO	RESERVED.
26:24	ADSEL4	0x0	RW	Select the number of measurements to average in the accumulate divide module for this slot. AVG_1_MSRMT = 0x0 - Average in 1 measurement in the accumulate divide module for this slot. AVG_2_MSRMTS = 0x1 - Average in 2 measurements in the accumulate divide module for this slot. AVG_4_MSRMTS = 0x2 - Average in 4 measurements in the accumulate divide module for this slot. AVG_8_MSRMT = 0x3 - Average in 8 measurements in the accumulate divide module for this slot. AVG_16_MSRMTS = 0x4 - Average in 16 measurements in the accumulate divide module for this slot. AVG_32_MSRMTS = 0x5 - Average in 32 measurements in the accumulate divide module for this slot. AVG_64_MSRMTS = 0x6 - Average in 64 measurements in the accumulate divide module for this slot. AVG_128_MSRMTS = 0x7 - Average in 128 measurements in the accumulate divide module for this slot.
23:18	RSVD	0x0	RO	RESERVED.
17:16	PRMODE4	0x0	RW	Set the Precision Mode For Slot. P14B = 0x0 - 14-bit precision mode P12B = 0x1 - 12-bit precision mode P10B = 0x2 - 10-bit precision mode P8B = 0x3 - 8-bit precision mode
15:12	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 734: SL4CFG Register Bits

Bit	Name	Reset	RW	Description
11:8	CHSEL4	0x0	RW	Select one of the 14 channel inputs for this slot. SE0 = 0x0 - single ended external GPIO connection to pad16. SE1 = 0x1 - single ended external GPIO connection to pad29. SE2 = 0x2 - single ended external GPIO connection to pad11. SE7 = 0x7 - single ended external GPIO connection to pad35. SE8 = 0x8 - single ended external GPIO connection to pad13. SE9 = 0x9 - single ended external GPIO connection to pad12. DF0 = 0xA - differential external GPIO connections to pad12(N) and pad13(P). DF1 = 0xB - differential external GPIO connections to pad15(N) and pad14(P). TEMP = 0xC - internal temperature sensor. BATT = 0xD - internal voltage divide-by-3 connection. VSS = 0xE - Input VSS
7:2	RSVD	0x0	RO	RESERVED.
1	WCEN4	0x0	RW	This bit enables the window compare function for slot 4. WCEN = 0x1 - Enable the window compare for slot 4.
0	SLEN4	0x0	RW	This bit enables slot 4 for ADC conversions. SLEN = 0x1 - Enable slot 4 for ADC conversions.

15.6.2.9 SL5CFG Register

Slot 5 Configuration Register

OFFSET: 0x00000020

INSTANCE 0 ADDRESS: 0x50010020

Slot 5 Configuration Register

Table 735: SL5CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD					ADSEL5			RSVD						PRMODE5		RSVD				CHSEL5				RSVD						WCEN5	SLEN5

Table 736: SL5CFG Register Bits

Bit	Name	Reset	RW	Description
31:27	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 736: SL5CFG Register Bits

Bit	Name	Reset	RW	Description
26:24	ADSEL5	0x0	RW	Select number of measurements to average in the accumulate divide module for this slot. AVG_1_MSRMT = 0x0 - Average in 1 measurement in the accumulate divide module for this slot. AVG_2_MSRMTS = 0x1 - Average in 2 measurements in the accumulate divide module for this slot. AVG_4_MSRMTS = 0x2 - Average in 4 measurements in the accumulate divide module for this slot. AVG_8_MSRMT = 0x3 - Average in 8 measurements in the accumulate divide module for this slot. AVG_16_MSRMTS = 0x4 - Average in 16 measurements in the accumulate divide module for this slot. AVG_32_MSRMTS = 0x5 - Average in 32 measurements in the accumulate divide module for this slot. AVG_64_MSRMTS = 0x6 - Average in 64 measurements in the accumulate divide module for this slot. AVG_128_MSRMTS = 0x7 - Average in 128 measurements in the accumulate divide module for this slot.
23:18	RSVD	0x0	RO	RESERVED.
17:16	PRMODE5	0x0	RW	Set the Precision Mode For Slot. P14B = 0x0 - 14-bit precision mode P12B = 0x1 - 12-bit precision mode P10B = 0x2 - 10-bit precision mode P8B = 0x3 - 8-bit precision mode
15:12	RSVD	0x0	RO	RESERVED.
11:8	CHSEL5	0x0	RW	Select one of the 14 channel inputs for this slot. SE0 = 0x0 - single ended external GPIO connection to pad16. SE1 = 0x1 - single ended external GPIO connection to pad29. SE2 = 0x2 - single ended external GPIO connection to pad11. SE7 = 0x7 - single ended external GPIO connection to pad35. SE8 = 0x8 - single ended external GPIO connection to pad13. SE9 = 0x9 - single ended external GPIO connection to pad12. DF0 = 0xA - differential external GPIO connections to pad12(N) and pad13(P). DF1 = 0xB - differential external GPIO connections to pad15(N) and pad14(P). TEMP = 0xC - internal temperature sensor. BATT = 0xD - internal voltage divide-by-3 connection. VSS = 0xE - Input VSS
7:2	RSVD	0x0	RO	RESERVED.
1	WCEN5	0x0	RW	This bit enables the window compare function for slot 5. WCEN = 0x1 - Enable the window compare for slot 5.
0	SLEN5	0x0	RW	This bit enables slot 5 for ADC conversions. SLEN = 0x1 - Enable slot 5 for ADC conversions.

©2017 Ambiq Micro, Inc.
All rights reserved.

15.6.2.10SL6CFG Register

Slot 6 Configuration Register

OFFSET: 0x00000024

INSTANCE 0 ADDRESS: 0x50010024

Slot 6 Configuration Register

Table 737: SL6CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD					ADSEL6			RSVD						PRMODE6		RSVD				CHSEL6				RSVD						WCEN6	SLEN6

Table 738: SL6CFG Register Bits

Bit	Name	Reset	RW	Description
31:27	RSVD	0x0	RO	RESERVED.
26:24	ADSEL6	0x0	RW	Select the number of measurements to average in the accumulate divide module for this slot. AVG_1_MSRMT = 0x0 - Average in 1 measurement in the accumulate divide module for this slot. AVG_2_MSRMTS = 0x1 - Average in 2 measurements in the accumulate divide module for this slot. AVG_4_MSRMTS = 0x2 - Average in 4 measurements in the accumulate divide module for this slot. AVG_8_MSRMT = 0x3 - Average in 8 measurements in the accumulate divide module for this slot. AVG_16_MSRMTS = 0x4 - Average in 16 measurements in the accumulate divide module for this slot. AVG_32_MSRMTS = 0x5 - Average in 32 measurements in the accumulate divide module for this slot. AVG_64_MSRMTS = 0x6 - Average in 64 measurements in the accumulate divide module for this slot. AVG_128_MSRMTS = 0x7 - Average in 128 measurements in the accumulate divide module for this slot.
23:18	RSVD	0x0	RO	RESERVED.
17:16	PRMODE6	0x0	RW	Set the Precision Mode For Slot. P14B = 0x0 - 14-bit precision mode P12B = 0x1 - 12-bit precision mode P10B = 0x2 - 10-bit precision mode P8B = 0x3 - 8-bit precision mode
15:12	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 738: SL6CFG Register Bits

Bit	Name	Reset	RW	Description
11:8	CHSEL6	0x0	RW	Select one of the 14 channel inputs for this slot. SE0 = 0x0 - single ended external GPIO connection to pad16. SE1 = 0x1 - single ended external GPIO connection to pad29. SE2 = 0x2 - single ended external GPIO connection to pad11. SE7 = 0x7 - single ended external GPIO connection to pad35. SE8 = 0x8 - single ended external GPIO connection to pad13. SE9 = 0x9 - single ended external GPIO connection to pad12. DF0 = 0xA - differential external GPIO connections to pad12(N) and pad13(P). DF1 = 0xB - differential external GPIO connections to pad15(N) and pad14(P). TEMP = 0xC - internal temperature sensor. BATT = 0xD - internal voltage divide-by-3 connection. VSS = 0xE - Input VSS
7:2	RSVD	0x0	RO	RESERVED.
1	WCEN6	0x0	RW	This bit enables the window compare function for slot 6. WCEN = 0x1 - Enable the window compare for slot 6.
0	SLEN6	0x0	RW	This bit enables slot 6 for ADC conversions. SLEN = 0x1 - Enable slot 6 for ADC conversions.

15.6.2.11SL7CFG Register

Slot 7 Configuration Register

OFFSET: 0x00000028

INSTANCE 0 ADDRESS: 0x50010028

Slot 7 Configuration Register

Table 739: SL7CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD					ADSEL7			RSVD							PRMODE7	RSVD				CHSEL7				RSVD							WCEN7	SLEN7

Table 740: SL7CFG Register Bits

Bit	Name	Reset	RW	Description
31:27	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 740: SL7CFG Register Bits

Bit	Name	Reset	RW	Description
26:24	ADSEL7	0x0	RW	Select the number of measurements to average in the accumulate divide module for this slot. AVG_1_MSRMT = 0x0 - Average in 1 measurement in the accumulate divide module for this slot. AVG_2_MSRMTS = 0x1 - Average in 2 measurements in the accumulate divide module for this slot. AVG_4_MSRMTS = 0x2 - Average in 4 measurements in the accumulate divide module for this slot. AVG_8_MSRMT = 0x3 - Average in 8 measurements in the accumulate divide module for this slot. AVG_16_MSRMTS = 0x4 - Average in 16 measurements in the accumulate divide module for this slot. AVG_32_MSRMTS = 0x5 - Average in 32 measurements in the accumulate divide module for this slot. AVG_64_MSRMTS = 0x6 - Average in 64 measurements in the accumulate divide module for this slot. AVG_128_MSRMTS = 0x7 - Average in 128 measurements in the accumulate divide module for this slot.
23:18	RSVD	0x0	RO	RESERVED.
17:16	PRMODE7	0x0	RW	Set the Precision Mode For Slot. P14B = 0x0 - 14-bit precision mode P12B = 0x1 - 12-bit precision mode P10B = 0x2 - 10-bit precision mode P8B = 0x3 - 8-bit precision mode
15:12	RSVD	0x0	RO	RESERVED.
11:8	CHSEL7	0x0	RW	Select one of the 14 channel inputs for this slot. SE0 = 0x0 - single ended external GPIO connection to pad16. SE1 = 0x1 - single ended external GPIO connection to pad29. SE2 = 0x2 - single ended external GPIO connection to pad11. SE7 = 0x7 - single ended external GPIO connection to pad35. SE8 = 0x8 - single ended external GPIO connection to pad13. SE9 = 0x9 - single ended external GPIO connection to pad12. DF0 = 0xA - differential external GPIO connections to pad12(N) and pad13(P). DF1 = 0xB - differential external GPIO connections to pad15(N) and pad14(P). TEMP = 0xC - internal temperature sensor. BATT = 0xD - internal voltage divide-by-3 connection. VSS = 0xE - Input VSS
7:2	RSVD	0x0	RO	RESERVED.
1	WCEN7	0x0	RW	This bit enables the window compare function for slot 7. WCEN = 0x1 - Enable the window compare for slot 7.
0	SLEN7	0x0	RW	This bit enables slot 7 for ADC conversions. SLEN = 0x1 - Enable slot 7 for ADC conversions.

©2017 Ambiq Micro, Inc.
All rights reserved.

15.6.2.12WULIM Register

Window Comparator Upper Limits Register

OFFSET: 0x0000002C

INSTANCE 0 ADDRESS: 0x5001002C

Window Comparator Upper Limits Register

Table 741: WULIM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD												ULIM																			

Table 742: WULIM Register Bits

Bit	Name	Reset	RW	Description
31:20	RSVD	0x0	RO	RESERVED.
19:0	ULIM	0x0	RW	Sets the upper limit for the wondow comparator.

15.6.2.13WLLIM Register

Window Comparator Lower Limits Register

OFFSET: 0x00000030

INSTANCE 0 ADDRESS: 0x50010030

Window Comparator Lower Limits Register

Table 743: WLLIM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD												LLIM																			

Table 744: WLLIM Register Bits

Bit	Name	Reset	RW	Description
31:20	RSVD	0x0	RO	RESERVED.
19:0	LLIM	0x0	RW	Sets the lower limit for the wondow comparator.

©2017 Ambiq Micro, Inc.
All rights reserved.

15.6.2.14FIFO Register

FIFO Data and Valid Count Register

OFFSET: 0x00000038

INSTANCE 0 ADDRESS: 0x50010038

The ADC FIFO Register contains the slot number and fifo data for the oldest conversion data in the FIFO. The COUNT field indicates the total number of valid entries in the FIFO. A write to this register will pop one of the FIFO entries off the FIFO and decrease the COUNT by 1 if the COUNT is greater than zero.

Table 745: FIFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	SLOTNUM			COUNT								DATA																			

Table 746: FIFO Register Bits

Bit	Name	Reset	RW	Description
31	RSVD	0x0	RO	RESERVED.
30:28	SLOTNUM	0x0	RO	Slot number associated with this FIFO data.
27:20	COUNT	0x0	RO	Number of valid entries in the ADC FIFO.
19:0	DATA	0x0	RO	Oldest data in the FIFO.

15.6.2.15INTEN Register

ADC Interrupt registers: Enable

OFFSET: 0x00000200

INSTANCE 0 ADDRESS: 0x50010200

Set bits in this register to allow this module to generate the corresponding interrupt.

Table 747: INTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										WCINC	WCEXC	FIFOOVR2	FIFOOVR1	SCNCMP	CNVCMP

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 748: INTEN Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED.
5	WCINC	0x0	RW	Window comparator voltage incursion interrupt. WCINCINT = 0x1 - Window comparator voltage incursion interrupt.
4	WCEXC	0x0	RW	Window comparator voltage excursion interrupt. WCEXCINT = 0x1 - Window comparator voltage excursion interrupt.
3	FIFOOVR2	0x0	RW	FIFO 100% full interrupt. FIFOFULLINT = 0x1 - FIFO 100% full interrupt.
2	FIFOOVR1	0x0	RW	FIFO 75% full interrupt. FIFO75INT = 0x1 - FIFO 75% full interrupt.
1	SCNCMP	0x0	RW	ADC scan complete interrupt. SCNCMPINT = 0x1 - ADC scan complete interrupt.
0	CNVCMP	0x0	RW	ADC conversion complete interrupt. CNVCMPINT = 0x1 - ADC conversion complete interrupt.

15.6.2.16INTSTAT Register

ADC Interrupt registers: Status

OFFSET: 0x00000204

INSTANCE 0 ADDRESS: 0x50010204

Read bits from this register to discover the cause of a recent interrupt.

Table 749: INTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										WCINC	WCEXC	FIFOOVR2	FIFOOVR1	SCNCMP	CNVCMP

Table 750: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 750: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
5	WCINC	0x0	RW	Window comparator voltage incursion interrupt. WCINCINT = 0x1 - Window comparator voltage incursion interrupt.
4	WCEXC	0x0	RW	Window comparator voltage excursion interrupt. WCEXCINT = 0x1 - Window comparator voltage excursion interrupt.
3	FIFOOVR2	0x0	RW	FIFO 100% full interrupt. FIFOFULLINT = 0x1 - FIFO 100% full interrupt.
2	FIFOOVR1	0x0	RW	FIFO 75% full interrupt. FIFO75INT = 0x1 - FIFO 75% full interrupt.
1	SCNCMP	0x0	RW	ADC scan complete interrupt. SCNCMPINT = 0x1 - ADC scan complete interrupt.
0	CNVCMP	0x0	RW	ADC conversion complete interrupt. CNVCMPINT = 0x1 - ADC conversion complete interrupt.

15.6.2.17INTCLR Register

ADC Interrupt registers: Clear

OFFSET: 0x00000208

INSTANCE 0 ADDRESS: 0x50010208

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 751: INTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										WCINC	WCEXC	FIFOOVR2	FIFOOVR1	SCNCMP	CNVCMP

Table 752: INTCLR Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED.
5	WCINC	0x0	RW	Window comparator voltage incursion interrupt. WCINCINT = 0x1 - Window comparator voltage incursion interrupt.
4	WCEXC	0x0	RW	Window comparator voltage excursion interrupt. WCEXCINT = 0x1 - Window comparator voltage excursion interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 752: INTCLR Register Bits

Bit	Name	Reset	RW	Description
3	FIFOOVR2	0x0	RW	FIFO 100% full interrupt. FIFOFULLINT = 0x1 - FIFO 100% full interrupt.
2	FIFOOVR1	0x0	RW	FIFO 75% full interrupt. FIFO75INT = 0x1 - FIFO 75% full interrupt.
1	SCNCMP	0x0	RW	ADC scan complete interrupt. SCNCMPINT = 0x1 - ADC scan complete interrupt.
0	CNVCMP	0x0	RW	ADC conversion complete interrupt. CNVCMPINT = 0x1 - ADC conversion complete interrupt.

15.6.2.18INTSET Register

ADC Interrupt registers: Set

OFFSET: 0x0000020C

INSTANCE 0 ADDRESS: 0x5001020C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 753: INTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																										WCINC	WCEXC	FIFOOVR2	FIFOOVR1	SCNCMP	CNVCMP

Table 754: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:6	RSVD	0x0	RO	RESERVED.
5	WCINC	0x0	RW	Window comparator voltage incursion interrupt. WCINCINT = 0x1 - Window comparator voltage incursion interrupt.
4	WCEXC	0x0	RW	Window comparator voltage excursion interrupt. WCEXCINT = 0x1 - Window comparator voltage excursion interrupt.
3	FIFOOVR2	0x0	RW	FIFO 100% full interrupt. FIFOFULLINT = 0x1 - FIFO 100% full interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 754: INTSET Register Bits

Bit	Name	Reset	RW	Description
2	FIFOOVR1	0x0	RW	FIFO 75% full interrupt. FIFO75INT = 0x1 - FIFO 75% full interrupt.
1	SCNCMP	0x0	RW	ADC scan complete interrupt. SCNCMPINT = 0x1 - ADC scan complete interrupt.
0	CNVCMP	0x0	RW	ADC conversion complete interrupt. CNVCMPINT = 0x1 - ADC conversion complete interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

16. Voltage Comparator Module

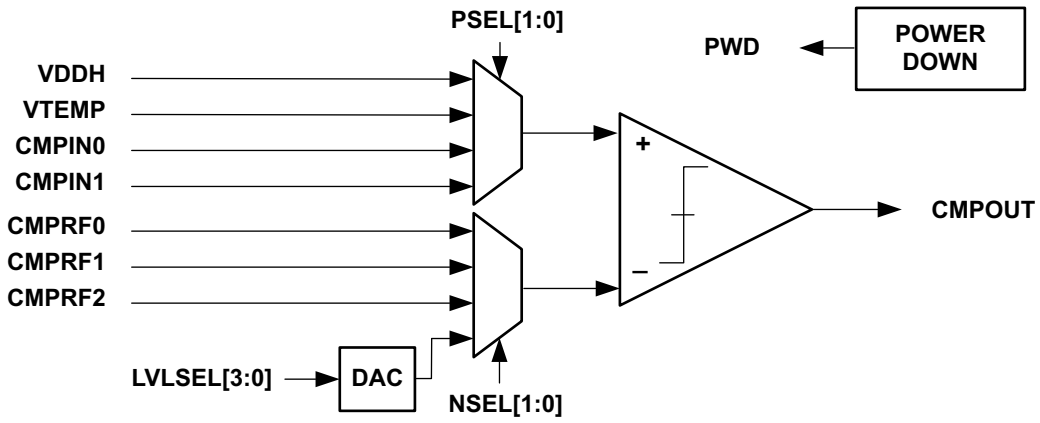


Figure 72. Block diagram for the Voltage Comparator Module

16.1 Functional Overview

The Voltage Comparator Module, shown in Figure 72, measures a user-selectable voltage at all times. It provides interrupt and software access to the comparator output with multiple options for input and reference voltages . It can be configured to generate an interrupt when the monitored voltage rises above a user-configurable threshold or when the monitored voltage drops below a user-configurable threshold.

The voltage to be monitored is selected by programming the comparator's positive terminal signal, PSEL[1:0] and may be any of: 1) the supply voltage (VDDH), 2) the PTAT voltage from the temperature sensor (VTEMP), or 3) two external voltage channels (CMPIN0 and CMPIN1).

The reference voltage is selected by programming the comparator's negative terminal, NSEL[1:0] and may be any of: 1) three external voltage channels (CMPRF0, CMPRF1, CMPRF2), or 2) the internally generated reference (VREFINT). The internal reference voltage is tuned using an on-chip DAC with level select signal LVLSEL[3:0]. When using external inputs or reference inputs, the associated pads must be configured using the GPIO function selects explained in the GPIO document section.

The Voltage Comparator CMPOUT output will remain high while the voltage at the positive input is above the voltage at reference input. The CMPOUT output will transition low when the voltage at the positive input to the comparator falls below the reference input taking into account hysteresis (see Section 18.10 for hysteresis range). The CMPOUT output is directly accessible by software by reading the CMPOUT field in the status register. The OUTHI interrupt will be set if enabled and the CMPOUT transitions high or if it is high at the time the interrupt is enabled. Similarly, the OUTLOW interrupt will be set if enabled and the CMPOUT output transitions low or if it is low at the time the interrupt is enabled.

The Voltage Comparator Module is enabled by default and may be powered off by writing 0x37 to the PWDKEY register.

16.2 VCOMP Registers

Voltage Comparator

INSTANCE 0 BASE ADDRESS:0x4000C000

©2017 Ambiq Micro, Inc.
All rights reserved.

This is the detailed description of the Voltage Comparator Register Block. The Voltage Cmparator Register Block contains the software control for selecting the comparator inputs, powerdown control, observing comparator output status and enabling interrupts.

16.2.1 Register Memory Map

Table 755: VCOMP Register Map

Address(s)	Register Name	Description
0x4000C000	CFG	Configuration Register
0x4000C004	STAT	Status Register
0x4000C008	PWDKEY	Key Register for Powering Down the Voltage Comparator
0x4000C200	INTEN	Voltage Comparator Interrupt registers: Enable
0x4000C204	INTSTAT	Voltage Comparator Interrupt registers: Status
0x4000C208	INTCLR	Voltage Comparator Interrupt registers: Clear
0x4000C20C	INTSET	Voltage Comparator Interrupt registers: Set

©2017 Ambiq Micro, Inc.
All rights reserved.

16.2.2 VCOMP Registers

16.2.2.1 CFG Register

Configuration Register

OFFSET: 0x00000000

INSTANCE 0 ADDRESS: 0x4000C000

The Voltage Comparator Configuration Register contains the software control for selecting beween the 4 options for the positive input as well as the multiple options for the reference input.

Table 756: CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD												LVLSEL				RSVD						NSEL		RSVD						PSEL	

Table 757: CFG Register Bits

Bit	Name	Reset	RW	Description
31:20	RSVD	0x0	RO	This bitfield is reserved for future use.
19:16	LVLSEL	0x0	RW	When the reference input NSEL is set to NSEL_DAC, this bitfield selects the voltage level for the negative input to the comparator. 0P58V = 0x0 - Set Reference input to 0.58 Volts. 0P77V = 0x1 - Set Reference input to 0.77 Volts. 0P97V = 0x2 - Set Reference input to 0.97 Volts. 1P16V = 0x3 - Set Reference input to 1.16 Volts. 1P35V = 0x4 - Set Reference input to 1.35 Volts. 1P55V = 0x5 - Set Reference input to 1.55 Volts. 1P74V = 0x6 - Set Reference input to 1.74 Volts. 1P93V = 0x7 - Set Reference input to 1.93 Volts. 2P13V = 0x8 - Set Reference input to 2.13 Volts. 2P32V = 0x9 - Set Reference input to 2.32 Volts. 2P51V = 0xA - Set Reference input to 2.51 Volts. 2P71V = 0xB - Set Reference input to 2.71 Volts. 2P90V = 0xC - Set Reference input to 2.90 Volts. 3P09V = 0xD - Set Reference input to 3.09 Volts. 3P29V = 0xE - Set Reference input to 3.29 Volts. 3P48V = 0xF - Set Reference input to 3.48 Volts.
15:10	RSVD	0x0	RO	This bitfield is reserved for future use.
9:8	NSEL	0x0	RW	This bitfield selects the negative input to the comparator. VREFEXT1 = 0x0 - Use external reference 1 for reference input. VREFEXT2 = 0x1 - Use external reference 2 for reference input. VREFEXT3 = 0x2 - Use external reference 3 for reference input. DAC = 0x3 - Use DAC output selected by LVLSEL for reference input.
7:2	RSVD	0x0	RO	This bitfield is reserved for future use.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 757: CFG Register Bits

Bit	Name	Reset	RW	Description
1:0	PSEL	0x0	RW	This bitfield selects the positive input to the comparator. VDDADJ = 0x0 - Use VDDADJ for the positive input. VTEMP = 0x1 - Use the temperature sensor output for the positive input. Note: If this channel is selected for PSEL, the bandap circuit required for temperature comparisons will automatically turn on. The bandgap circuit requires 11us to stabalize. VEXT1 = 0x2 - Use external voltage 0 for positive input. VEXT2 = 0x3 - Use external voltage 1 for positive input.

16.2.2.2 STAT Register

Status Register

OFFSET: 0x00000004

INSTANCE 0 ADDRESS: 0x4000C004

Status Register

Table 758: STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														PWDSTAT	CMPOUT

Table 759: STAT Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	This bitfield is reserved for future use.
1	PWDSTAT	0x0	RO	This bit indicates the power down state of the voltage comparator. POWERED_DOWN = 0x1 - The voltage comparator is powered down.
0	CMPOUT	0x0	RO	This bit is 1 if the positive input of the comparator is greater than the negative input. VOUT_LOW = 0x0 - The negative input of the comparator is greater than the positive input. VOUT_HIGH = 0x1 - The positive input of the comparator is greater than the negative input.

16.2.2.3 PWDKEY Register

Key Register for Powering Down the Voltage Comparator

OFFSET: 0x00000008

INSTANCE 0 ADDRESS: 0x4000C008

©2017 Ambiq Micro, Inc.
All rights reserved.

Key Register for Powering Down the Voltage Comparator

Table 760: PWDKEY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PWDKEY																															

Table 761: PWDKEY Register Bits

Bit	Name	Reset	RW	Description
31:0	PWDKEY	0x0	RW	Key register value. Key = 0x37 - Key

16.2.2.4 INTEN Register

Voltage Comparator Interrupt registers: Enable

OFFSET: 0x00000200

INSTANCE 0 ADDRESS: 0x4000C200

Set bits in this register to allow this module to generate the corresponding interrupt.

Table 762: INTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														OUTHI	OUTLOW

Table 763: INTEN Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	This bitfield is reserved for future use.
1	OUTHI	0x0	RW	This bit is the vcompout high interrupt.
0	OUTLOW	0x0	RW	This bit is the vcompout low interrupt.

16.2.2.5 INTSTAT Register

Voltage Comparator Interrupt registers: Status

OFFSET: 0x00000204

©2017 Ambiq Micro, Inc.
All rights reserved.

INSTANCE 0 ADDRESS: 0x4000C204

Read bits from this register to discover the cause of a recent interrupt.

Table 764: INTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														OUTHI	OUTLOW

Table 765: INTSTAT Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	This bitfield is reserved for future use.
1	OUTHI	0x0	RW	This bit is the vcompout high interrupt.
0	OUTLOW	0x0	RW	This bit is the vcompout low interrupt.

16.2.2.6 INTCLR Register

Voltage Comparator Interrupt registers: Clear

OFFSET: 0x00000208

INSTANCE 0 ADDRESS: 0x4000C208

Write a 1 to a bit in this register to clear the interrupt status associated with that bit.

Table 766: INTCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														OUTHI	OUTLOW

Table 767: INTCLR Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	This bitfield is reserved for future use.
1	OUTHI	0x0	RW	This bit is the vcompout high interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 767: INTCLR Register Bits

Bit	Name	Reset	RW	Description
0	OUTLOW	0x0	RW	This bit is the vcompout low interrupt.

16.2.2.7 INTSET Register

Voltage Comparator Interrupt registers: Set

OFFSET: 0x0000020C

INSTANCE 0 ADDRESS: 0x4000C20C

Write a 1 to a bit in this register to instantly generate an interrupt from this module. (Generally used for testing purposes).

Table 768: INTSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD																														OUTHI	OUTLOW

Table 769: INTSET Register Bits

Bit	Name	Reset	RW	Description
31:2	RSVD	0x0	RO	This bitfield is reserved for future use.
1	OUTHI	0x0	RW	This bit is the vcompout high interrupt.
0	OUTLOW	0x0	RW	This bit is the vcompout low interrupt.

©2017 Ambiq Micro, Inc.
All rights reserved.

17. Voltage Regulator Module

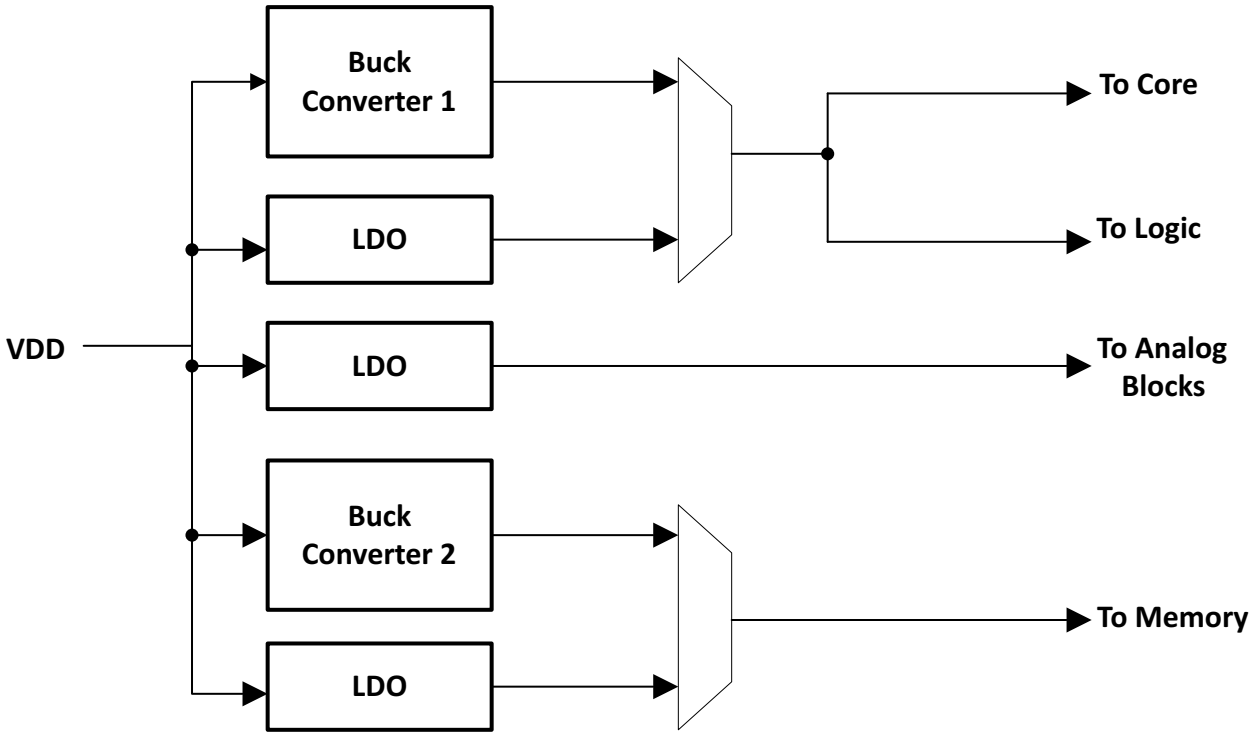


Figure 73. Block Diagram for the Voltage Regulator Module

17.1 Functional Overview

The Voltage Regulator Module down-converts and regulates the supply voltage, VDD, with extremely high efficiency. A pair of Buck Converters enables down-conversion from the power supply input (e.g., a battery) at efficiency of >90%. With ultra-low quiescent current, the Buck Converters are optimized for low power environments. There are also integrated low dropout linear regulators which are used in very low power modes and can also be utilized to provide a lower cost system solution by eliminating the need for the external capacitors/inductors required in buck mode.

The Buck Converters and LDOs of the Voltage Regulator Module are tightly coupled to the various low power modes in the Apollo2 Blue. When the Apollo2 Blue enters deep sleep mode, the Buck Converters can be optionally powered down and bypassed, and the LDOs can be placed in an extreme low power mode with only nanoamps of quiescent current.

Consult the Power Control (PWRCTRL) and MCU Control (MCUCTRL) registers in the MCU Core Details chapter for control and status of the LDOs and Buck Converters.

©2017 Ambiq Micro, Inc.
All rights reserved.

18. Electrical Characteristics

For all tables T_A = -40ºC to 85ºC, Typical values at 25ºC, 1.8v, unless otherwise specified.

18.1 Absolute Maximum Ratings

The absolute maximum ratings are the limits to which the device can be subjected without permanently damaging the device and are stress ratings only. Device reliability may be adversely affected by exposure to absolute-maximum ratings for extended periods. Functional operation of the device at the absolute maximum ratings or any other conditions beyond the recommended operating conditions is not implied.

Table 771: Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{DDP}	Pad supply voltage		-	3.60	V
V_{DDH}	Digital supply voltage		-	3.60	V
V_{DDA}	Analog supply voltage		-	3.60	V
VIO	GPIO supply voltage for BLE sub-system			3.60	V
VCC	Analog supply voltage for BLE sub-system		-	3.60	V
VBAT1	DCDC supply voltage for BLE sub-system		-	3.60	V
VBAT2	Power management supply voltage for BLE sub-system		-	3.60	V
V_{INPUT}	Voltage on any input pin		0	V_{DDP}	V
I_{SRC_STD}	Standard output pin source continuous current		-	16	mA
I_{SINK_STD}	Standard output pin sink continuous current		-	16	mA
I_{HSC_PWR}	High side power switch continuous source current(1)		-	50	mA
I_{HSP_PWR}	High side power switch pulsed source current(1)	10 ms pulse, 1% duty cycle	-	150	mA
I_{LSC_PWR}	Low side power switch continuous sink current(2)		-	50	mA
I_{LSP_PWR}	Low side power switch pulsed sink current(2)	10 ms pulse, 1% duty cycle		150	mA
T_S	Storage temperature		-55	125	ºC
T_J	Junction temperature		-40	85	ºC
T_{OP}	Operating temperature		-40	85	ºC
θ_{JA}	Thermal resistance, junction to ambient	BGA Package on 4 layer PCB in still air, 3mW power dissipation		76.2	ºC/W
θ_{JC}	Thermal resistance, junction to package case	BGA Package on 4 layer PCB in still air, 3mW power dissipation		17.0	ºC/W
T_{REFLOW}	Reflow temperature	Reflow Profile per JEDEC J-STD-020D.1		260	ºC
I_{LU}	Latch-up current			10	mA
V_{ESDHBM}	ESD Human Body Model (HBM)			2500	V

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 771: Absolute Maximum Ratings

V_{ESDCDM}	ESD Charged Device Model (CDM)			500	V

(1) High side power switches are available on PAD22 and PAD41

(2) A low side power switch is available on PAD4

©2017 Ambiq Micro, Inc.
All rights reserved.

18.2 Recommended Operating Conditions

Table 772: Recommended Operating Conditions[1]

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDP}	Pad supply voltage	1.755	-	3.60	V
V_{DDH}	Digital supply voltage	1.755	-	3.60	V
V_{DDA}	Analog supply voltage	1.755	-	3.60	V
VIO	GPIO supply voltage for BLE sub-system	-		3.60[2]	V
VCC	Analog supply voltage for BLE sub-system	1.755	-	3.60	V
VBAT1	DCDC supply voltage for BLE sub-system	1.755	-	3.60	V
VBAT2	Power management supply voltage for BLE sub-system	1.755	-	3.60	V
V_{INPUT}	Voltage on any input pin	0		V_{DDH}/VIO	V
V_{OPLV_32K}	VDDH voltage (below BODL) for RTC and STIMER operation from the 32kHz crystal clock	1.2			V
V_{OPLV_LFRC}	VDDH voltage (below BODL) for RTC and STIMER operation from the LFRC clock	1.2			V
V_{OPLV_RET}	VDDH voltage (below BODL) for retention of RTC and CLKGEN registers, IOS LRAM, and STIMER SNVR0-2 registers	1.2			V
T_A	Ambient operating temperature	-40	-	85	ºC
F_{HFRC}	High Frequency RC oscillator frequency (HFRC)	-	48	-	MHz
F_{LFRC}	Low Frequency RC oscillator frequency (LFRC)	-	1.024	-	kHz
F_{XTAL}	Crystal frequency	-	32.768	-	kHz

1. $V_{DD} = V_{DDP} = V_{DDA} = V_{DDH} = VIO$
2. VIO supply for the BLE sub-system and the Apollo2 VDDH supply must be at the same voltage

18.3 Current Consumption

Table 773: Current Consumption

Symbol	Parameter	Test Conditions[1,2]	VDD	Min	Typ	Max	Unit
I_{RUNFB}	Flash program run current, bucks enabled	Executing CoreMark from internal flash memory, cache enabled, HFRC = 48 MHz, all peripherals disabled, buck converters enabled, 8K SRAM, FLASH1 off	3.3 V	-	14.5	-	µA/MHz
			1.8 V	-	24.0	-	µA/MHz
I_{RUNF}	Flash program run current	Executing CoreMark from internal flash memory, cache enabled, HFRC = 48 MHz, all peripherals disabled, buck converters disabled, 8K SRAM, FLASH1 off	3.3 V	-	46.4	-	µA/MHz
			1.8 V	-	46.5	-	µA/MHz
$I_{RUNFNCB}$	Flash program run current, no cache	Executing CoreMark from internal flash memory, cache disabled, HFRC = 48 MHz, all peripherals disabled, buck converters enabled, 8K SRAM, FLASH1 off	3.3 V	-	13.6	-	µA/MHz
			1.8 V	-	21.5	-	µA/MHz
I_{RUNFNC}	Flash program run current, no cache	Executing CoreMark from internal flash memory, cache disabled, HFRC = 48 MHz, all peripherals disabled, buck converters disabled, 8K SRAM, FLASH1 off	3.3 V	-	40.9	-	µA/MHz
			1.8 V	-	40.9	-	µA/MHz

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 773: Current Consumption

Symbol	Parameter	Test Conditions[1,2]	VDD	Min	Typ	Max	Unit
I_{RUNFSB}	SRAM program run current	Executing CoreMark from internal SRAM memory, HFRC = 48 MHz, all peripherals disabled, buck converters enabled, 8K SRAM, FLASH1 off	3.3 V	-	14.7	-	µA/MHz
			1.8 V	-	24.6	-	µA/MHz
I_{RUNFS}	SRAM program run current	Executing CoreMark from internal SRAM memory, HFRC = 48 MHz, all peripherals disabled, buck converters disabled, 64K SRAM, FLASH1 off	3.3 V	-	41.5	-	µA/MHz
			1.8 V	-	41.3	-	µA/MHz
I_{RUNPNB}	Flash program run current	Executing prime number calculator, buck converters enabled, all Flash/SRAM on	3.3 V	-	9.6	-	µA/MHz
			1.8 V	-	16.4	-	µA/MHz
I_{SS1}	Sleep mode 1 current	WFI instruction with SLEEP = 1, clocks gated, osc's ON, all power domains active idle, 8K SRAM	3.3 V	-	105	-	µA
			1.8 V	-	130	-	µA
$I_{DS2-256RET}$	System Deep Sleep mode 2 w/ full SRAM retention current	WFI instruction with SLEEPDEEP = 1, 256KB SRAM retained, registers retained, cache retained, XTAL running	3.3 V	-	6.4	-	µA
			1.8 V	-	5.7	-	µA
I_{DS2}	Deep sleep mode 2 current	WFI instruction with SLEEPDEEP = 1, 8kB SRAM retained, registers retained, cache retained, XTAL running	3.3 V	-	3.2	-	µA
			1.8 V	-	2.6	-	µA
I_{DS3}	Deep sleep mode 3 current	WFI instruction with SLEEPDEEP = 1, no SRAM/cache retained, XTAL/HFRC off	3.3 V	-	2.9	-	µA
			1.8 V	-	2.3	-	µA
ADC Operating Current[3]							
$I_{ADC_RUN_LPM0}$	ADC run mode low power mode 0	Average run current (LPMODE0: max conversion rate, single slot, 14-bit, CPU in deep sleep otherwise with 16kB SRAM and cache in retention. ADC / gated domains ON. All other IO domains OFF	3.3 V		795		µA
$I_{ADC_RUN_LPM1}$	ADC run mode low power mode 1	Average run current (LPMODE1: 1kHz sample period, single slot, 14-bit, CPU in deep sleep otherwise with 16kB SRAM and cache in retention, main ADC power domain ON. HW controlled ADC gated domain duty cycled between samples.	3.3 V		61		µA
$I_{ADC_RUN_LPM2}$	ADC run mode low power mode 2	Average run current (LPMODE2: 10Hz sample period, single slot, 14-bit, CPU in deep sleep otherwise with 16kB SRAM and cache in retention, main ADC power domain duty cycled by software with calibration each sample conversion	3.3 V		17		µA
Flash Memory Operating Current							
$I_{PROGRAM}$	Supply current during a page program	Buck Mode	3.3 V		1.8		mA
			1.8 V		1.3		mA
$I_{PROGRAM}$	Supply current during a page program	LDO Mode	3.3 V		4.1		mA
			1.8 V		3.9		mA
I_{ERASE}	Supply current during a page erase	Buck Mode	3.3 V		1.1		mA
			1.8 V		0.73		mA

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 773: Current Consumption

Symbol	Parameter	Test Conditions[1,2]	VDD	Min	Typ	Max	Unit
I_{ERASE}	Supply current during a page erase	LDO Mode	3.3 V		3.4		mA
			1.8 V		3.3		mA
$I_{MASSERASE}$	Supply current during a mass erase	Buck Mode	3.3 V		1.1		mA
			1.8 V		0.72		mA
$I_{MASSERASE}$	Supply current during a mass erase	LDO Mode	3.3 V		3.4		mA
			1.8 V		3.3		mA

1. Core clock (HCLK) is 48 MHz for each parameter unless otherwise noted.
2. All values measured at 25°C
3. Base SoC power state is S_{DS2} with minimal SRAM retention. Current represents total current at battery.

18.4 Power Mode Transitions

Table 774: Power Mode Transitions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Buck mode						
$T_{RUN_TO_SLEEP}$	Run to Sleep mode transition time	HCLK frequency = 48 MHz	-	2/ F_{HFRC}	TBD	ns
$T_{RUN_TO_DEEPSLEEP}$	Run mode to Deep Sleep mode transition time	HCLK frequency = 48 MHz	-	11.6	12.5	µs
$T_{SLEEP_TO_RUN}$	Sleep to Run mode transition time		-	1.9	2.1	µs
$T_{DEEPSLEEP_TO_RUN}$	Deep-Sleep to Run mode transition time		-	24.5	25.5	µs
LDO mode						
$T_{RUN_TO_SLEEP}$	Run to Sleep mode transition time	HCLK frequency = 48 MHz	-	2/ F_{HFRC}	TBD	ns
$T_{RUN_TO_DEEPSLEEP}$	Run mode to Deep Sleep mode transition time	HCLK frequency = 48 MHz	-	11.5	12.5	µs
$T_{SLEEP_TO_RUN}$	Sleep to Run mode transition time		-	1.9	2.1	µs
$T_{DEEPSLEEP_TO_RUN}$	Deep-Sleep to Run mode transition time		-	16.5	17.5	µs

18.5 Clocks/Oscillators

Table 775: Clocks/Oscillators

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{HFRC}	HFRC frequency		46.5	48	49.5	MHz
F_{LFRC}	LFRC frequency		840	1024	1114	Hz
F_{XT}	XT frequency		-	32.768	-	kHz

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 775: Clocks/Oscillators

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{RTC}	RTC frequency		-	100	-	Hz
T_{J_LFRC}	LFRC RMS jitter	25ºC, STDEV of period	-	3	13.5	µs
T_{J_XT}	32.768kHz crystal oscillator clock output jitter	At 25°C using a 32.768kHz tuning fork crystal, 7pF load caps on XI and XO, XTALBIASTRIM = 0	-	20	50	ns
DC_{HFRC}	HFRC duty cycle			50		%
DC_{LFRC}	LFRC duty cycle on CLKOUT	CLKGEN_CLKOUT_CKSEL = LFRC_DIV2		50		%
DC_{XT}	32.768kHz crystal oscillator clock output mean duty cycle	At 25°C using a 32.768kHz tuning fork crystal, 7pF load caps on XI and XO, XTALBIASTRIM = 24	-	42	-	%
C_{INT_XT}	Internal XI/XO pin capacitance			2.5		pF
$C_{EXT_XT_TOL}$	Allowed external XI/XO pin capacitance per pin		-	-	7	pF
F_{OF_XT}	XT oscillator failure detection frequency	LFRC @ 1024Hz, over 32ms sample period		8		kHz
OA_{XT}	XT oscillation allowance	At 25°C using a 32.768kHz tuning fork crystal, no external crystal load caps on XI and X0, XTALBIASTRIM = -25	400	-	-	kΩ
OA_{XT7}	XT oscillation allowance, 7pF load	At 25°C using a 32.768kHz tuning fork crystal, 7pF load caps on XI and XO, XTALBIASTRIM = 14	400	-	-	kΩ

©2017 Ambiq Micro, Inc.
All rights reserved.

18.6 Analog-to-Digital Converter (ADC)

Table 776: Analog to Digital Converter (ADC)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ANALOG INPUT						
V_{ADCIN}	Input voltage range single-ended input		0		V_{ADCREF}	V
V_{ADCIN_DIFF}	Input voltage range in differential mode		$-V_{ADCREF}/2$		$+V_{ADCREF}/2$	V
V_{ADCINN} V_{ADCINP}	Absolute differential input voltage range		0		VDDH	V
V_{ADCREF_15E}	External reference voltage range (1.5v mode)		1.425	1.5	1.575	V
V_{ADCREF_20E}	External reference voltage range (2.0v mode)		1.9	2.0	2.1	V
V_{ADCREF_15I}	Internal reference voltage range (1.5v mode)		1.475	1.5	1.525	V
V_{ADCREF_20I}	Internal reference voltage range (2.0v mode)		1.975	2.0	2.025	V
I_{ADCIN}	ADC channel pin input leakage current (static)	GPIO 16 measured at 85 C, TTT part, 2.05 V; 2 V on pad; 10.8 nA with 3.63 or 1.8 V on VDD and pad	-	.5	50	nA
C_{ADCIN}	Input source capacitance			4		pF
$C_{ADCVREF}$	External ADC capacitance for internal reference		400	470	540	nF
SAMPLING DYNAMICS						
RES	Resolution		8		14	bit
F_{ADCONV}	Conversion rate			1.2 (14b) 1.7(12b) 2.4(10b) 2.8 (8b)		MS/s
$T_{TRIG_TO_START_L2}$	Delay from trigger to start of conversion – LPM2, Slot 0			TBD		µs
$T_{TRIG_TO_START_L1}$	Delay from trigger to start of conversion – LPM1, Slot 0, warm start			TBD		µs
$T_{TRIG_TO_START_L0}$	Delay from trigger to start of conversion – LPM0, Slot 0, warm start			TBD		µs
$T_{TRIG_TO_START_L1_CS}$	Delay from trigger to start of conversion – LPM1, Slot 0, cold start			TBD		µs
$T_{TRIG_TO_START_L0_CS}$	Delay from trigger to start of conversion – LPM0, Slot 0, cold start			TBD		µs
T_{CAL}	Calibration Period			6415		cycles
DYNAMIC CHARACTERISTICS, External 2v Reference, LDO or Buck Mode						

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 776: Analog to Digital Converter (ADC)

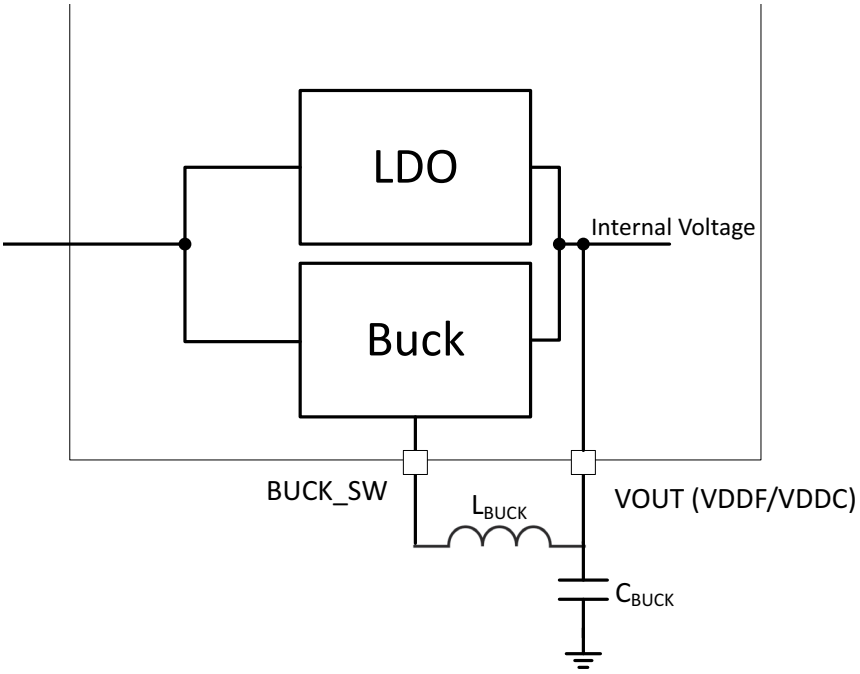
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$ENOB_{CAL}$	Calibrated ENOB	Single/Diff. Ended Input, external 2 V ref, 1 kHz input, ADC running in 14-bit mode	10.3	10.9		ENOB
$ENOB_{UNCAL}$	Uncalibrated ENOB	Single/Diff. Ended Input, external 2 V ref, 1 kHz input, ADC running in 14-bit mode		8.9(10b) 7.8(8b)		ENOB
THD_{ADC}	Total harmonic distortion (THD)	Single/Diff. Ended Input, external 2 V ref, 1 kHz input, ADC running in 14-bit mode,1st 7 harmonics		-80.4	-71.7	dB
SNR_{ADC}	Signal-to-noise ratio (SNR)	Single/Diff. Ended Input, external 2 V ref, 1 kHz input, ADC running in 14-bit mode	64.1	68		dB
$SFDR_{ADC}$	Spurious-free dynamic range (SFDR)	Single/Diff. Ended Input, external 2 V ref, 1 kHz input, ADC running in 14-bit mode	78.55	85.9		dB
$SINAD_{ADC}$	Signal-to-noise and distortion ratio (SINAD)	Single/Diff. Ended Input, external 2 V ref, 1 kHz input, ADC running in 14-bit mode	64.04	67.7		dB
PERFORMANCE						
NMC_{ADC}	No missing codes			14		bits
INL_{ADC}	Integral nonlinearity	Full input range		+/- 2.4	+/- 3.5	LSB
DNL_{ADC}	Differential nonlinearity	Full input range		+/- 0.9	+/- 1.7	LSB
E_{ADC_OFFEST}	Offset error		1		1	%FS
E_{ADC_GAIN}	Gain error				1	%FS
INTERNAL TEMPERATURE SENSOR						
E_{TEMP}	Temperature sensor accuracy			+/- 3		°C
S_{TEMP}	Temperature sensor slope			3.8		mV/°C
BATTERY RESISTANCE						
R_{BATT}	Internal resistance for Battery Measurement		487.32	524	560.68	Ω
$V_{BATTDIV}$	Battery divider voltage		-2.5%	0.333 * V_{DDH}	+1.5%	V

©2017 Ambiq Micro, Inc.
All rights reserved.

18.7 Buck Converter

Table 777: Buck Converter

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
L_{BUCK}	Buck converter inductance (V_{DDC}, V_{DDF})			2.2		µH
C_{BUCK}	Buck converter output capacitance (V_{DDC}, V_{DDF})			1		µF
V_{VDDC}	VDDC output voltage			695		mV
V_{VDDF}	VDDF output voltage			945		mV
C_{LOAD}	Load capacitance		0.8	1	1.2	µF



18.8 Power-On RESET (POR) and Brown-Out Detector (BOD)

Table 778: Power-On Reset (POR) and Brown-Out Detector (BOD)

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR_RISING}	POR rising threshold voltage	1.62	1.72	1.755	V
$V_{POR_FALLING}$	POR falling threshold voltage	1.62	1.69	1.754	V
V_{BODH_RISING}	BODH rising threshold voltage	2.27		2.42	v
$V_{BODH_FALLING}$	Brown-out falling threshold voltage	2.12		2.28	v
T_{FALL_SLEW}	Maximum VDDH falling slew rate for BODL trigger			2.5	V/ms
T_{RESPR}	Response Time - Rise		10		µs
T_{RESPF}	Response Time - Fall			15	µs

©2017 Ambiq Micro, Inc.
All rights reserved.

18.9 Resets

Table 779: Resets

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{RST}	nRST pulse width to guarantee reset assertion	2KV/s supply slew rate	400			ns
T_{POR}	POR detect to nRST deassertion delay	2KV/s supply slew rate	30	34	50	ms
$T_{POR2HRST}$	Delay from nRST deassertion to HRESET deassertion	2KV/s supply slew rate	12		24	ms
T_{RSTDLY}	nRST reset delay from internal BODL	2KV/s supply slew rate		12		µs
T_{SOFT}	Software initiated reset delay	2KV/s supply slew rate		11		ms

18.10 Voltage Comparator (VCOMP)

Table 780: Voltage Comparator (VCOMP)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{COMPIN}	Input voltage range		0		V_{DDA}	V
V_{COMPIN_OV}	Input offset voltage			60		mV
I_{COMPIN_LEAK}	Input leakage current	GPIO 16 measured at 85 C, TTT part, 3.63 V; 3.63 V on pad; also at 1.8 V and 1.8 V	-	.5	50	nA
T_{COMP_RTRIG}	Rising voltage trigger response time			3	30	µs
T_{COMP_FTRIG}	Falling voltage trigger response time			8	50	µs
V_{HYST}	Hysteresis		35		110	mV

©2017 Ambiq Micro, Inc.
All rights reserved.

18.11 Inter-Integrated Circuit (I^2C) Interface

Table 781: Inter-Integrated Circuit (I^2C) Interface

Symbol	Parameter	Test Conditions	VCC	Min	Typ	Max	Unit
f_{SCL}	SCL input clock frequency		1.7 V - 3.6 V	10		1000	kHz
t_{LOW}	Low period of SCL clock	f_{SCL} = 400 kHz (Fast Mode)	1.7 V - 3.6 V	1.3			µs
t_{HIGH}	High period of SCL clock	f_{SCL} = 400 kHz (Fast Mode)	1.7 V - 3.6 V	600			ns
t_{RISE}	Rise time of SDA and SCL	f_{SCL} = 400 kHz (Fast Mode)	1.7 V - 3.6 V			300	ns
t_{FALL}	Fall time of SDA and SCL	f_{SCL} = 400 kHz (Fast Mode)	1.7 V - 3.6 V			300	ns
$t_{HD:STA}$	START condition hold time	f_{SCL} = 400 kHz (Fast Mode)	1.7 V - 3.6 V	600			ns
$t_{SU:STA}$	START condition setup time	f_{SCL} = 400 kHz (Fast Mode)	1.7 V - 3.6 V	600			ns
$t_{SU:DAT}$	SDA setup time	f_{SCL} = 400 kHz (Fast Mode)	1.7 V - 3.6 V	100			ns
$t_{HD:DAT}$	SDA hold time	f_{SCL} = 400 kHz (Fast Mode)	1.7 V - 3.6 V	0			ns
$t_{SU:STO}$	STOP condition setup time	f_{SCL} = 400 kHz (Fast Mode)	1.7 V - 3.6 V	600			ns
t_{BUF}	Bus free time before a new transmission	f_{SCL} = 400 kHz (Fast Mode)	1.7 V - 3.6 V	1.3			µs

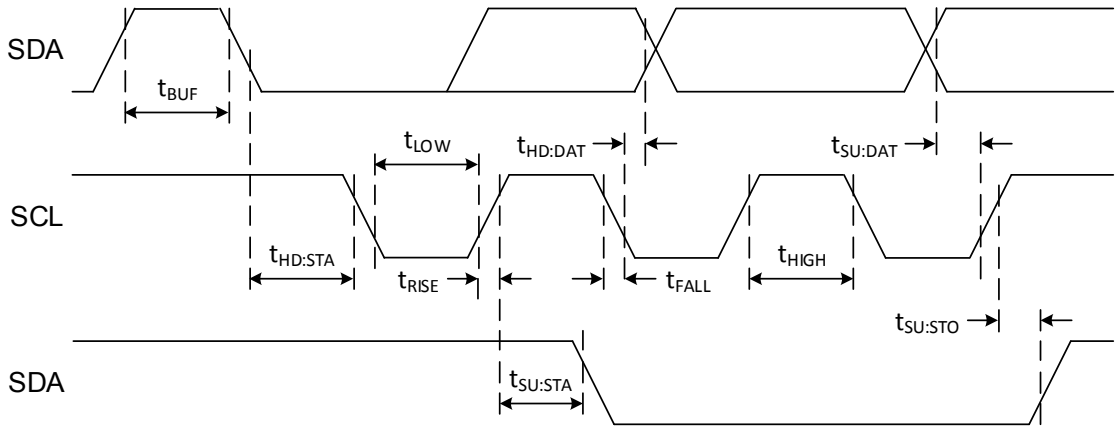


Figure 74. I^2C Timing

©2017 Ambiq Micro, Inc.
All rights reserved.

18.12 Serial Peripheral Interface (SPI) Master Interface (IOM1, 2)

Table 782: Serial Peripheral Interface (SPI) Master Interface

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range	-	8	12	MHz
B_{FIFO}	FIFO size		128		Bytes
T_{SCLK_LO}	Clock low time	$1/2F_{S-CLK(max)}$	1/2 FSCLK	-	s
T_{SCLK_HI}	Clock high time	$1/2F_{S-CLK(max)}$	1/2 FSCLK	-	s
T_{SU_MI}	MISO input data setup time	-	-	-	ns
T_{HD_MI}	MISO input data hold time	-	-	-	ns
T_{HD_MO}	MOSI output data hold time	-	-	-	ns
$T_{VALID,MO}$	MOSI output data valid time	-	-	-	ns

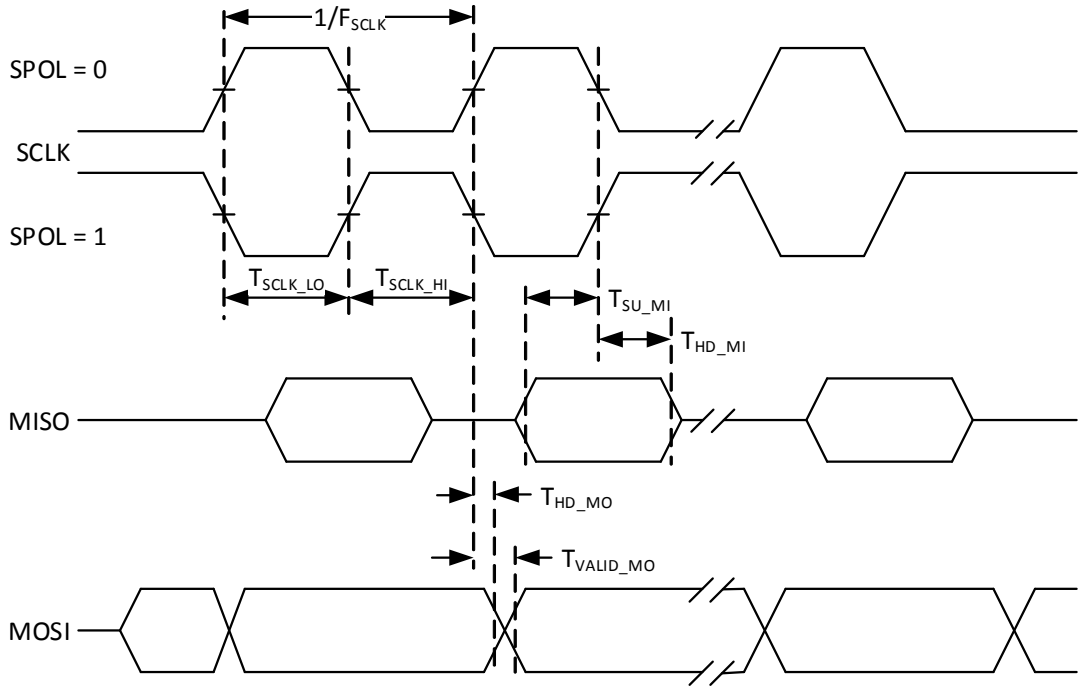


Figure 75. SPI Master Mode, Phase = 0

©2017 Ambiq Micro, Inc.
All rights reserved.

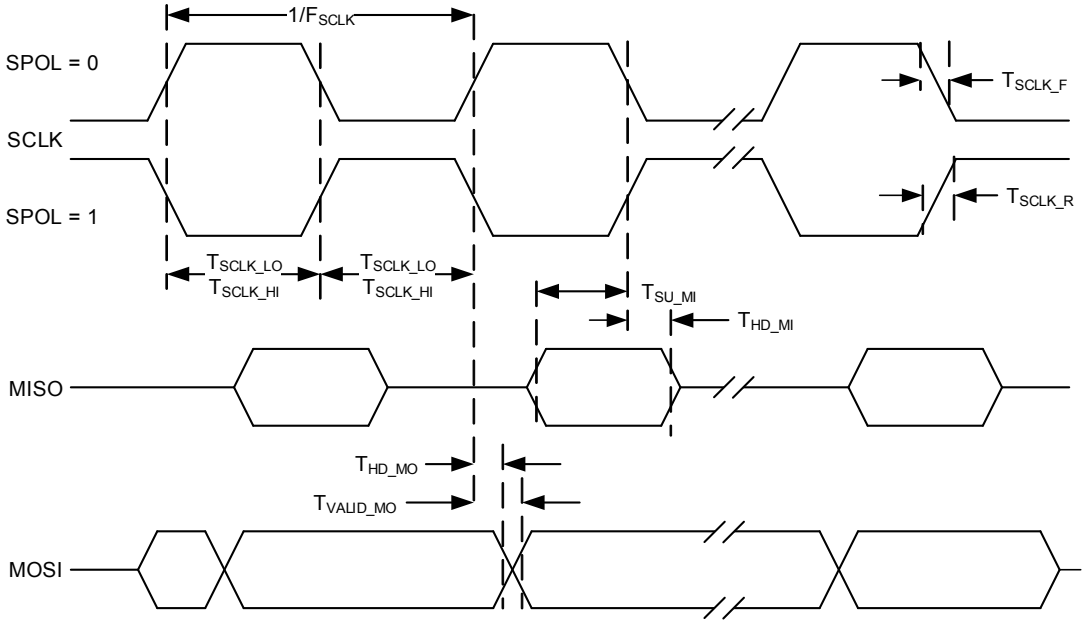


Figure 76. SPI Master Mode, Phase = 1

©2017 Ambiq Micro, Inc.
All rights reserved.

18.13 High Speed Serial Peripheral Interface (SPI) Master Interface (IOM 0, 4)

Table 783: High Speed Serial Peripheral Interface (SPI) Master Interface

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range	-	12	24	MHz
B_{FIFO}	FIFO size		128		Bytes
T_{SCLK_LO}	Clock low time	$1/2F_{S-CLK(max)}$	1/2 FSCLK	-	s
T_{SCLK_HI}	Clock high time	$1/2F_{S-CLK(max)}$	1/2 FSCLK	-	s
T_{SU_MI}	MISO input data setup time	-	-	-	ns
T_{HD_MI}	MISO input data hold time	-	-	-	ns
T_{HD_MO}	MOSI output data hold time	-	-	-	ns
$T_{VALID,MO}$	MOSI output data valid time	-	-	-	ns

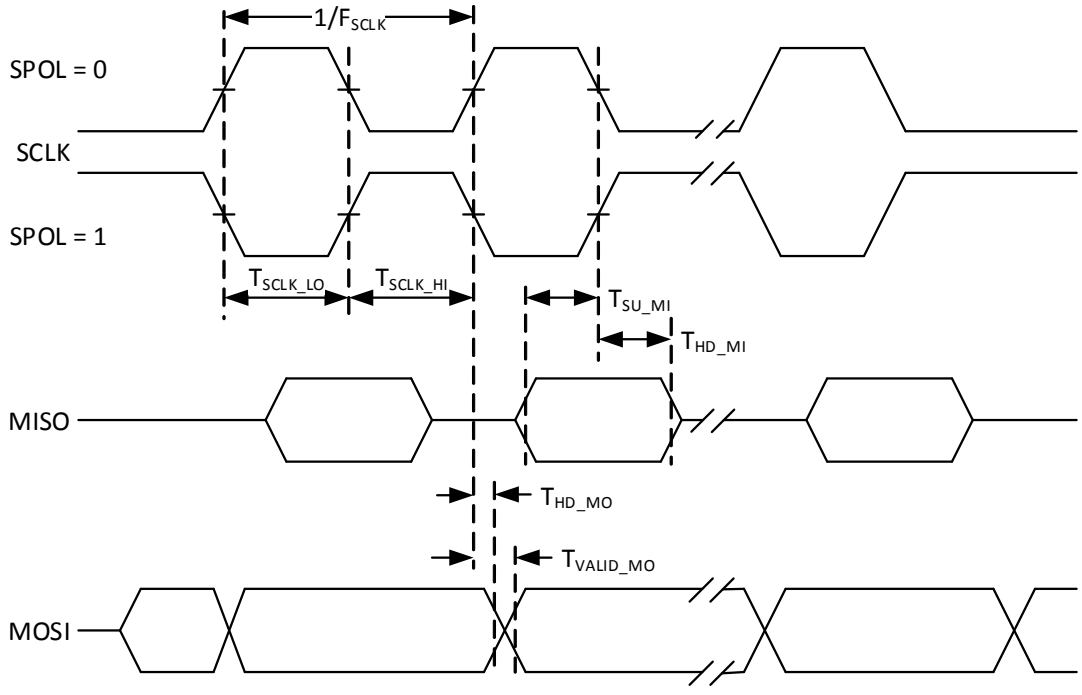


Figure 77. SPI Master Mode, Phase = 0

©2017 Ambiq Micro, Inc.
All rights reserved.

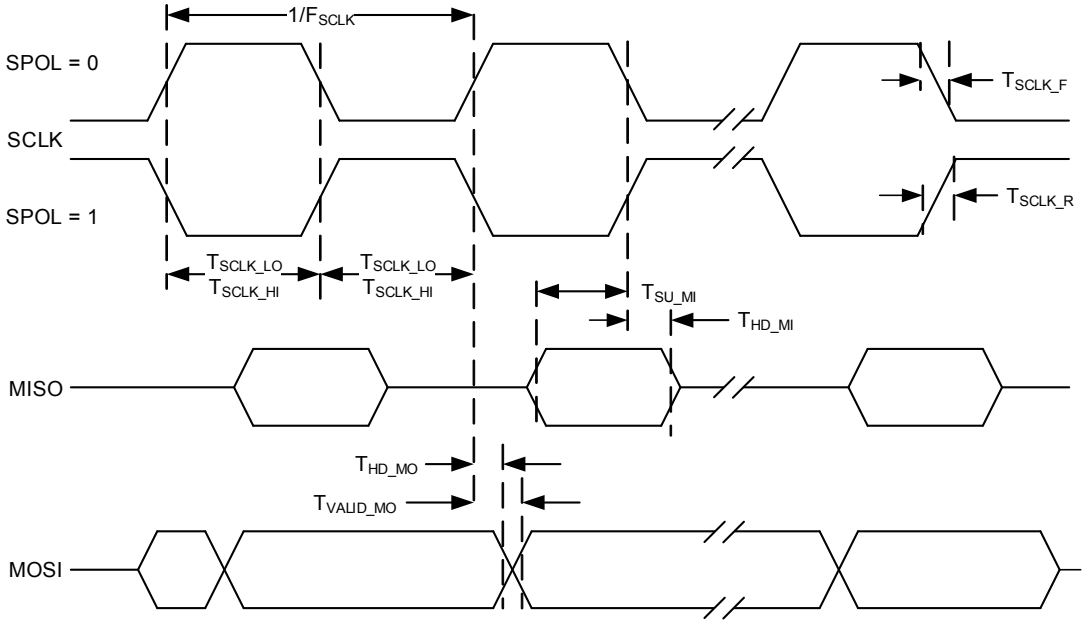


Figure 78. SPI Master Mode, Phase = 1

©2017 Ambiq Micro, Inc.
All rights reserved.

18.14 Serial Peripheral Interface (SPI) Slave Interface

Table 784: Serial Peripheral Interface (SPI) Slave Interface

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range	-	-	12	MHz
B_{FIFO}	FIFO size		128		Bytes
T_{SCLK_LO}	Clock low time	$1/2F_{S-CLK(max)}$	-	-	s
T_{SCLK_HI}	Clock high time	$1/2F_{S-CLK(max)}$	-	-	s
T_{CE_LEAD}	Chip enable low to first SCLK edge	-	-	-	ns
T_{CE_LAG}	Chip enable high to last SCLK edge	-	-	-	ns
T_{CE_SDO}	Chip enable low to MISO data output	-	-	-	ns
T_{CE_SDZ}	Chip enable high to MISO data tri-state	-	-	-	ns
T_{SU_SI}	MOSI input data setup time	-	-	-	ns
T_{HD_SI}	MOSI input data hold time	-	-	-	ns
T_{HD_SO}	MISO output data hold time	-	-	-	ns
$T_{VALID,SO}$	MISO output data valid time	-	-	-	ns

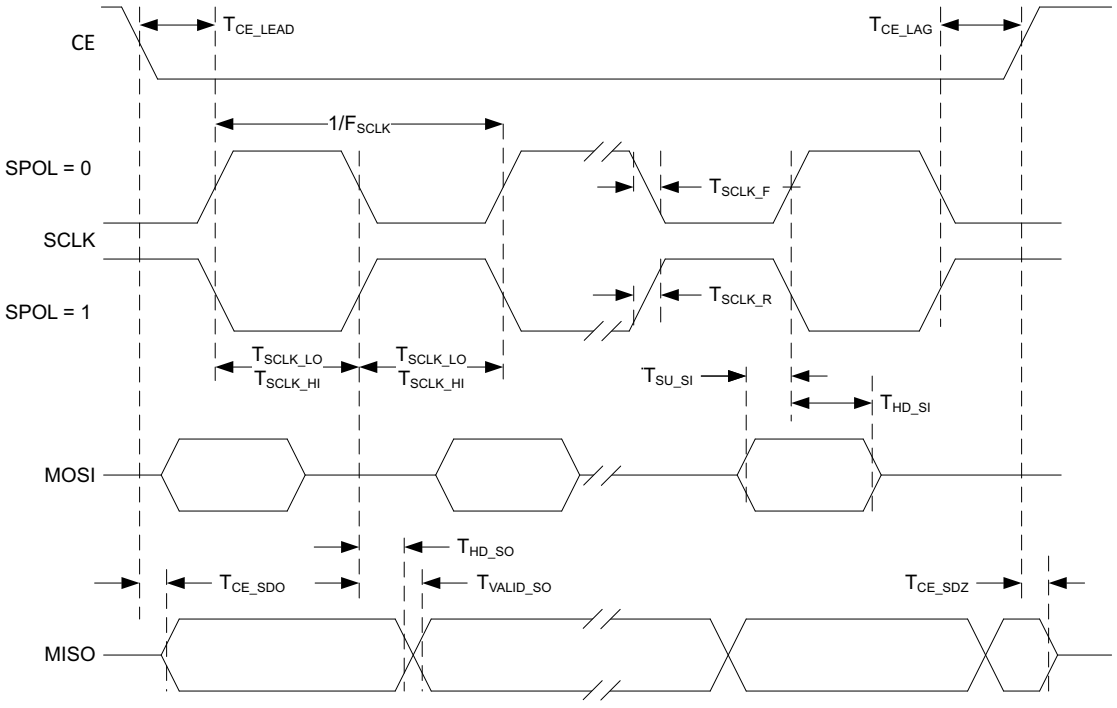


Figure 79. SPI Slave Mode, Phase = 0

©2017 Ambiq Micro, Inc.
All rights reserved.

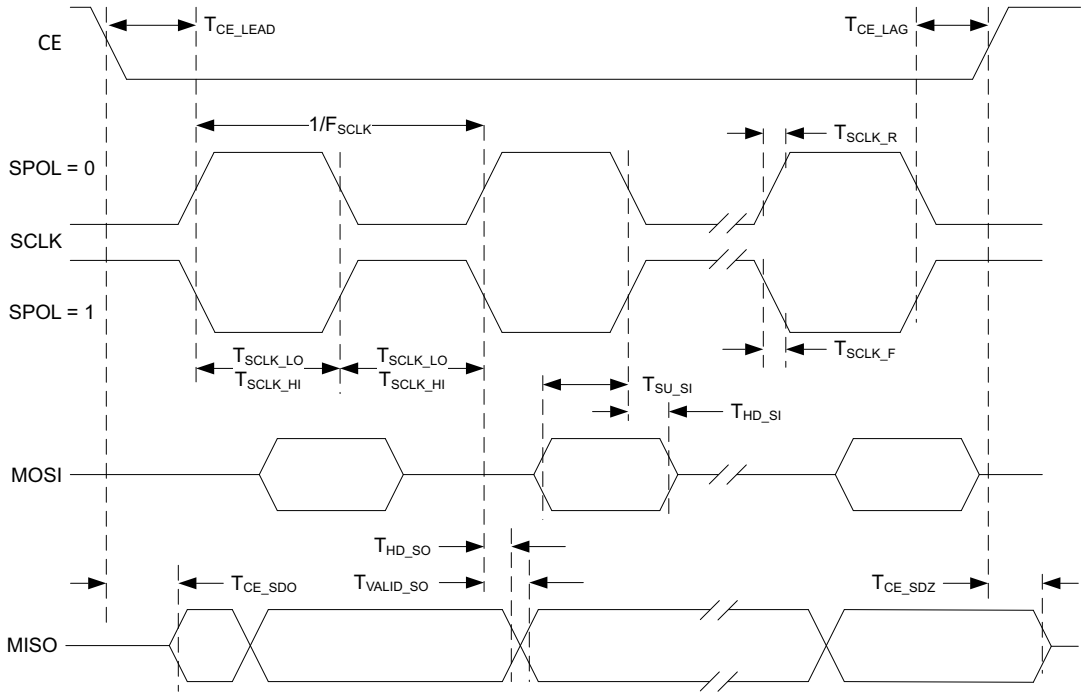


Figure 80. SPI Slave Mode, Phase = 1

©2017 Ambiq Micro, Inc.
All rights reserved.

18.15 PDM Interface

Table 785: Pulse Density Modulation (PDM) Interface

Symbol	Parameter	Test Conditions	VDD	Min	Typ	Max	Unit
F_{PDM_CLK}	PDM output clock frequency		1.755V - 3.63V	0.187	-	12	MHz
DC_{PDMCLK}	PDM clock duty cycle[1]	20pF load, 12mA/4mA drive strength, GPIO12/GPIO37	1.755V - 3.63V	40	-	55	%
J_{PDM_CLK}	PDM clock jitter	20pF load, 12mA drive strength, GPIO12, 3MHz clock freq	1.755V - 3.63V		131	300	ps
T_{PDM_RISE}	PDM clock rise time - 12 mA Drive Strength	20pF load, 12mA drive strength, GPIO12	3.3 V	-	4.6	-	ns
			1.8 V	-	5.3	-	ns
T_{PDM_RISE}	PDM clock rise time - 4 mA Drive Strength	20pF load, 4mA drive strength, GPIO30 & GPIO37	3.3 V	-	5.2	-	ns
			1.8 V	-	6.4	-	ns
T_{PDM_FALL}	PDM clock fall time - 12 mA Drive Strength	20pF load, 12mA drive strength, GPIO12	3.3 V	-	4.7	-	ns
			1.8 V	-	5.4	-	ns
T_{PDM_FALL}	PDM clock fall time - 4 mA Drive Strength	20pF load, 4mA drive strength, GPIO30 & GPIO37	3.3 V	-	5.6	-	ns
			1.8 V	-	7.3	-	ns
T_{SU_PDM}	PDM input data setup time			-	-	TBD	ns
T_{HD_PDM}	PDM input data hold time			TBD	-	-	ns

1. Applicable when F_{PDMCLK} <= 2.4 MHz and PDM_PCFG_MCLKDIV set to MCKDIV1, MCKDIV2 or MCKDIV4 only. PDM_PCFG_MCLKDIV setting of MCKDIV3 has a duty cycle of 67%.

18.16I2S Interface

Table 786: Inter-Integrated Serial (I2S) Interface

Symbol	Parameter	Test Conditions	VDD	Min	Typ	Max	Unit
F_{BCLK}	I2S input BCLK frequency range		1.755V - 3.63V	0.187	-	12	MHz
F_{WDCLK}	I2S input WDCLK frequency range		1.755V - 3.63V	11.7	-	750	kHz
DC_{BCLK}	I2S BCLK duty cycle		1.755V - 3.63V	40	-	60	%
DC_{WDCLK}	I2S WDCLK duty cycle		1.755V - 3.63V	40	-	60	%
T_{I2S_RISE}	I2S clock and data rise time	20pF load, 4mA drive strength, GPIO30	3.3V	-	5.4-		ns
			1.8V	-	6.8		ns
T_{I2S_FALL}	I2S clock and data fall time	20pF load, 4mA drive strength, GPIO30	3.3V	-	5.6		ns
			1.8V	-	7.6		ns
T_{SU_I2S}	I2S input data setup time			-	-	TBD	ns
T_{HD_I2S}	I2S input data hold time			TBD	-	-	ns

©2017 Ambiq Micro, Inc.
All rights reserved.

18.17 Universal Asynchronous Receiver/Transmitter (UART)

Table 787: Universal Asynchronous Receiver/Transmitter (UART)

Symbol	Parameter	Min	Typ	Max	Unit
F_{BAUD}	UART baud rate		-	921600	bps

18.18 Counter/Timer (CTIMER)

Table 788: Counter/Timer (CTIMER)

Symbol	Parameter	Min	Typ	Max	Unit
F_{CTIMER}	Input frequency	-	-	24	MHz
T_{CTIMER}	Capture pulse width	50	-	-	ns

18.19 System Timer (STIMER)

Table 789: System Timer (WDT)

Symbol	Parameter	Min	Typ	Max	Unit
F_{STIMER}	Input frequency	-	-	$F_{HFRC}/16$	MHz
T_{STIMER}	Capture pulse width to trigger an interrupt	50	-	-	ns

18.20 Watchdog Timer (WDT)

Table 790: Watchdog Timer (WDT)

Symbol	Parameter	Min	Typ	Max	Unit
T_{WD}	Watchdog timer resolution	.0625	128	128	Hz

©2017 Ambiq Micro, Inc.
All rights reserved.

18.21 Flash Memory

Table 791: Flash Memory

Symbol	Parameter	Min	Typ	Max	Unit
PE_{CYC}	Program/erase cycles before failure	10,000	-	-	cycles
T_{FDR}	Data retention @85C	10	-	-	years
T_{PAGE_ERASE}	Single page erase time (8192 bytes)	10	15	20	ms
T_{MASS_ERASE}	Mass erase time	10	15	20	ms
T_{PAGE_PGM}	Single page program time (8192 bytes)	23	28	33	ms

18.22 General Purpose Input/Output (GPIO)

All GPIOs have Schmitt trigger inputs.

Table 792: General Purpose Input/Output (GPIO)

Symbol	Parameter	Test Conditions	VDD	Min	TYP	Max	Unit
ALL GPIOs							
V_{OH}	High-level output voltage			0.8 * V_{DDH}	-	-	V
V_{OL}	Low-level output voltage			-	-	0.2 * V_{DDH}	V
V_{IH}	Positive going input threshold voltage					0.7 * V_{DDH}	V
V_{IL}	Negative going input threshold voltage			0.3 * V_{DDH}			V
V_{HYS}	Input Hysteresis			0.1 * V_{DDH}		-	V
C_{GPI}	Input capacitance	Pad input capacitance standard GPIO	1.755V - 3.63V	-	2.5	-	pF
R_{PU}	Pull-up resistance			8	35	150	kΩ
R_{PD}	Pull-down resistance			9	20	150	kΩ
$R_{PUI2C00}$	I2C pad pull-up resistance, RSEL = 0x00			1.2	1.4	1.6	kΩ
$R_{PUI2C01}$	I2C pad pull-up resistance, RSEL = 0x01			4	4.5	6	kΩ
$R_{PUI2C10}$	I2C pad pull-up resistance, RSEL = 0x10			8	10	12	kΩ
$R_{PUI2C11}$	I2C pad pull-up resistance, RSEL = 0x11			14	22	32	kΩ

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 792: General Purpose Input/Output (GPIO)

Symbol	Parameter	Test Conditions	VDD	Min	TYP	Max	Unit
I_{IN}	Input pin leakage current	GPIO0 measured at 25 C	1.755V - 3.63V	-	0.13	50	nA
I_{INOD}	Open drain output leakage current	GPIO0 measured at 25 C, TTT part, 3.3 V VDD, 3.3 V pad voltage, GPIO configured as open drain, WTA set to 1	1.755V - 3.63V	-	.1	50	nA
STANDARD GPIOs							
T_{RISE_STD}	Rise time	20pF load, 2mA drive strength, GPIO39	3.3 V	-	7.35	-	ns
			1.8 V	-	14.5	-	ns
T_{RISE_STD}	Rise time	20pF load, 4mA drive strength, GPIO39	3.3 V	-	2.56	-	ns
			1.8 V	-	6.4	-	ns
T_{RISE_STD}	Rise time	20pF load, 8mA drive strength, GPIO39	3.3 V	-	1.66	-	ns
			1.8 V	-	2.4	-	ns
T_{RISE_STD}	Rise time	20pF load, 12mA drive strength, GPIO39	3.3 V	-	1.3	-	ns
			1.8 V	-	1.8	-	ns
T_{FALL_STD}	Fall time	20pF load, 2mA drive strength, GPIO39	3.3 V	-	10.0	-	ns
			1.8 V	-	18.1	-	ns
T_{FALL_STD}	Fall time	20pF load, 4mA drive strength, GPIO39	3.3 V	-	3.61	-	ns
			1.8 V	-	7.6	-	ns
T_{FALL_STD}	Fall time	20pF load, 8mA drive strength, GPIO39	3.3 V	-	1.85	-	ns
			1.8 V	-	3.1	-	ns
T_{FALL_STD}	Fall time	20pF load, 12mA drive strength, GPIO39	3.3 V	-	1.37	-	ns
			1.8 V	-	2.1	-	ns
I_{SRC_STD}	Output source current, 2mA drive strength			-	3.5	-	mA
I_{SNK_STD}	Output sink current, 2mA drive strength			-	3.4	-	mA
I_{SRC_STD}	Output source current, 4mA drive strength			-	7.1	-	mA
I_{SNK_STD}	Output sink current, 4mA drive strength			-	6.8	-	mA
I_{SRC_STD}	Output source current, 8mA drive strength			-	14.1	-	mA
I_{SNK_STD}	Output sink current, 8mA drive strength			-	13.5	-	mA

©2017 Ambiq Micro, Inc.
All rights reserved.

Table 792: General Purpose Input/Output (GPIO)

Symbol	Parameter	Test Conditions	VDD	Min	TYP	Max	Unit
I_{SRC_STD}	Output source current, 12mA drive strength			-	21.1	-	mA
I_{SNK_STD}	Output sink current, 12mA drive strength			-	20.2	-	mA
POWER SWITCH GPIOs							
R_{SRC_PWR}	High side power switch resistance			-	1.5	2.4	Ω
I_{SRC_PWR}	High side power switch source current			-	-	100	mA
$I_{SRC_PWR_LKG}$	High side power switch source leakage current	GPIO4 measured at 85 C, TTT part, 3.63 V; 3.63 V on pad; PC_SEL = 1	1.755V - 3.63V	-	1.3	200	nA
R_{SNK_PWR}	Low side power switch resistance			-	1.8	2.4	Ω
I_{SNK_PWR}	Low side power switch sink current			-	-	100	mA
$I_{SNK_PWR_LKG}$	Low side power switch source leakage current	GPIO22 measured at 85 C, TTT part, 3.63 V; 0 V on pad; PC_SEL = 1 (TYP at 3.3 V w/ 0 V on pad)	1.755V - 3.63V	-	1.7	200	nA

©2017 Ambiq Micro, Inc.
All rights reserved.

18.23 Serial Wire Debug (SWD)

Table 793: Serial Wire Debug (SWD)

Symbol	Parameter	Min	Typ	Max	Unit
T_{SWDCK_HI}	SWDCK clock high period	0.1		500	µs
T_{SWDCK_LO}	SWDCK clock low period	0.1		500	µs
T_{OS_SWD}	SWDIO output skew to falling edge of SWDCLK	0		45	ns
T_{SU_SWD}	Input setup time between SWDIO and rising edge SWDCK	65			ns
T_{HD_SWD}	Input hold time between SWDIO and rising edge SWDCK	125			ns

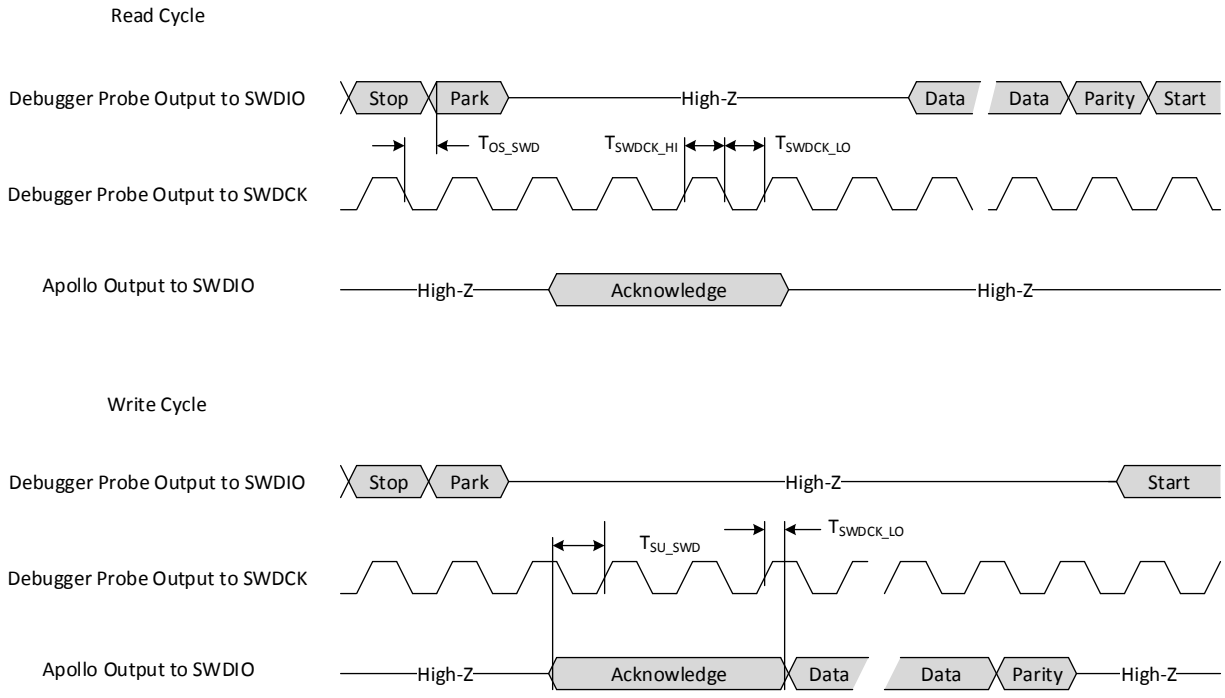


Figure 81. Serial Wire Debug Timing

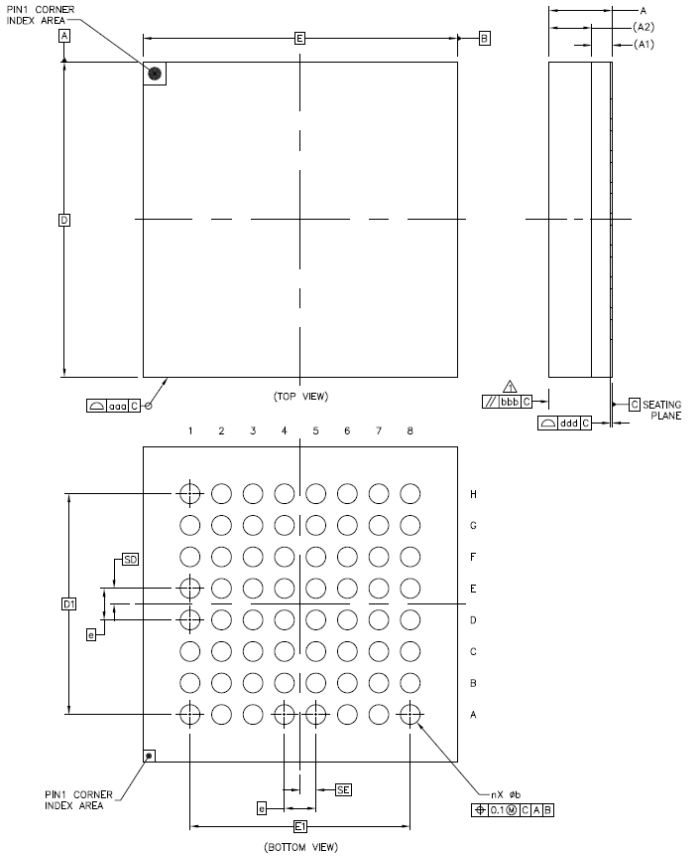
©2017 Ambiq Micro, Inc.
All rights reserved.

19. Package Mechanical Information

19.1 LGA Package

Table 794: Reflow Soldering Requirements (Pb-free assembly)

Profile Feature	Requirement
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (ts) from (T_{smin} to T_{smax})	 150°C 200°C 60-120 seconds
Ramp-up rate (T_L to T_p)	3°C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217°C 60-150 seconds
Peak package body temperature (T_p)	260°C max.
Time (t_p) within 5°C of T_p	30 seconds max.
Ramp-down rate (T_p to T_L)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.9
SUBSTRATE THICKNESS	A1		0.26	REF
MOLD THICKNESS	A2		0.54	REF
BODY SIZE	D		4	BSC
	E		4	BSC
LEAD WIDTH	W	---	---	---
LEAD LENGTH	L	---	---	---
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		64	
EDGE BALL CENTER TO CENTER	D1		2.8	BSC
	E1		2.8	BSC
BODY CENTER TO CONTACT BALL	SD		0.2	BSC
	SE		0.2	BSC
BALL WIDTH		---	---	---
BALL DIAMETER			---	
BALL OPENING	b		0.25	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

NOTES:

⚠ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 82. 4 x 4 x 0.9 mm, 0.4 mm Pitch, 64-lead LGA Package

©2017 Ambiq Micro, Inc.
All rights reserved.

19.2 SMT Assembly Considerations for LGA Package

19.2.1 Solder Paste

The screen printing quantity of solder paste is an key factor in producing high yield assemblies. Recommended solder paste has the following qualities:

- Alloys: 63Sn/37Pb or 62Sn/36Pb/2Ag Sn/Ag/Cu family for lead-free application
- Low residue,no clean flux
- Particle size:
  - Type III (25 ~ 45 µm) or Type IV (25 ~ 38 µm)
  - Type IV is preferred to improved printing performance.

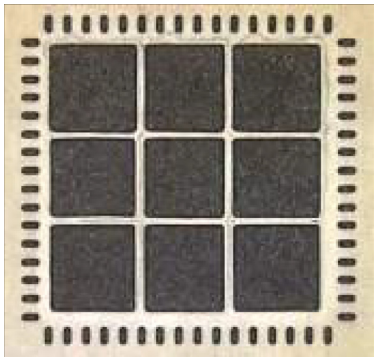
19.2.2 Solder Stencils

The contrast between a large thermal pad and small terminal pads of the LGA can present a challenge in production and even solder line thickness. The precise volume of solder paste deposited onto the device land pattern is controlled by the stencil thickness and the opening geometry. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow-solder processing. The solder joint thickness for LGA terminal pads should be 50 - 75 µm.

The stencil used should have the following characteristics:

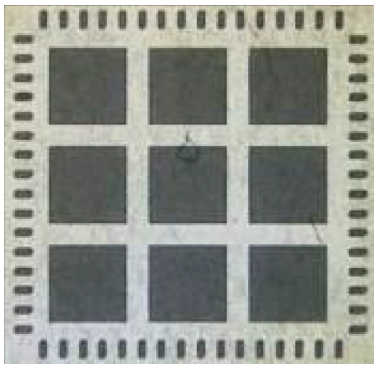
- Stencil Type & Thickness
  - Laser cut
  - Stainless steel
  - Thickness: 100 ~ 150 µm (125 µm as a guide)
  - Actual thickness of a stencil depends on other SMDs on the PCB
- Aperture size and Shape for terminal pad
  - Aspect ratio (width / thickness) > 1.5
  - Area ratio > 0.66 (Area of aperture opening / aperture wall area)
- Aperture shape
  - Typically designed to match the pad size on the PCB 1-to-1
  - Fine pitch components of 0.5 mm and below may require reducing the stencil aperture length by 20%
  - Oval-shaped openings should be used for optimum paste release
  - Rounded corners to minimize clogging
  - Positive taper walls (5° tapering) with bottom opening larger than the top
- Aperture design for thermal pad
  - Small multiple openings should be used instead of one large opening
  - 60% ~ 85% solder paste coverage
  - Rounded corners to minimize clogging
  - Positive taper walls (5° tapering) with bottom opening larger than the top

©2017 Ambiq Micro, Inc.
All rights reserved.



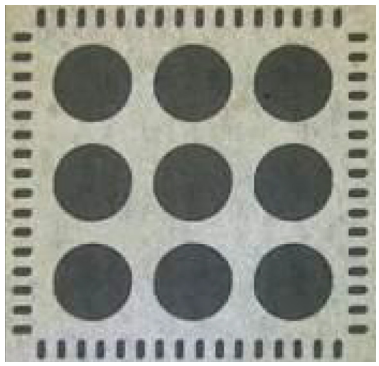
Not recommended

Coverage 91%



Recommended

Coverage 77%



Recommended

Coverage 65%

The squeegee used should have the following characteristics:

- Metal blade
- Polymer with 90° hardness

19.2.3 Package-to-board Assembly

Printing parameters are as follows:

- Metal squeegee with 45° ~ 60° printing angle
- Speed: Start with 20 mm/sec,,increasing with experience
- Printing pressure: 10 N/mm2
- Snap-off distance: 0 mm

For pitch < or = 0.5 mm, 3D post-printing inspection is highly recommended.

The LGA should be placed as follows:

- Use standard pick and place machine with ± 0.05 mm accuracy
- Mount at slower speed and higher force
- Place package 1 ~ 2 mils into the paste
- LGAs have excellent self-alignment during solder reflow if a minimum of 75% of the lead diameter intersects with the pad.

Reflow oven parameters are as follows:

- Forced convection reflow with nitrogen
- Temperature uniformity < or = 5°C

The reflow profile should be the following:

- Follow datasheet of solder paste
- Other concerns: other parts, board density, board thickness

©2017 Ambiq Micro, Inc.
All rights reserved.

- For the PPF leadframe, the palladium will dissolved in the solder and the joint is formed with the underlying nickel layer. Higher reflow temperature is required to form a good solder joint.

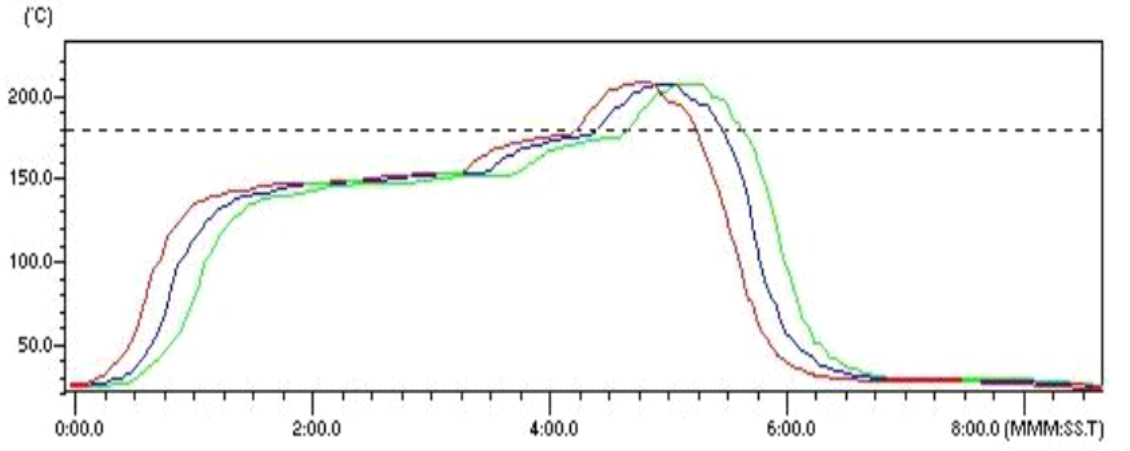


Figure 83. Recommended Reflow Profile for 63/37 Solder Paste or Cu lead frame

This profile is designed for use with Sn63 or Sn62 and can serve as a general guideline in establishing a reflow profile.

- Heating-up @1 ~ 3°C/sec to 140°C
- Preheat @ 140 - 150°C for 120 ~ 160 sec
- Ramp @ 2 ~ 3°C/sec to peak temperature (220 ~ 225°C),
- Temperature over 183°C for 45~ 75 sec
- Cooling down to room temperature @4 ~ 2°C/sec to avoid undesired intermetallic compound layer.

Figure 84 shows the recommended reflow profile fo lead-free paste or PPF lead frame. Inspections are done using transmission X-rays to sample-monitor the solder joint, where side-view inspection is also recommended.

©2017 Ambiq Micro, Inc.
All rights reserved.

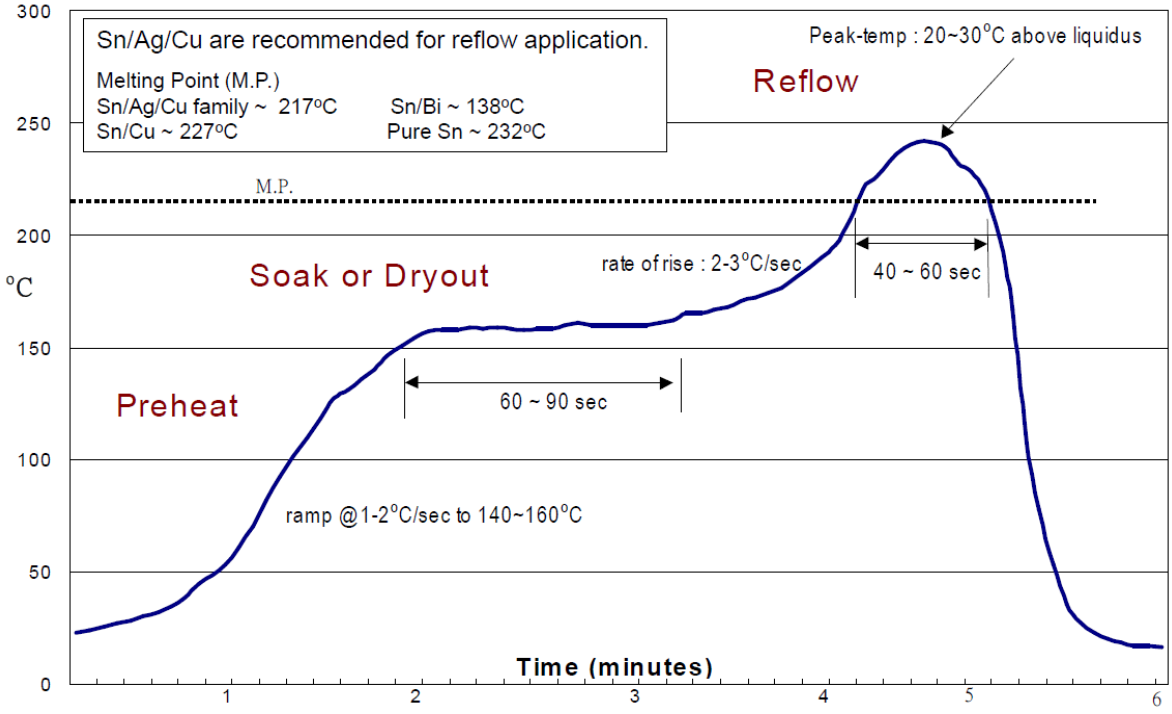


Figure 84. Recommended Reflow Profile for Lead-free Solder Paste or PPF lead frame

©2017 Ambiq Micro, Inc.
All rights reserved.

©2017 Ambiq Micro, Inc.
All rights reserved.

Index

Numerics
10BIT 149
12/24 Hour Mode 357
3-wire mode 152
A
Access permissions 55
accumulation control 451
accumulation, automatic 451
ACK 148, 184
Acknowledge 148
Active Mode 56
ADC 48, 208, 251, 448
ADC Configuration Register 456
ADC Reference Generator 450
ADC_DIV3 449
ADC_EXT0 449
ADC_EXT1 449
ADC_EXT2 449
ADC_EXT6 449
ADC_EXT7 449
ADCREF 251
ADC_SWT 450
ADC_TEMP 449
ADC_TRIG0 450
ADC_TRIG1 450
ADC_VSS 449
AHB 55, 176
Alarm Registers 357
ALM interrupt 357
ALM100 357
AM08XX, *see* real-time clock
AM18XX, *see* real-time clock
AMBA 55
Analog Multiplexer Channel Selection 451
analog mux 449
analog-to-digital converter 48
APB 55
Architecture Reference Manual 56
Area, Direct 177
ARM, *see* processor
ARMv7 56
Attachment, debugger 70
Autoadjustment, HFRC 340
Automatic Sample Accumulation 451

©2017 Ambiq Micro, Inc.
All rights reserved.

B
Bandgap 450
battery life 47
BCD format 356
Buck Converter Charge Insertion 370
Buck Converters 491
Bus Not Busy 148, 183
bus, AMBA AHB 55
bus, AMBA APB 55
bus, DCode 55
bus, ICode 55
bus, System 55
C
Calibration, Distributed Digital 338, 339
CALRC 338
CALXT 339
CLKOUT 337, 338, 340
Clock Generator Module 337
clock sources 48
clock, interface 144
CMPOUT 484
CMPR0 368, 369
CMPR1 369
CONT 151
Continuous 369
control, accumulation 451
converters, buck 491
core, *see* processor
Cortex, *see* processor
counter, 32-bit 370
CPHA 152, 155, 188
CPOL 152, 155, 188
CTRERR 356
CTS 246, 248
D
Data Valid 148, 184
DCode 55
debug 70
Debug Interfaces 70
debugger attachment 70
Deep Sleep 337
Deep Sleep Mode 56
Deep Slope Mode 188
Direct Area 177
Distributed Digital Calibration 338, 339

©2017 Ambiq Micro, Inc.
All rights reserved.

E
EG_IOSLAVE_FIFOPTR_FIFOSIZ 180
event 50
event, wakeup 56
F
Fast Mode Plus 183
fault handler, Memanage 55
Faulting Address Trapping Hardware 70
FIFO 177
    Area Functions 180
FIFOCTR 180
FIFOPTR 180
FIFOREM 147
FIFORTHR 147
FIFOSIZ 147, 180
FIFOUPD 181
FIFOWTHR 147
flash 48
G
GPIO 229
GPIO and Pad Configuration Module 225
GPIOA_IER 230
GPIOA_ISR 230
GPIOA_WCR 230
GPIOB_IER 230
GPIOB_ISR 230
GPIOB_WCR 230
GPIOB_WSR 230
GPIOEN 229
GPIOENA 230
GPIOENB 230
GPIOnINCFG 229, 232
GPIOn_INT 232
GPIOnINTD 232
GPIOnINTP 230
GPIOnOUTCFG 231
GPIORD 232
GPIORDA 229
GPIORDB 229
GPIOWT 229, 230
GPIOWTA 230
GPIOWTB 230
GPIOWTCA 230
GPIOWTCB 230
GPIOWTSA 230
GPIOWTSB 230

©2017 Ambiq Micro, Inc.
All rights reserved.

H
Hardware, Fault Address Trapping 70
HFADJCK 340
HFRC 340, 449
HFRC Autoadjustment 340
HFXTADJ 340
High Frequency RC Oscillator 340
HR1224 357
I
I2C
    10-bit addressing 184
    7-bit addressing 184
    ADDRESS 149
    Address 184
    Command 149
    FIFO 147
    I2CADDR 183, 184
    IO Master 0 232
    IO Master 0 Loopback 242
    IO Master 1 233, 234
    IO Master 1 Loopback 243
    IO Slave 241
    master 144
    Multi-master Arbitration 151
    Normal Read 150
    Normal Write 150
    Offset Address 149, 185
    Raw Read 151
    Raw Write 151
    Read 186
    receiver 147
    SCL 147
    SDA 147
    Slave 176, 183
    transmitter 147
    Write 185
I2C/SPI Master 337
I2C/SPI Master Module 144
ICode 55
IE bit 367
Instrumentation Trace Macrocell 70
Instrumentation Trace Module 48
interfaces, debug 70
interrupt 50
    ALM 357
    IOINT 181

©2017 Ambiq Micro, Inc.
All rights reserved.

RDERR 181
Interrupts
Vector Table 50
IO Slave Interrupt 242
IOINT 181
IOREAD 181
ITM, *see* Instrumentation Trace Macrocell
L
LDO 491
LFRC 338, 341
life, battery 47
Loopback 242
Low-Power Consumption Modes 50
M
Managed Conversion Slots 450
map, memory 53
Master Module , I2C/SPI 144
MemManage 55
memory 48
LRAM 147, 176
RAM 48
SRAM 55
memory map 53
peripheral device 54
Memory Protection Unit 55
MISO 152
mode
Active 56
Deep Sleep 56, 337
Sleep 56
mode, Deep Sleep 56
Module, ADC and Temperature Sensor 448
module, PINCFG 152
MOSI 152
MPU, *see* Memory Protection Unit
mux, analog 449
N
NAK 184
Nested Vectored Interrupt Controller 50
NSEL 484
NVIC, *see* Nested Vectored Interrupt Controller
O
OPER 149
oscillator
High Frequency RC 340
high frequency RC 48, 337, 449

©2017 Ambiq Micro, Inc.
All rights reserved.

low frequency RC 48, 337, 338
RC 48
XTAL 48, 337, 338
XTAL Failure Detection 341
OUTDATSEL 230
OUTENSEL 230, 231, 232
P
PAD10PULL 236, 237, 238, 239
PAD20FNCSEL 253
PAD20INPEN 253
PAD21INPEN 253
PAD5INPEN 232, 234
PAD5PULL 232, 234
PAD5RSEL 232
PAD6INPEN 232, 234
PAD6PULL 232, 234
PAD6RSEL 232
PAD7PULL 234
PAD8INPEN 233, 234, 236, 237, 238, 239
PAD8PULL 233, 234, 236, 237, 238, 239
PAD9INPEN 233, 234, 236, 237, 238, 239
PAD9PULL 233, 234, 236, 237, 238, 239
PADKEY 229
PADnFNCSEL 225–??, 229
PADnINPEN 232, 236, 237, 238, 239, 245, 247, 249, 250
PADnPULL 226, 232, 236, 237, 238, 239, 245, 247, 249, 250
PADnRSEL 232
Peripheral Device Memory Map 54
PINCFG 152
power 47
power modes 56
Power Optimization 370
power-on reset 56
processor 48
Protected Memory System Architecture 55
Protection regions 55
PSEL 484
PTAT 484
PWDKEY 484
R
RDERR 181
Real Time Clock Module 341
real-time clock 48
REG_CLK_GEN_ALMLOW_ALM100 357
REG_CLK_GEN_ALMLOW_ALMHR 357
REG_CLK_GEN_ALMLOW_ALMMIN 357

©2017 Ambiq Micro, Inc.
All rights reserved.

REG_CLK_GEN_ALMLOW_ALMSEC 357
REG_CLK_GEN_ALMUP_ALMDATE 357
REG_CLK_GEN_ALMUP_ALMMO 357
REG_CLK_GEN_ALMUP_ALMWKDY 357
REG_CLKGEN_CALXT 339
REG_CLK_GEN_CTRLOW_CTR100 356
REG_CLK_GEN_CTRLOW_CTRHR 356
REG_CLK_GEN_CTRLOW_CTRMIN 356
REG_CLK_GEN_CTRLOW_CTRSEC 356
REG_CLK_GEN_CTRUP_CB 356
REG_CLK_GEN_CTRUP_CEB 357
REG_CLK_GEN_CTRUP_CTRDATE 356
REG_CLK_GEN_CTRUP_CTRERR 356
REG_CLK_GEN_CTRUP_CTRMO 356
REG_CLK_GEN_CTRUP_CTRWKDY 356
REG_CLK_GEN_CTRUP_CTRYR 356
REG_CLKGEN_HFTUNERB 340
REG_CLKGEN_OCTRL_OSEL 338, 339
REG_CLK_GEN_RTCCTL_HR1224 357
REG_CLK_GEN_RTCCTL_RPT 357
REG_CLK_GEN_RTCCTL_RSTOP 356
REG_CLK_GEN_RTCCTL_WRTC 356
REG_CLKGEN_STATUS_OMODE 339
REG_CLKGEN_STATUS_OSCF 339
REG_CTIMER_CMPR0 367
REG_CTIMER_CMPR0/1 366
REG_CTIMER_CTCTRLx_CTRLINKx 370
REG_CTIMER_CTCTRLx_TMRxyFN 366
REG_CTIMER_TMRxyCLR 367
REG_CTIMER_TMRxyEN 368
REG_CTIMER_TMRxyIE 368
REG_CTIMER_TMRxyPE 367, 368
REG_CTIMER_TMRxyPOL 368
REG_GPIO_GPIOCFGy 229
REG_GPIO_GPIOyCFG_GPIOnOUTCFG 229
REG_GPIO_PADKEY 225
REG_GPIO_PADREG 225
REG_GPIO_PADREGy_PAD11PWRDN 226
REG_GPIO_PADREGy_PAD20PULL 226
REG_GPIO_PADREGy_PAD3PWRUP 226
REG_GPIO_PADREGy_PAD4PWRUP 226
REG_GPIO_PADREGy_PADnFNCSEL 225
REG_GPIO_PADREGy_PADnINPEN 226
REG_GPIO_PADREGy_PADnPULL 226
REG_GPIO_PADREGy_PADnSTRNG 225
REG_IOMSTRn_CLKCFG_DIV3 144

©2017 Ambiq Micro, Inc.
All rights reserved.

REG_IOMSTRn_CLKCFG_DIVEN 145
REG_IOMSTRn_CLKCFG_FSEL 144
REG_IOMSTRn_CLKCFG_LOWPER 145
REG_IOMSTRn_CLKCFG_TOTPER 145
REG_IOMSTRn_CMD 146
REG_IOMSTRn_FIFOPTR_FIFOREM 147
REG_IOMSTRn_FIFOPTR_FIFOSIZ 147
REG_IOMSTRn_FIFOTHR_FIFOWTHR 146
REG_IOMSTRn_IOMCFG_SPHA 152
REG_IOMSTRn_IOMCFG_SPOL 152
REG_IOSLAVE_FIFOCFG_FIFOBASE 177
REG_IOSLAVE_FIFOCFG_FIFOMAX 177
REG_IOSLAVE_FIFOCFG_ROBASE 180
REG_IOSLAVE_FIFOCTR 180
REG_IOSLAVE_FIFOPTR_FIFOPTR 180
REG_IOSLAVE_FUPD_FIFOUPD 181
REG_IOSLAVE_FUPD_IOREAD 181
REG_IOSLAVE_IOSCFG_I2CADDR 183
REG_IOSLAVE_IOSCFG_LSB 188
REG_IOSLAVE_PRENC 179
Repeated Count 367
Repeated Pulse 368
Reset Module 424
reset, power-on 56
RESTART 184
RSTn 424
RTC, *see* real-time clock
RTS 246, 248
S
SAR, *see* Successive Approximation Register
SCR, *see* System Control Register
Serial Wire Debug 70
Serial Wire Debugger 48
Single Count 367
Single Pulse 368
Sleep Mode 56, 188
SLEEPONEXIT 56
Slots, Mananged Conversion 450
SPHA 155
SPI 152
    3-wire 187
    CHANNEL 152
    CMD Register 152
    Complex Operations 154
    frequency 145
    IO Master 0 3-wire 239

©2017 Ambiq Micro, Inc.
All rights reserved.

IO Master 0 4-wire 234
IO Master 0 4-wire Loopback 243
IO Master 1 3-wire 239, 240, 241
IO Master 1 4-wire 236, 237, 238, 239
IO Master 1 4-wire Loopback 243
IO Slave 3-wire 242
IO Slave 4-wire 242
master 144
Normal Read 153
Normal Write 152
OPER 152
Phase 155
Polarity 155
Raw Read 154
Raw Write 153
Read 187
Slave 176, 186
slave 186
Slave Addressing 152
Write 187
SPOL 155, 188
START 184
Start Data Transfer 148, 184
STOP 151, 184
STOP condition 148
Stop Data Transfer 148, 184
Successive Approximation Register 48, 448
SWD, *see* Serial Wire Debug
SWD, *see* Serial Wire Debugger
SWDCK 253
SWDIO 253
SYSRESETREQn 424
System Control Register 56
T
Temperature Sensor 448
TMRWCR 367, 368
TPIU, *see* Trace Port Interface Unit
Trace Port Interface Unit 48, 70
Track and Hold Time 451
TRIGSEL 450
TX 245, 247, 249, 250
U
UART 245, 340
CTS 246, 248
RTS 246, 248
RX 245, 247, 249, 250

©2017 Ambiq Micro, Inc.
All rights reserved.

UPLNGTH 152
V
VCOMP, *see* Voltage Comparator
VEXT1 484
VEXT2 484
Voltage Comparator 253, 484
Voltage Regulator Module 135, 491
VREFEXT1 484
VREFEXT2 484
VREFEXT3 484
VREFINT 484
VTEMP 484
W
Wait-For-Interrupt 56
Wakeup 188
wake-up 48
Wake-Up Interrupt Controller 56
Watchdog Timer 417
WC bit 367
WDTCFG 417
WFI, *see* Wait-For-Interrupt
WIC, *see* wake-up
Window Comparisons 451
X
XT 338, 341
XT Oscillator 338

©2017 Ambiq Micro, Inc.
All rights reserved.

20. Ordering Information

Table 796: Ordering Information

Orderable Part Number	Flash	RAM	Package	Packing	Temperature Range	Availability
AMA2B1KK-KLR	1 MB	256 KB	64-pin LGA	Tape and Reel	–40 to 85°C	Now

©2017 Ambiq Micro, Inc.
All rights reserved.

21. Document Revision History

Table 797: Document Revision List

Revision Number	Date	Description
0.10	Apr 2017	Initial NDA release
0.11	May 2017	Updated product brief "Description" section Updated typical system application diagram in first page Updated ball map to highlight internally shared and "not to use" pins Updated system block diagram (system_core) Created a die connection diagram (system_core) in BLE chapter Corrected all references of Apollo2 to Apollo2 Blue Reduced content in the BLE chapter to relevant
0.12	May 2017	Updated Pin List and Function Table Updated Block Diagram for the Bluetooth Low Energy sub-system Updated Pad Function Mapping table Updated GPIO configuration registers Added Die-to-Die Interconnection Table
0.13	Aug 2017	Updated Feature List and diagram Corrected interchanged pads 45 and 46 in Pin Configuration Figure diagram and Die Interconnection diagram/list Section 2.2 added Chapter 4 (BLE Sub-system) updated Removed ADC inputs and triggers not available in package Updated electricals Updated Order Information table Updated part number
0.8	Nov 2017	Electricals: Many TBDs filled in Pin List and Functions Table: Noted analog inputs IOS: I2C/SPI Slave Module LRAM Addressing figure corrected and text in section 5.3 added for clarity. GPIO: Corrected 4-wire SPI loopback mode table CLKGEN: Made CCTRL reg visible and added instructions for initializing. Corrected orderable part number

©2017 Ambiq Micro, Inc.
All rights reserved.

Contact Information

Address	Ambiq Micro, Inc. 6500 River Place Blvd. Building 7, Suite 200 Austin, TX 78730-1156
Phone	+1 (512) 879-2850
Website	http://www.ambiqmicro.com/
Sales	sales@ambiqmicro.com
Technical Support	support@ambiqmicro.com

Legal Information and Disclaimers

AMBIQ MICRO INTENDS FOR THE CONTENT CONTAINED IN THE DOCUMENT TO BE ACCURATE AND RELIABLE. THIS CONTENT MAY, HOWEVER, CONTAIN TECHNICAL INACCURACIES, TYPOGRAPHICAL ERRORS OR OTHER MISTAKES. AMBIQ MICRO MAY MAKE CORRECTIONS OR OTHER CHANGES TO THIS CONTENT AT ANY TIME. AMBIQ MICRO AND ITS SUPPLIERS RESERVE THE RIGHT TO MAKE CORRECTIONS, MODIFICATIONS, ENHANCEMENTS, IMPROVEMENTS AND OTHER CHANGES TO ITS PRODUCTS, PROGRAMS AND SERVICES AT ANY TIME OR TO DISCONTINUE ANY PRODUCTS, PROGRAMS, OR SERVICES WITHOUT NOTICE.

THE CONTENT IN THIS DOCUMENT IS PROVIDED "AS IS". AMBIQ MICRO AND ITS RESPECTIVE SUPPLIERS MAKE NO REPRESENTATIONS ABOUT THE SUITABILITY OF THIS CONTENT FOR ANY PURPOSE AND DISCLAIM ALL WARRANTIES AND CONDITIONS WITH REGARD TO THIS CONTENT, INCLUDING BUT NOT LIMITED TO, ALL IMPLIED WARRANTIES AND CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHT.

AMBIQ MICRO DOES NOT WARRANT OR REPRESENT THAT ANY LICENSE, EITHER EXPRESS OR IMPLIED, IS GRANTED UNDER ANY PATENT RIGHT, COPYRIGHT, MASK WORK RIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT OF AMBIQ MICRO COVERING OR RELATING TO THIS CONTENT OR ANY COMBINATION, MACHINE, OR PROCESS TO WHICH THIS CONTENT RELATE OR WITH WHICH THIS CONTENT MAY BE USED.

USE OF THE INFORMATION IN THIS DOCUMENT MAY REQUIRE A LICENSE FROM A THIRD PARTY UNDER THE PATENTS OR OTHER INTELLECTUAL PROPERTY OF THAT THIRD PARTY, OR A LICENSE FROM AMBIQ MICRO UNDER THE PATENTS OR OTHER INTELLECTUAL PROPERTY OF AMBIQ MICRO.

INFORMATION IN THIS DOCUMENT IS PROVIDED SOLELY TO ENABLE SYSTEM AND SOFTWARE IMPLEMENTERS TO USE AMBIQ MICRO PRODUCTS. THERE ARE NO EXPRESS OR IMPLIED COPYRIGHT LICENSES GRANTED HEREUNDER TO DESIGN OR FABRICATE ANY INTEGRATED CIRCUITS OR INTEGRATED CIRCUITS BASED ON THE INFORMATION IN THIS DOCUMENT. AMBIQ MICRO RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN. AMBIQ MICRO MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR DOES AMBIQ MICRO ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT, AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY, INCLUDING WITHOUT LIMITATION CONSEQUENTIAL OR INCIDENTAL DAMAGES. “TYPICAL” PARAMETERS WHICH MAY BE PROVIDED IN AMBIQ MICRO DATA SHEETS AND/OR SPECIFICATIONS CAN AND DO VARY IN DIFFERENT APPLICATIONS AND ACTUAL PERFORMANCE MAY VARY OVER TIME. ALL OPERATING PARAMETERS, INCLUDING “TYPICALS” MUST BE VALIDATED FOR EACH CUSTOMER APPLICATION BY CUSTOMER’S TECHNICAL EXPERTS. AMBIQ MICRO DOES NOT CONVEY ANY LICENSE UNDER NEITHER ITS PATENT RIGHTS NOR THE RIGHTS OF OTHERS. AMBIQ MICRO PRODUCTS ARE NOT DESIGNED, INTENDED, OR AUTHORIZED FOR USE AS COMPONENTS IN SYSTEMS INTENDED FOR SURGICAL IMPLANT INTO THE BODY, OR OTHER APPLICATIONS INTENDED TO SUPPORT OR SUSTAIN LIFE, OR FOR ANY OTHER APPLICATION IN WHICH THE FAILURE OF THE AMBIQ MICRO PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR. SHOULD BUYER PURCHASE OR USE AMBIQ MICRO PRODUCTS FOR ANY SUCH UNINTENDED OR UNAUTHORIZED APPLICATION, BUYER SHALL INDEMNIFY AND HOLD AMBIQ MICRO AND ITS OFFICERS, EMPLOYEES, SUBSIDIARIES, AFFILIATES, AND DISTRIBUTORS HARMLESS AGAINST ALL CLAIMS, COSTS, DAMAGES, AND EXPENSES, AND REASONABLE ATTORNEY FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PERSONAL INJURY OR DEATH ASSOCIATED WITH SUCH UNINTENDED OR UNAUTHORIZED USE, EVEN IF SUCH CLAIM ALLEGES THAT AMBIQ MICRO WAS NEGLIGENT REGARDING THE DESIGN OR MANUFACTURE OF THE PART.

©2017 Ambiq Micro, Inc.
All rights reserved.