Embedded FLOTOX Flash on Ultra-Low Power 55nm Logic DDC Platform


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Abstract

We have successfully embedded flash memory on an ultra-low power (<0.9V) 55nm Deeply Depleted Channel™ (DDC) platform. In spite of reduced thermal budget of DDC process, single-bit charge loss (SBCL) of flash after cycling can be optimized and is comparable to that of baseline embedded flash. We have also verified that improved variability and resultant ultra-low power digital performance of the DDC process is maintained in an embedded flash flow.

Introduction

The DDC transistor has been shown to achieve ultra-low voltage SRAM operation [1] and to improve digital and analog performance [2] by aggressive reduction in random dopant fluctuation (RDF) and improvement in device electrostatic performance.

It is strongly desired to embed non-volatile memories on the DDC platform to enable a wide range of ultra-low power applications such as smartcards and a variety of energy harvesting and sensor MCUs for Internet of Things (IoT) applications.

We have successfully embedded and characterized 1T NOR FLOTOX flash macro on DDC platform. The FLOTOX flash cell itself can be applied to other architectures such as 2T NOR flash suitable for ultra-low power applications [3-4].

DDC Structure and 1T NOR Flash Macro

Cross sectional DDC structure is shown in Fig.1. DDC process utilizes reduced thermal budget in order to suppress impurity diffusion into the undoped epitaxial channel layer.

Memory cell layout of 1T NOR FLOTOX flash macro used in this work is shown in Fig.2. The macro contains 512 word lines (WL) and 1024 bit lines (BL) resulting 512k cells.

Process Flow and Challenges

Fig. 3 compares the process flow for embedded flash on DDC platform with that for standard DDC and embedded flash on baseline platform. Modified steps for embedded flash on DDC platform are highlighted by yellow. Epitaxial layer is thickened to compensate for Si loss during additional oxidation steps for flash tunnel oxide (TNOX) and high voltage gate oxide (HVGBOX). Temperatures for flash related steps are aggressively lowered. Channel and drain engineering for flash and HV transistors are carefully modified.

Fig. 4 shows cross-sectional TEM of fabricated flash cells on both baseline and DDC platforms. The cells are very similar with the exception of smaller STI corner rounding of flash on DDC platform.

 Leakage current through TNOX and ONO with aggressively reduced thermal budget is very concerned to degrade flash data retention characteristics. Moreover, past literature [5-7] suggests that low temperature TNOX and reduced STI corner rounding degrade flash reliability, especially single bit charge loss (SBCL) after program & erase (P/E) cycling.

DDC Characteristics

Fig. 5 shows Ion-Ioff plots comparing performance of DDC transistors with and without embedded flash. Though there found slightly worse NMOS but slightly better PMOS with embedded flash, the differences are small enough to adjust.

Fig. 6 shows Pelgrom AVT values as a function of $V_T$. Pelgrom AVT values on an embedded flash DDC flow are comparable to those on a standard DDC flow and significantly better than those on a baseline 55nm flow. The results validate that the additional thermal budget for the flash related steps could be enough reduced to suppress impurity diffusion from screen layer to un-doped epitaxial channel layer of DDC transistors.

High Voltage (10V) Transistors for Flash Control

Fig. 7 shows source drain (SD) breakdown voltage (BV) of high voltage (HV) transistors as a function of $V_T$. Even with the aggressive reduction in thermal budget, both NMOS and PMOS transistors show BV in excess of 10V. If HV NMOS and PMOS are used symmetrically for flash control, the peripheral circuit can apply 20V to the FLOTOX flash cell, making it applicable not only for 1T NOR but also for other architectures of FLOTOX cell such as 2T NOR.

The results validate that the aggressively reduced thermal budget for flash related steps is well acceptable for HV transistors.

Fundamental Characteristics of Single Flash Cell

Table 1 summarizes the 4 different process conditions for flash cells on DDC platform – 2 levels of SD implant energy and 3 levels of $V_T$ doses for lower SD implant energy.

Fig. 8 shows fundamental characteristics of single flash cell monitors, initial $V_T (V_{ti})$, program $V_T (V_{tp})$, Vtp after accelerated drain disturb (DD), erase $V_T (V_{te})$ and Vte after accelerated gate disturb (GD). Flash cells on DDC platform show a clear Vtp shift by the accelerated DD.
Other characteristics are comparable to baseline though Vti of some DDC splits are different.

Fig. 9 shows bias conditions for the accelerated DD. There are 2 possible models for the Vtp shift by DD. One is electron F-N tunneling from floating gate (FG) to drain through TNOX and the other is hot hole injection from drain edge to FG. The hot hole is generated by impact ionization at drain edge.

Fig. 10 shows Vtp shift by DD as a function of Vti. Vtp shift increases with increasing Vti dose and decreases with increasing SD implant energy. It is clear that the Vtp shift is caused by hot hole injection and not by intrinsic TNOX tunneling, since impact ionization during DD is increased with increasing Vti dose and decreased with increasing SD implant energy but F-N tunneling is not so much affected by the splits.

Fig. 11 shows Vtp by DD as a function of disturb time with normal program bias. If disturb time is less than 2ms, Vtp shift is negligibly small. Since programming for each cell is completed by 1-2 of 1us pulses, DD time for the worst cell on a BL is about 1ms and less than 2ms. These suggest that the observed Vtp shift by DD does not degrade Vtp distribution within in a flash array. But past literature [6] suggests that the degraded DD may degrade SBCL after cycling.

**Initial Characteristics of 512k Flash Macro**

Based on the single cell results and the suggestion of past literature [6] especially about impact of DD on SBCL, we compared DDC-1 and DDC-2 with baseline. DDC-2 has higher flash SD implant energy and smaller DD compared to DDC-1.

Fig. 12 shows Vt distributions at initial, program and erase state of 70 macros for each condition. Though initial Vt (Vti) is a little different from each other, program and erase Vt (Vtp and Vte) are comparable to others because of verify operation implemented in the macro. Nice Vt distributions for any of the conditions validate small enough impact of DD on array programming as expected from Fig. 11.

Fig. 13 shows Vtp distributions before and after 250C bake. No severe Vtp shift was seen for any of the conditions which validating leakage current through TNOX and ONO with the aggressively reduced thermal budget is not an issue.

These results validate that initial characteristics of the macro with the aggressively reduced thermal budget are well acceptable and healthy.

**Characteristics of 512k Flash Macro after Cycling**

Since flash reliability after cycling especially SBCL is a big concern, we cycled 20 dice for each condition up to 1k times. 10 dice for each were used for Vte shift and another 10 dice for Vtp shift after cycling and bake. We lowered the bake temperature down to 150C and elongated the bake time up to 1kH to detect SBCL definitely.

Fig. 14 shows minimum Vtp and maximum Vte in a 512k array as a function of cycling. We applied Vt verify operation for the normal cycling but did not apply it for program and erase operation just before Vtp and Vte measurement after predetermined cycling. Though flash cells on DDC platform showed a little faster window narrowing by charge trapping than flash cells on baseline, it is well acceptable.

Fig. 15 shows Vtp and Vte distributions after 1k cycling and 150C 0-1kH bake. We plotted all cells on 10 dice of 512k macro at once in a graph to make SBCL more clearly visible. No Vte shift was seen on any of the conditions. On the other hand, Vtp shift of SBCL was seen on DDC-1 but not seen on both DDC-2 and baseline. Since differences between DDC-1 & DDC-2 are flash Vt and SD implant conditions and resultant drain disturb (DD) amount, the results mean that (1) SBCL found on DDC-1 is dominated by hot hole injection during DD and can be optimized as DDC-2, (2) very low temperature TNOX and small STI rounding adopted for both DDC-1 and DDC-2 are not issues.

All of the results shown above validate healthy and well acceptable initial and post-cycling characteristics of DDC-2. Moreover, DDC-2 can be improved more because there is room to reduce Vt dose further and match DD to the baseline as seen in Figure 10.

**Conclusions**

Embedded flash memory has been successfully integrated on to an ultra-low power 55nm DDC platform. This should pave the way for a variety of low power MCU based applications.

This work on flash added new knowledge to the past literatures, (1) flash single bit charge loss (SBCL) is much dominated by hot hole injection during drain disturb (DD) rather than F-N stressing of TNOX and (2) very low temperature TNOX, ONO and STI schemes are not issues.

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**References**


[7] Ming-Yi Lee et al., ‘Anomalous Single Bit Retention Induced by Asymmetric STI-Corner-Thinning for Floating Gate Flash Memories’, *IEEE IPFA 2012*
Fig. 1: Structure of DDC transistor

Fig. 2: FLOTOX flash cell layout

Fig. 3: Process flow of DDC and embedded flash

Fig. 4: a) X-TEM of flash parallel to BL on baseline & DDC

Fig. 4: b) XTEM of flash parallel to WL on baseline & DDC

Fig. 5: a) Ion/Ioff plot for short channel NMOS

Fig. 5: b) Ion/Ioff plot for short channel PMOS

Fig. 6: Pelgrom AVT as a function of long channel V_T

Fig. 7: a) BV of HV NMOS

Fig. 7: b) BV of HV PMOS

Table 1: Conditions for flash evaluation

<table>
<thead>
<tr>
<th>Condition</th>
<th>Vt Implant</th>
<th>SD Implant</th>
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<tbody>
<tr>
<td>Baseline</td>
<td>POR</td>
<td>POR</td>
</tr>
<tr>
<td>DDC-1</td>
<td>highest</td>
<td>POR</td>
</tr>
<tr>
<td>DDC-1+</td>
<td>higher</td>
<td>POR</td>
</tr>
<tr>
<td>DDC-1-</td>
<td>lower</td>
<td>POR</td>
</tr>
<tr>
<td>DDC-2</td>
<td>lower</td>
<td>higher</td>
</tr>
</tbody>
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Fig. 8: Fundamental flash characteristics

Fig. 9: Bias condition of DD

Fig. 10: Dependence of $V_{tp}$ shift by DD on $V_{ti}$

Fig. 11: Dependence of $V_{tp}$ shift on DD time

Fig. 12: Distribution of UV, $V_{tp}$ & $V_{te}$ in 512k*70 dice

Fig. 13: $V_{tp}$ before & after 250C bake for 512k*70 dice

Fig. 14: Flash window as a function of cycling

Fig. 15: $V_{te}$ & $V_{tp}$ distribution after 1k cycling & 150C bake