FUJITSU SEMICONDUCTOR
MEMORY SOLUTION DATA SHEET

DS501-00071-1v1-E

Memory ReRAM

12M (1536 K × 8) Bit SPI

MB85AS12MT

■ DESCRIPTION

MB85AS12MT is a ReRAM (Resistive Random Access Memory) chip in a configuration of 1,572,864 words × 8 bits, using the resistance-variable memory process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.
MB85AS12MT adopts the Serial Peripheral Interface (SPI).
MB85AS12MT is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85AS12MT can be used for 5×10^5 rewrite operations.

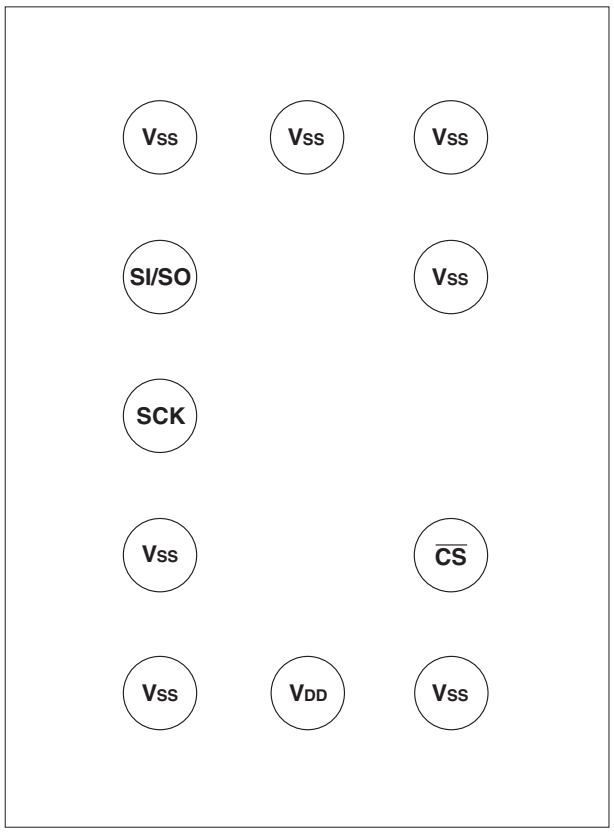
■ FEATURES

- Bit configuration : 12 Mbits (1,572,864 words × 8 bits)
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
  Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Write buffer size : 256 bytes
- Operating frequency : 10 MHz (Max)
- Data endurance : 5×10^5 times / 4bytes*
  *4 bytes are selected by A1 to A0.
- Data retention : 10 years (+85 °C)
- Operating power supply voltage : 1.6 V to 3.6 V
- Operating power supply current : Write current 1.5 mA (Typ)
  Read current 0.15 mA (Typ@5 MHz)
  Standby current 65 μA (Typ)
  Sleep current 6 μA (Typ)
- Operation ambient temperature range : -40 °C to +85 °C
- Package : 11-pin WLP
  RoHS compliant

2023.12

■ PIN ASSIGNMENT

(BOTTOM VIEW)

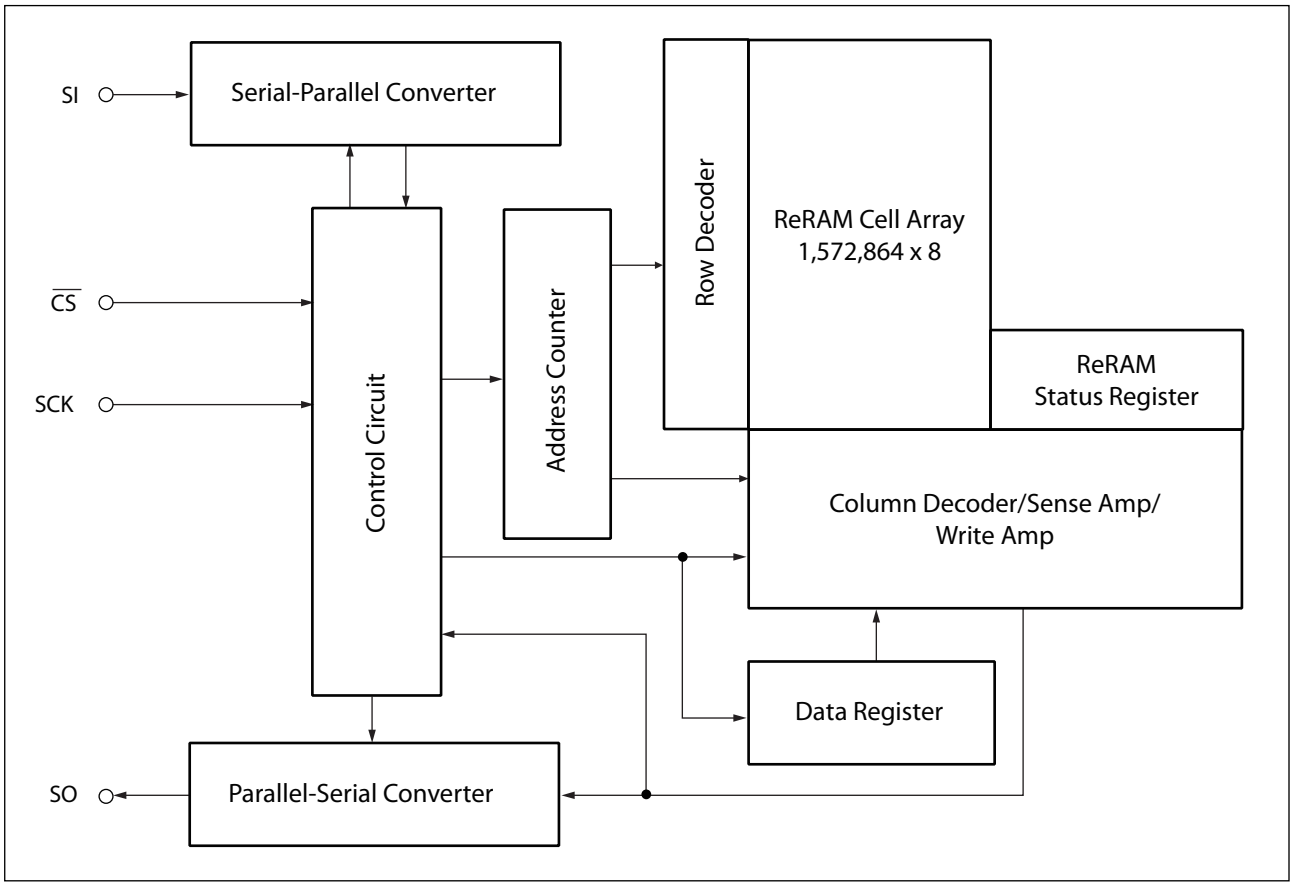


11-pin WLP Type-A

■ PIN FUNCTIONAL DESCRIPTIONS

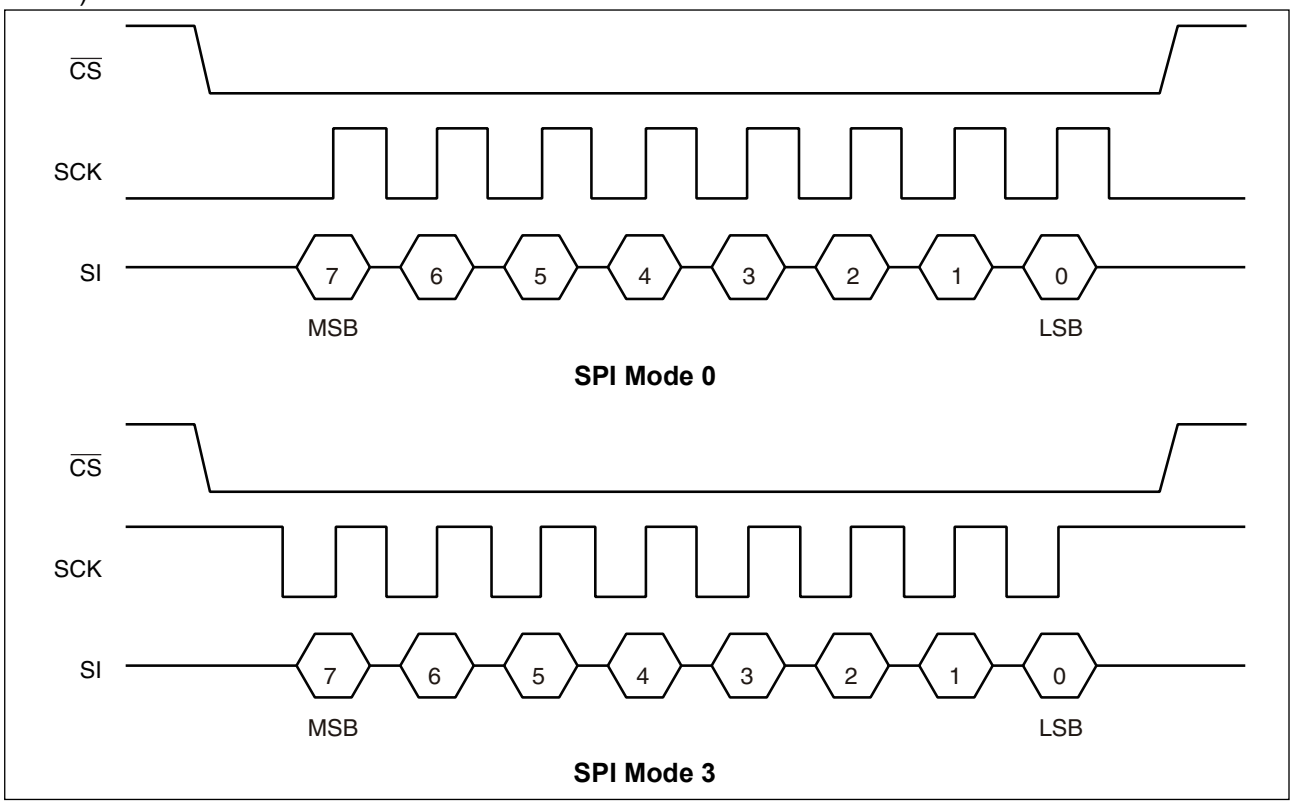
Pin Name	Functional description
$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is “H” level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is “L” level, device is in select (active) status. $\overline{CS}$ has to be “L” level before inputting op-code.
SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
SI/SO	Serial Data Input/Output pin This is an input/output pin of serial data. It inputs op-code, address, and writing data.In case of read command, it outputs read data of ReRAM memory cell array or data of status register after inputing op-code/address.
V_{DD}	Supply Voltage pin
V_{SS}	Ground pin

■ BLOCK DIAGRAM



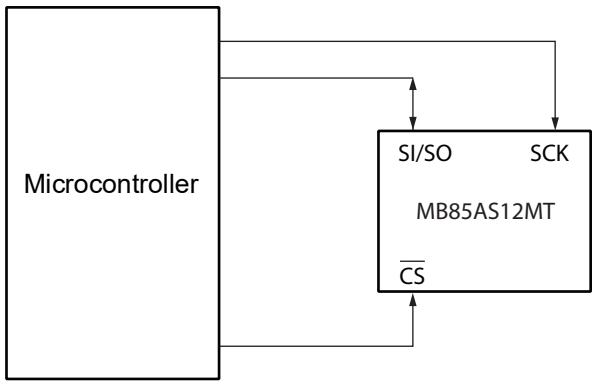
■ SPI MODE

MB85AS12MT corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .



■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85AS12MT works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port.



System Configuration

■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Not Used Bit This is bit composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command. Initial value is “0”.
6 to 4	—	Not Used Bits These are bits composed of volatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command. Initial value is “000”.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to “ BLOCK PROTECT”). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates ReRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. The rising edge of $\overline{CS}$ after WRDI command recognition. The end of writing process after WRSR command recognition. The end of writing process after WRITE command recognition.
0	WIP	Write In Progress This indicates ReRAM Array and status register are in writing process. During this writing process, any commands except RDSR will not be executed (refer to “ WRITING OPERATION OF NONVOLATILE MEMORY 2. WIP polling”). With the RDSR command, reading is possible but writing is not possible with the WRSR command.

■ OP-CODE

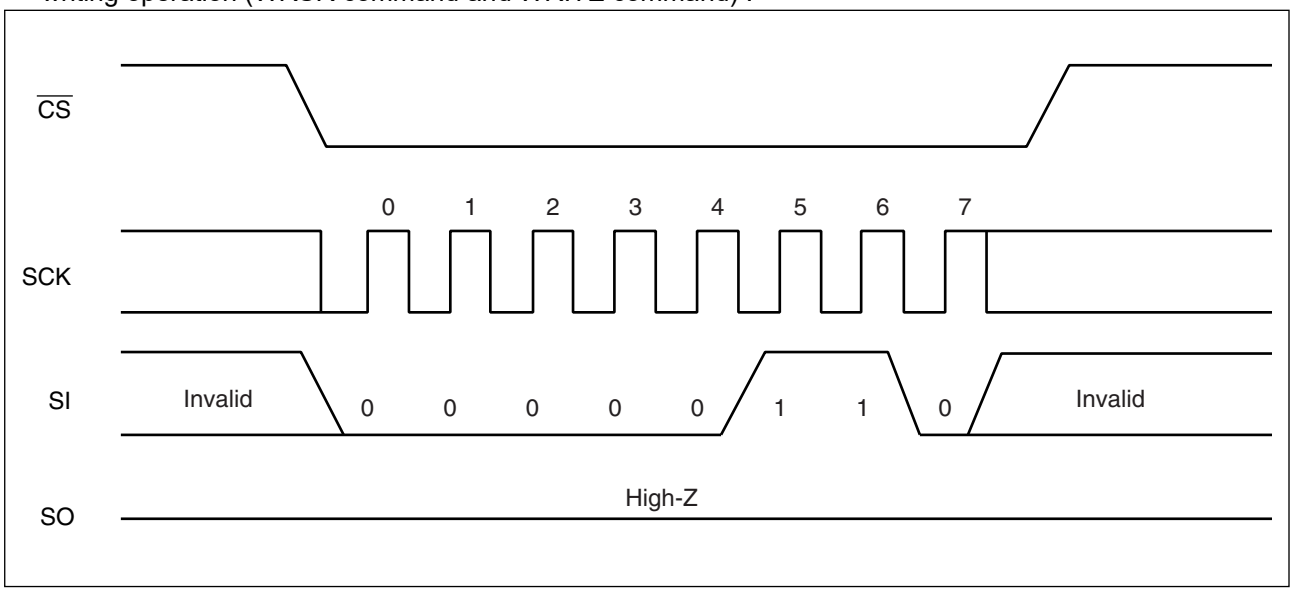
MB85AS12MT accepts 10 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If $\overline{CS}$ is risen while inputting op-code, the command are not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	$0000\ 0110_B$
WRDI	Reset Write Enable Latch	$0000\ 0100_B$
RDSR	Read Status Register	$0000\ 0101_B$
WRSR	Write Status Register	$0000\ 0001_B$
READ	Read Memory Code	$0000\ 0011_B$
WRITE	Write Memory Code	$0000\ 0010_B$
RDID	Read Device ID	$1001\ 1111_B$
RDUID	Read Device ID and Unique ID	$1000\ 0011_B$
SLEEP	Enter Sleep Mode (Power Down Mode)	$1011\ 1001_B$
PWDN		$1110\ 0010_B$

■ COMMAND

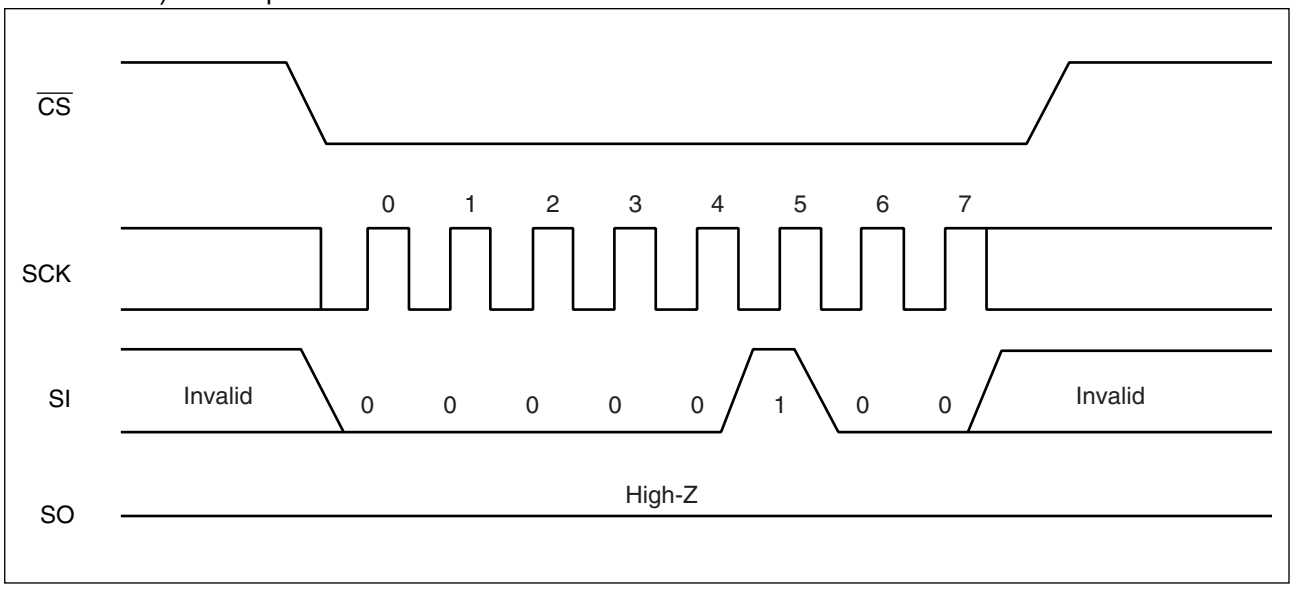
• WREN

The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) .



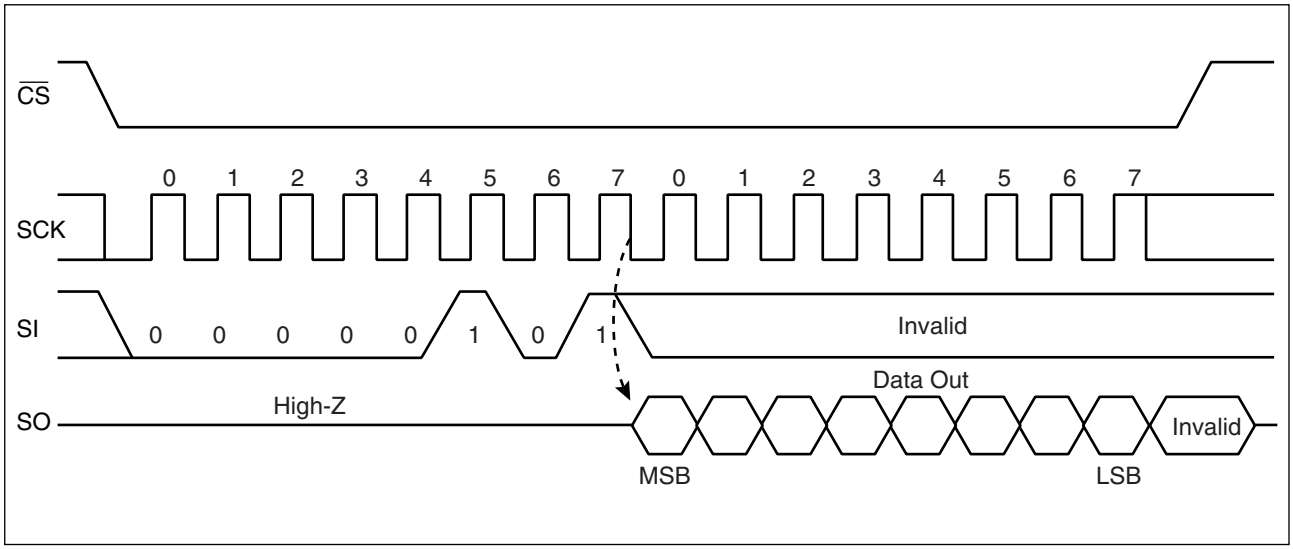
• WRDI

The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRSR command and WRITE command) are not performed when WEL is reset.



• **RDSR**

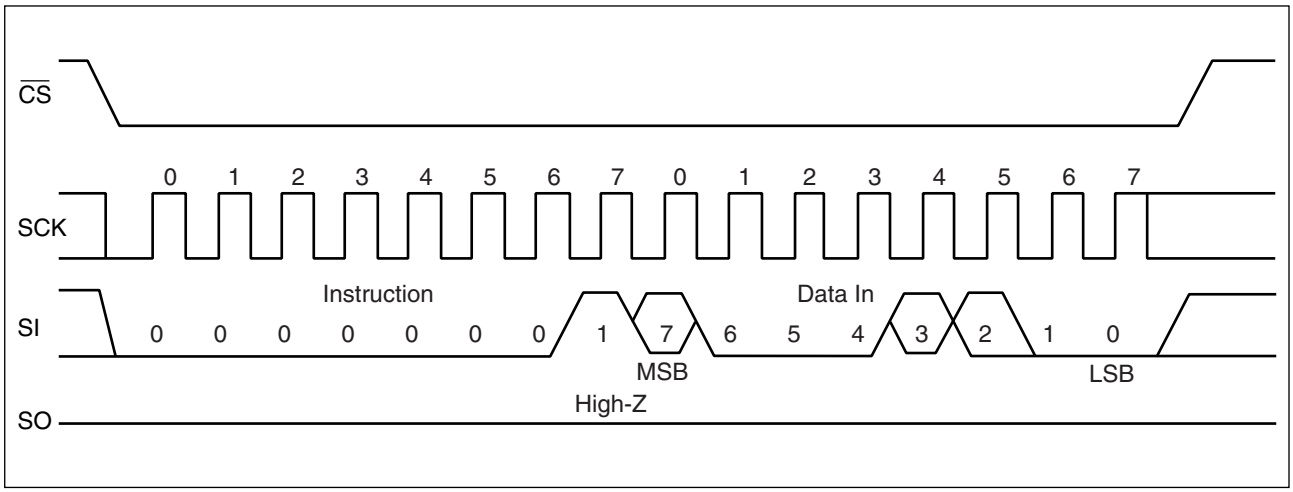
The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of $\overline{CS}$.



• **WRSR**

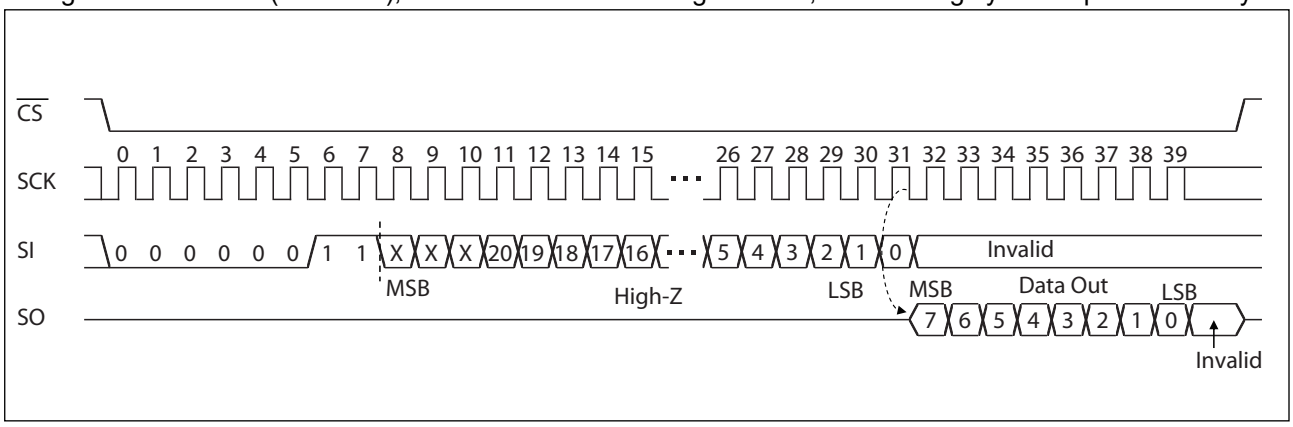
The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register cannot be written. The SI value corresponding to bit 0 is ignored. $\overline{WP}$ signal level shall be fixed before performing WRSR command, and do not change the $\overline{WP}$ signal level until the end of command sequence.

After rising edge of $\overline{CS}$, MB85AS12MT starts writing operation to nonvolatile register and set WIP bit in status register to “1”. After this writing operation has finished, reset this WIP bit from “1” to “0”. Although the RDSR command is executable for WIP polling during this writing process, any other commands will not be performed.



• **READ**

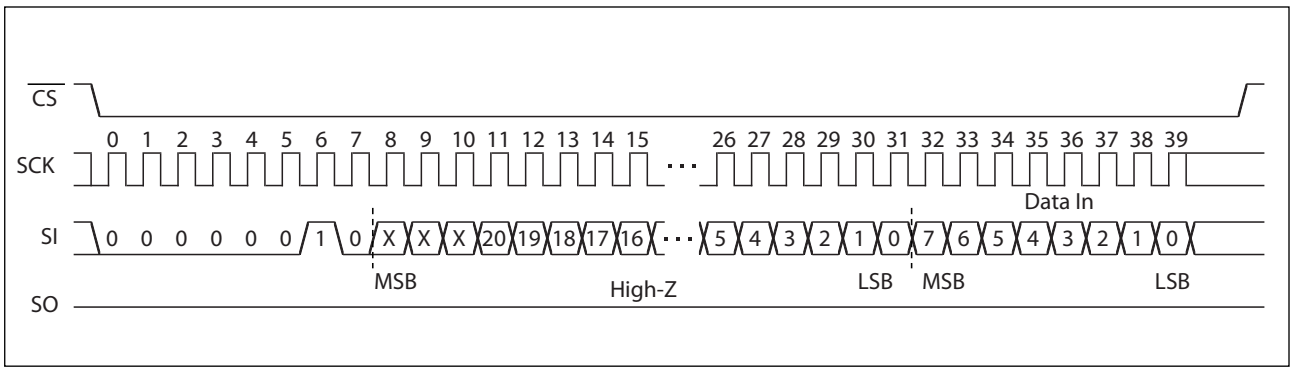
The READ command reads ReRAM memory cell array data. Arbitrary 24 bits address and op-code of READ are input to SI. The 3-bit upper address bit is invalid. And in case of designating address other than effective region (180000_H to $1FFFFF_H$), the command itself is ignored. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address ($17FFFF_H$), it rolls over to the starting address, and reading cycle keeps on infinitely.



• **WRITE**

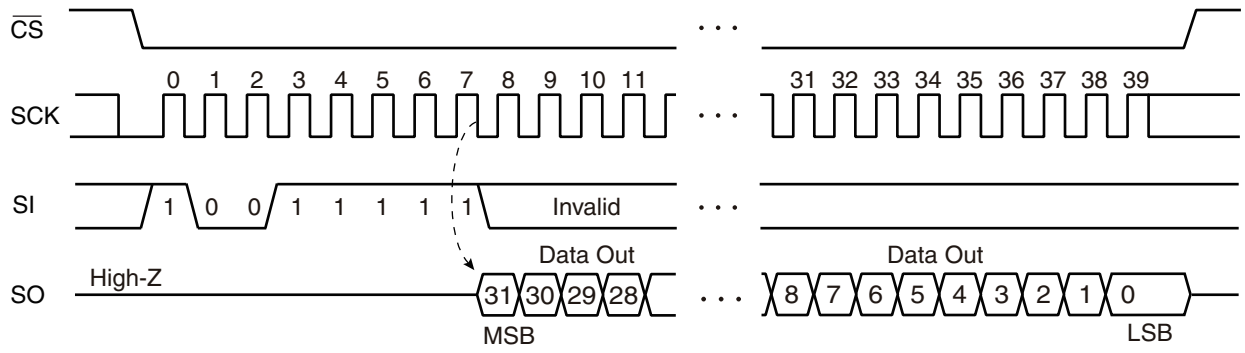
The WRITE command writes data to ReRAM memory cell array. WRITE op-code, arbitrary 24 bits of address and 8 bits of writing data are input to SI. The 3-bit upper address bit is invalid. And in case of designating address other than effective region (180000_H to $1FFFFF_H$), the command itself is ignored. During the $\overline{CS}$ is low, input writing data are temporary saved in the data register. The maximum writing data size is 256 bytes during this $\overline{CS}$ = low period. If the input writing data are more than 8 bits, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued up to 256 bytes (which is the size of data register). Data exceed 256 bytes can not be written.

After rising edge of $\overline{CS}$, MB85AS12MT starts writing operation to nonvolatile memory and set WIP bit in status register to “1”. After this writing operation has finished, reset this WIP bit from “1” to “0”. Although the RDSR command is executable for WIP polling during this writing process, any other commands will not be performed.



- **RDID**

  The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit in 32-bit Device ID until $\overline{CS}$ is risen.



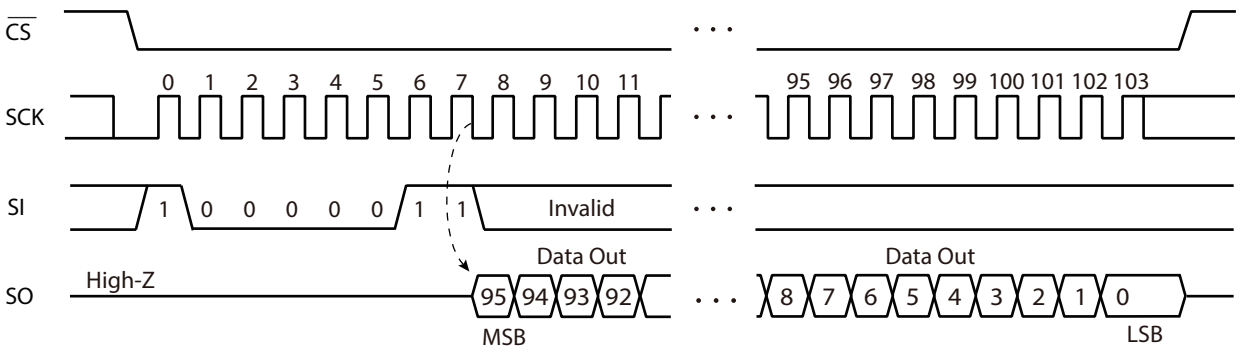
	bit									
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Hex**	
Manufacturer ID	0	0	0	0	0	1	0	0	04_H	Fujitsu
Continuation code	0	1	1	1	1	1	1	1	$7F_H$	

	Proprietary use			**Density**					**Hex**	
Product ID (1st Byte)	1	0	1	1	1	1	0	0	BC_H	Density: 11100_B = 12 Mbit

	Proprietary use								**Hex**	
Product ID (2nd Byte)	0	0	0	0	0	0	1	1	03_H	

- **RDUID**

The RDUID command reads (common) Device ID and (each chip-specific) Unique ID. After performing RDUID op-code to SI, 96-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit) / Continuation code (8bit) / Product ID (1st Byte) / Product ID (2nd Byte) as Device ID and Lot ID (40bit) / Wafer ID (8bit) / Chip ID (16bit) as Unique ID. In the RDUID command, SO holds the output state of the last bit in 96-bit Device ID and Unique ID until $\overline{CS}$ is risen.

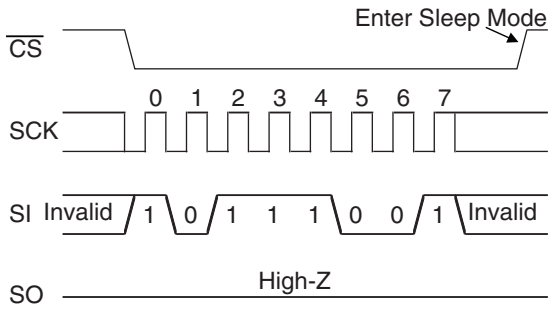


	Bits	Field	Value	Description
Device ID	[95:88]	Manufacture ID	04h	Fujitsu
Device ID	[87:80]	Continuation code	7Fh	
Device ID	[79:72]	Product ID	BCh	101b: Proprietary use 11100b: Density (12 Mbit)
Device ID	[71:64]	Product ID	03h	Proprietary use
Unique ID	[63:24]	Lot ID		64 bit Unique ID
Unique ID	[23:16]	Wafer ID		
Unique ID	[15:0]	Chip ID		

• **SLEEP/PWDN**

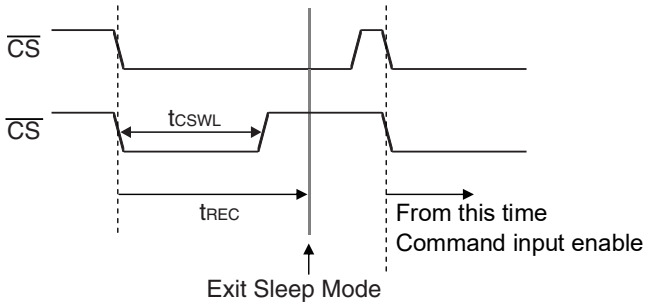
The SLEEP/PWDN command shifts the LSI to a low power mode called “SLEEP mode” (“Power Down mode”). The transition to the SLEEP mode (Power Down mode) is carried out at the rising edge of $\overline{CS}$ after operation code in the SLEEP (PWDN) command. However, when at least one SCK clock is inputted before the rising edge of $\overline{CS}$ after operation code in the SLEEP (PWDN) command, this SLEEP (PWDN) command is canceled.

After the SLEEP mode (Power Down mode) transition, SCK and SI/SO inputs are ignored.



Sleep Mode Entry

Returning to a normal operation from the SLEEP mode (Power Down mode) is carried out after t_{REC} time from the falling edge of $\overline{CS}$ (see the figure below). It is possible to return $\overline{CS}$ to H level before t_{REC} time. However, it is prohibited to bring down $\overline{CS}$ to L level again during t_{REC} period.



Sleep Mode Exit

■ WRITING OPERATION OF NONVOLATILE MEMORY

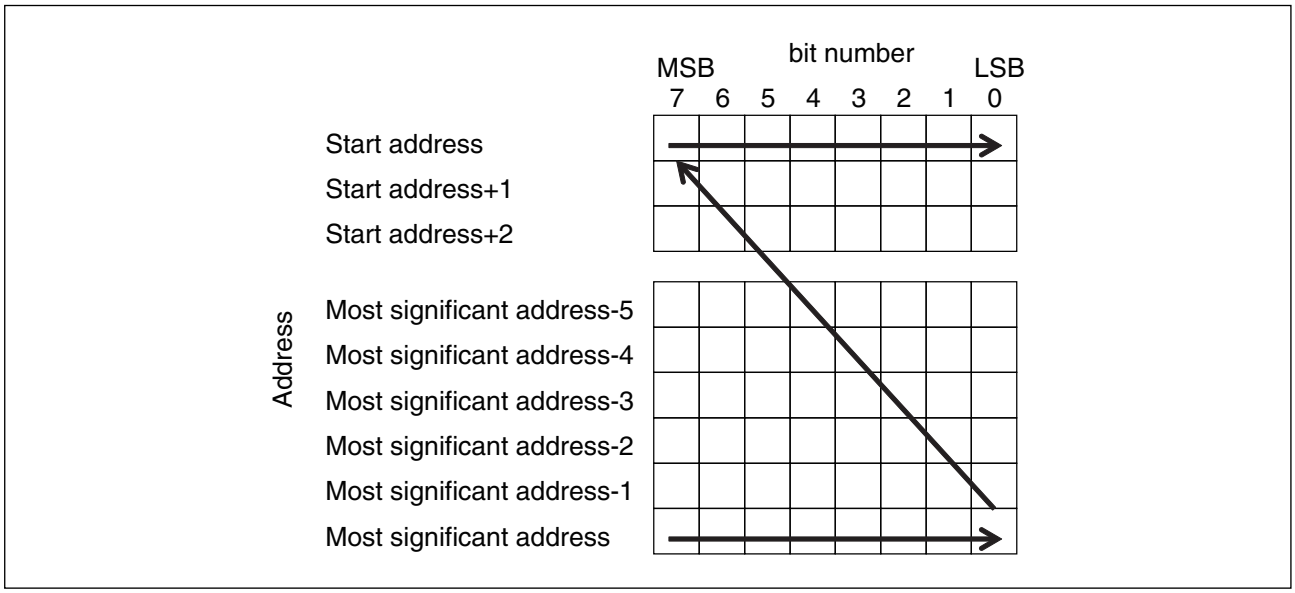
Each input data is not written to the nonvolatile memory by unit of byte right after its data input. Multiple bytes up to maximum 256 bytes are temporarily saved to the data register. After the command input is finished and rising edge of $\overline{CS}$, start writing operation from this data register to the nonvolatile memory.

1. Address counter control

In case of memory access by WRITE and READ commands, after the end of op-code and address input, it is possible to keep on accessing (= reading or writing) with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles while $\overline{CS}$ is low level. However, for the WRITE command, continuous writing is restricted by the limit of buffer size in the data register.

When it reaches the most significant address, it rolls over to the starting address, and this automatic address increment will be continued by the address counter control.

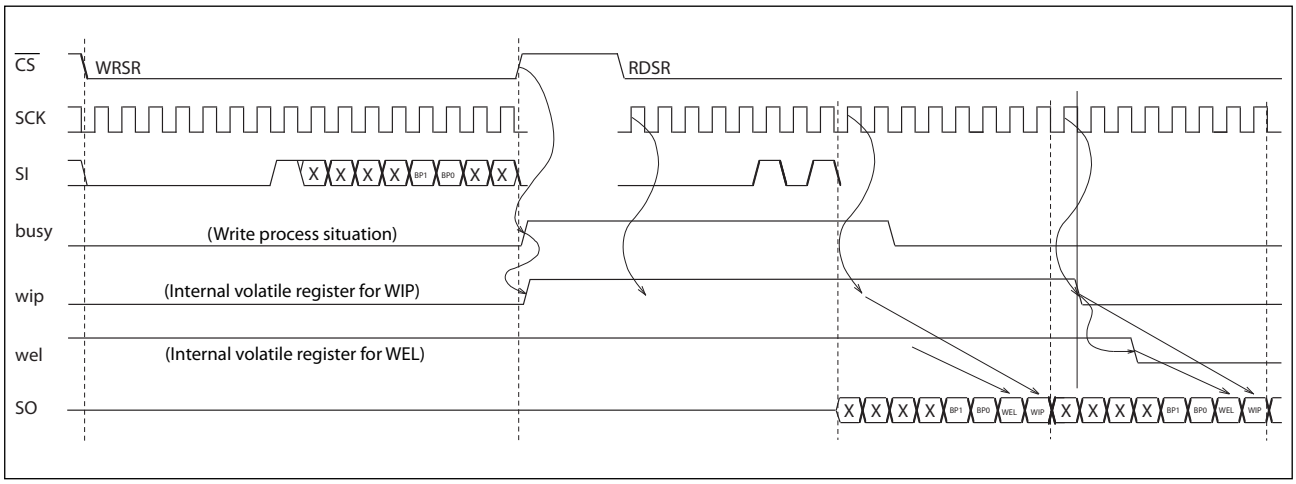
Over write protection to the nonvolatile memory is enabled by BP0 and BP1 bits in status register. When the memory address exceed it from write protected block to unprotected block by address counter control, write to the unprotected block only. Similarly, when memory address exceed it from unprotected block to protected block, does not write to the protected block.



2. WIP polling

After the last writing data was input, writing to the nonvolatile memory needs t_{WC} waiting time from the rising edge of $\overline{CS}$. This t_{WC} time becomes larger than a minimum clock cycle. Production variation and operating condition are considered, and this maximum t_{WC} value is defined. In the usual operation, this t_{WC} time is shorter than the maximum value. Therefore, MB85AS12MT supports WIP polling to improve memory access by optimizing the waiting time.

After starting the data writing to nonvolatile memory, MB85AS12MT sets “1” to a volatile register related to the WIP bit in status register. After finished the writing operation, reset this WIP bit from “1” to “0”. Although the usual commands are not executable during this writing process, only the RDSR command is acceptable. RDSR command outputs the value of status register to SO. It is possible to confirm if the internal writing operation to nonvolatile memory is finished or not, by checking the corresponding bit to WIP in output data from SO.



RDSR command also outputs the BP1 and BP0 of status register to SO. In the polling after WRSR command, MB85AS12MT outputs the BP1 and BP0 data which is set before the writing to nonvolatile memory is completed. On the other hand for WEL and WIP, MB85AS12MT outputs (WEL,WIP)=2'b11 when the writing to nonvolatile memory is not completed. When it is competed, outputs (WEL,WIP)=2'b00.

If continuously sending clocks to SCK during $\overline{CS}$ = low, it is also possible to keep on outputting from the most significant address to the least significant address (WIP bit) in status register in unit of 8 cycles since 17th clock. In case the WIP polling is applied, WIP and WEL bits in status register output to SO by RDSR command are updated regularly.

Figure shows the example of RDSR command input with continuously sending clocks over 17 during $\overline{CS}$ = low, before the writing process of WRSR command is finished.

■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	120000H to 17FFFFH (upper 1/4)
1	0	0C0000H to 17FFFFH (upper 1/2)
1	1	000000H to 17FFFFH (all)

■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, as shown in the table. .

WEL	Protected Blocks	Unprotected Blocks	Status Register
0	Protected	Protected	Protected
1	Protected	Unprotected	Unprotected

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 4.0	V
Input voltage*	V_{IN}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Output voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Operation ambient temperature	T_A	− 40	+ 85	°C
Storage temperature	Tstg	− 55	+ 125	°C

*:These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	V_{DD}	1.6	—	3.6	V
Operation ambient temperature*2	T_A	− 40	—	+ 85	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current	$\|I_{LI}\|$	$\overline{CS}$, SCK = 0 V to V_{DD}	—	—	1	µA
Output leakage current	$\|I_{LO}\|$	SI/SO = 0 V to V_{DD}	—	—	1	µA
Operating power supply current (Read)	I_{DDR} (60)	SCK = 5 MHz, T_A=0 °C to 60 °C, 1.6V ≤ V_{DD} ≤ 2.0V	—	0.15	0.3	mA
	I_{DDR} (85)	SCK = 10 MHz, T_A= − 40 °C to 85 °C, 1.6V ≤ V_{DD} ≤ 3.6V	—	—	0.7	
Operating power supply current (Write)	I_{DDW} (60)	SCK = t_{WC}, T_A=0 °C to 60 °C, 1.6V ≤ V_{DD} ≤ 2.0V	—	1.5	—	mA
	I_{DDW} (85)	SCK = t_{WC}, T_A= − 40 °C to 85 °C, 1.6V ≤ V_{DD} ≤ 3.6V	—	—	2.5	
Standby current	I_{SB}	SCK = SI = $\overline{CS}$ = V_{DD}	—	65	500	µA
Sleep current	I_{ZZ}	$\overline{CS}$ = V_{DD} All inputs V_{SS} or V_{DD} V_{DD}=3.6V, T_A=85 °C	—	6	8	µA
		$\overline{CS}$ = V_{DD} All inputs V_{SS} or V_{DD} V_{DD}=1.45V, T_A=60 °C	—	—	6	µA
Input high voltage	V_{IH}	V_{DD} = 1.6 V to 3.6 V	V_{DD} × 0.7	—	V_{DD} + 0.5	V
Input low voltage	V_{IL}	V_{DD} = 1.6 V to 3.6 V	− 0.5	—	V_{DD} × 0.3	V
Output high voltage	V_{OH}	I_{OH} = − 1.5 mA @V_{DD} ≥ 1.8 V I_{OH} = − 1.2 mA @V_{DD} < 1.8 V	V_{DD} × 0.8	—	—	V
Output low voltage	V_{OL}	I_{OL} = 1.5 mA @V_{DD} ≥ 1.8 V I_{OL} = 1.2 mA @V_{DD} < 1.8 V	—	—	V_{DD} × 0.2	V

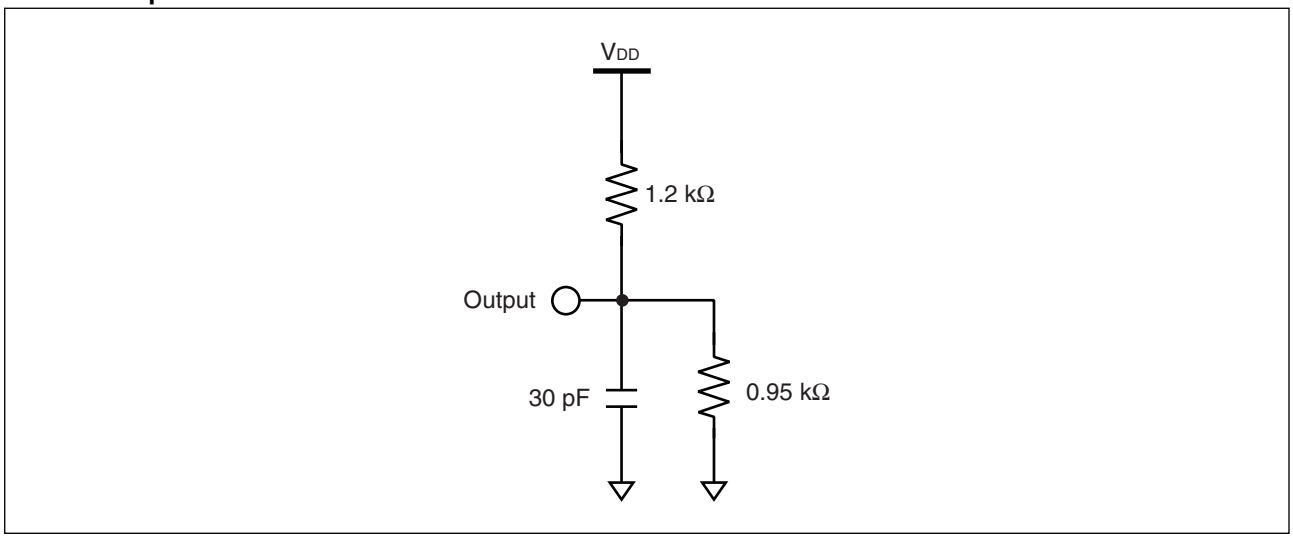
2. AC Characteristics

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
SCK clock frequency	f_{CK}	0	—	10	MHz	
Clock high time	t_{CH}	40	—	—	ns	
Clock low time	t_{CL}	40	—	—	ns	
Chip select set up time	t_{CSUH}	30	—	—	ns	$\overline{CS}$ rising to SCK rising
	t_{CSUL}	30	—	—		$\overline{CS}$ falling to SCK rising
Chip select hold time	t_{CSHH}	30	—	—	ns	SCK rising to $\overline{CS}$ falling
	t_{CSHL}	30	—	—		SCK rising to $\overline{CS}$ rising
	t_{CSH}	30	—	—		SCK falling to $\overline{CS}$ rising
Output disable time	t_{OD}	—	—	30	ns	
Output active time	t_{OLZ}	0	—	—	ns	
Output data valid time	t_{ODV}	—	—	35	ns	
Output hold time	t_{OH}	0	—	—	ns	
Deselect time	t_{D}	100	—	—	ns	
Data rising time	t_{R}	—	—	50	ns	
Data falling time	t_{F}	—	—	50	ns	
Data set up time	t_{SU}	20	—	—	ns	
Data hold time	t_{H}	20	—	—	ns	
Write cycle time	t_{WC}	—	5000	10000	µs	@100% data turn over
Recovery time from SLEEP mode	t_{REC}	—	400	1000	µs	
$\overline{CS}$ pulse width at SLEEP mode exit	t_{CSWL}	100	—	—	ns	

AC Test Condition

Power supply voltage : 1.6 V to 3.6 V
Operation ambient temperature : − 40 °C to + 85 °C
Input voltage magnitude : $V_{DD} \times 0.7 \leq V_{IH} \leq V_{DD}$
$0 \leq V_{IL} \leq V_{DD} \times 0.3$
Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

AC Load Equivalent Circuit

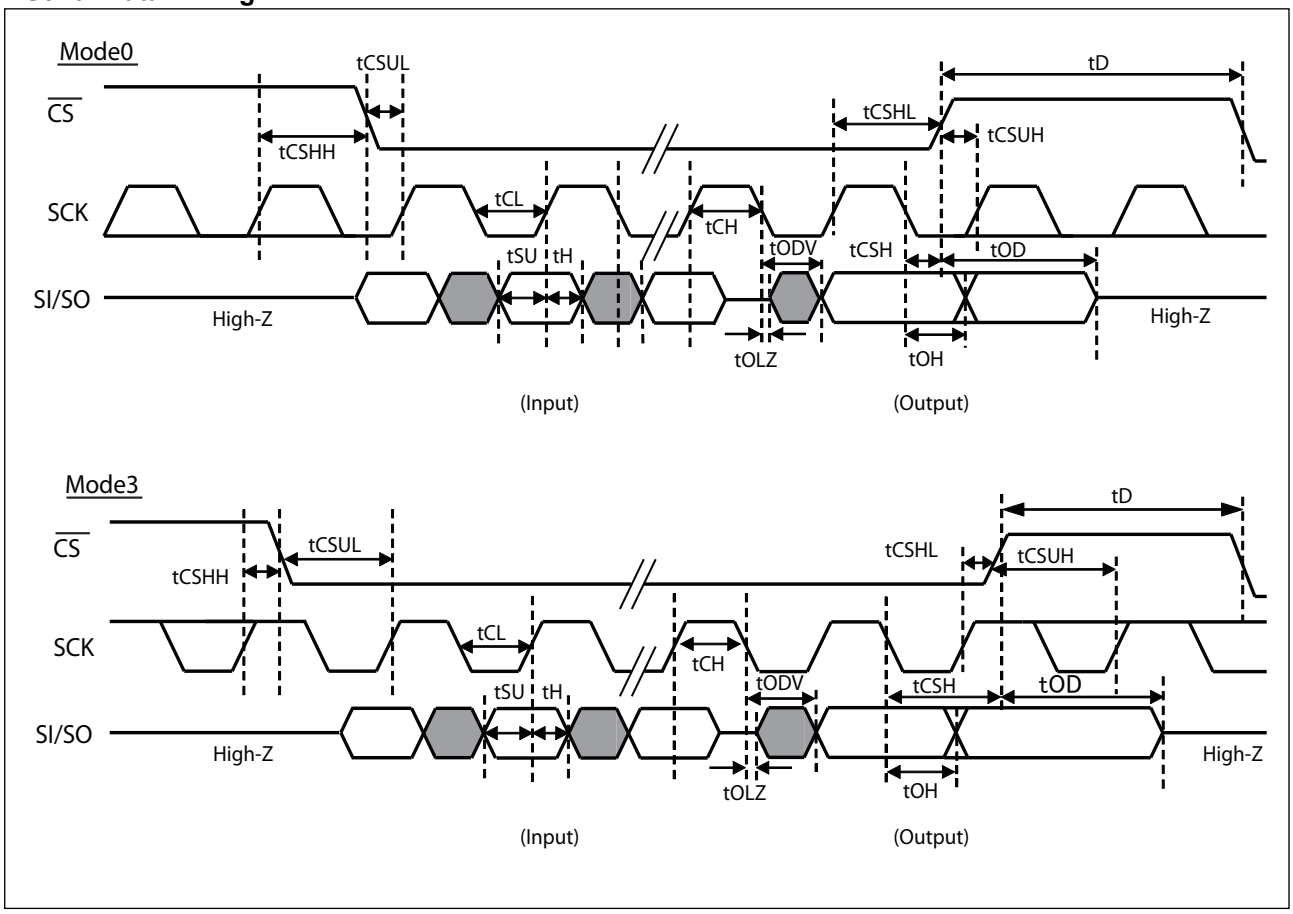


3. Pin Capacitance

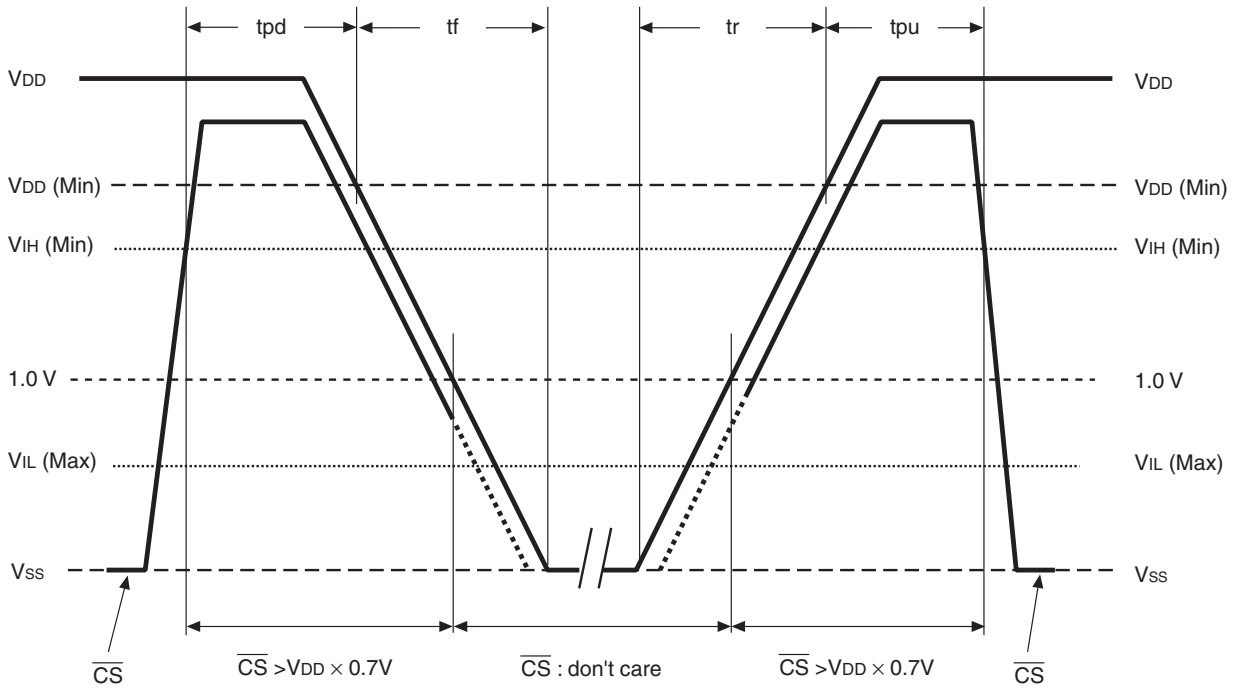
Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output capacitance	C_{IO}	V_{DD} = V_{IN} = V_{OUT} = 0 V, f = 1 MHz, T_A = +25 °C	—	6	pF
Input capacitance	C_I		—	3	pF

■ TIMING DIAGRAM

• Serial Data Timing



■ POWER ON/OFF SEQUENCE



* : $\overline{CS}$ (Max) < V_{DD} + 0.5 V

Parameter	Symbol	Value		Unit
		Min	Max	
$\overline{CS}$ level hold time at power OFF	tpd	10	—	ms
$\overline{CS}$ level hold time at power ON	tpu	1	—	ms
Power supply rising time	tr	50	—	µs/V
Power supply falling time	tf	100	—	µs/V

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ ReRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Write Endurance	5×10^5	—	Times/4bytes*	Operation Ambient Temperature T_A = + 85 °C
Data Retention	10	—	Years	Operation Ambient Temperature T_A = + 85 °C
Data register size	—	256	byte	

*: 4 bytes are selected by A1 to A0.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85AS12MT	≥ |2000 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		≥ |500 V|
Latch-Up (I-test) JESD78 compliant		≥ |100 mA|

■ MB85AS12MT REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

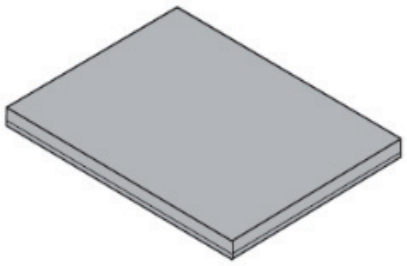
■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

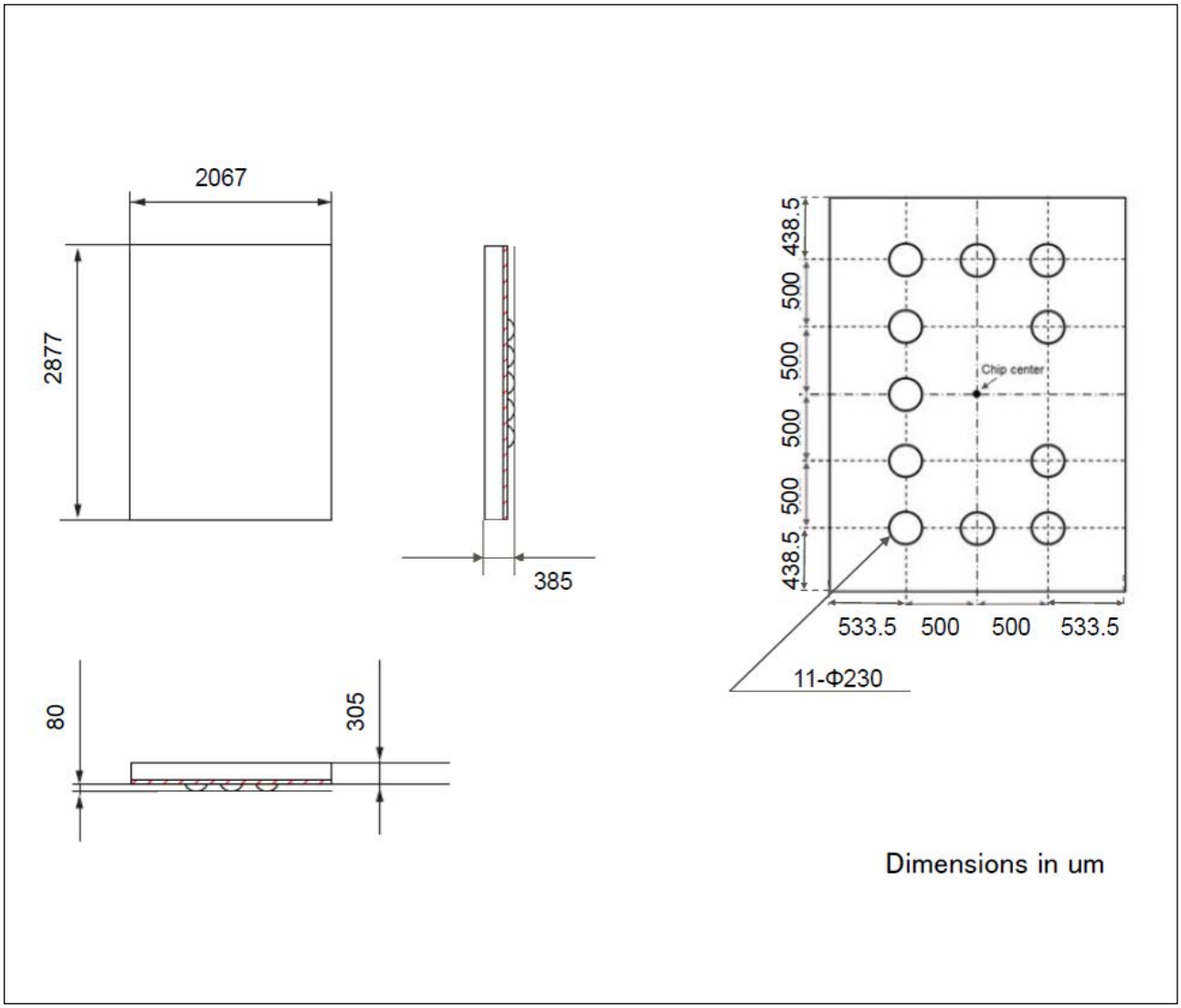
This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

■ ORDERING INFORMATION

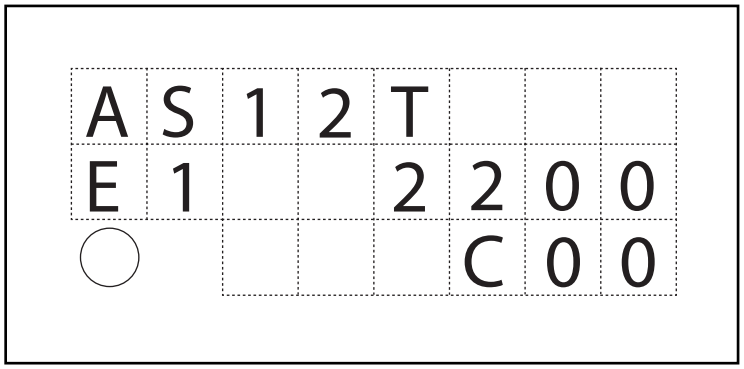
Part number	Package	Shipping form	Minimum shipping quantity
MB85AS12MTPW-GAERE1	11-pin WLP Type-A	Embossed Carrier Tape	10,000

■ PACKAGE DIMENSION

11-pin WLP		
 MB85AS12MTPW-GAERE1	Bump pitch	0.5 mm
	Package width × package length	2.067 mm × 2.877 mm
	Bump shape	Soldering ball
	Mounting height	0.385 mm



■ MARKING (11-pin WLP)



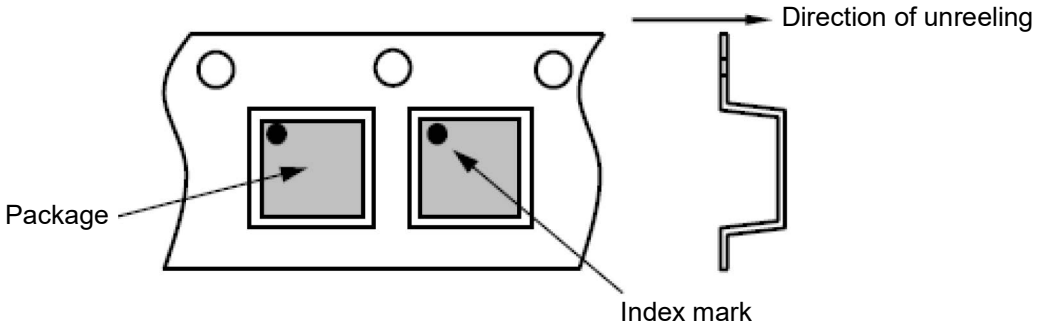
11-pin WLP Type A

AS12T	: Product name
E1	: Fixed code
2200	: Year and Week code
C00	: C (Fixed code)+00 (Trace code)

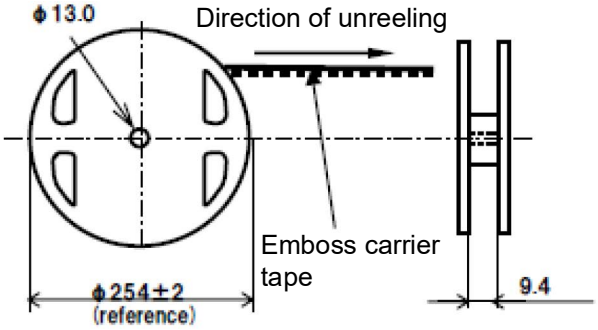
■ PACKING FIGURE

1. Emboss carrier tape and package direction of storage

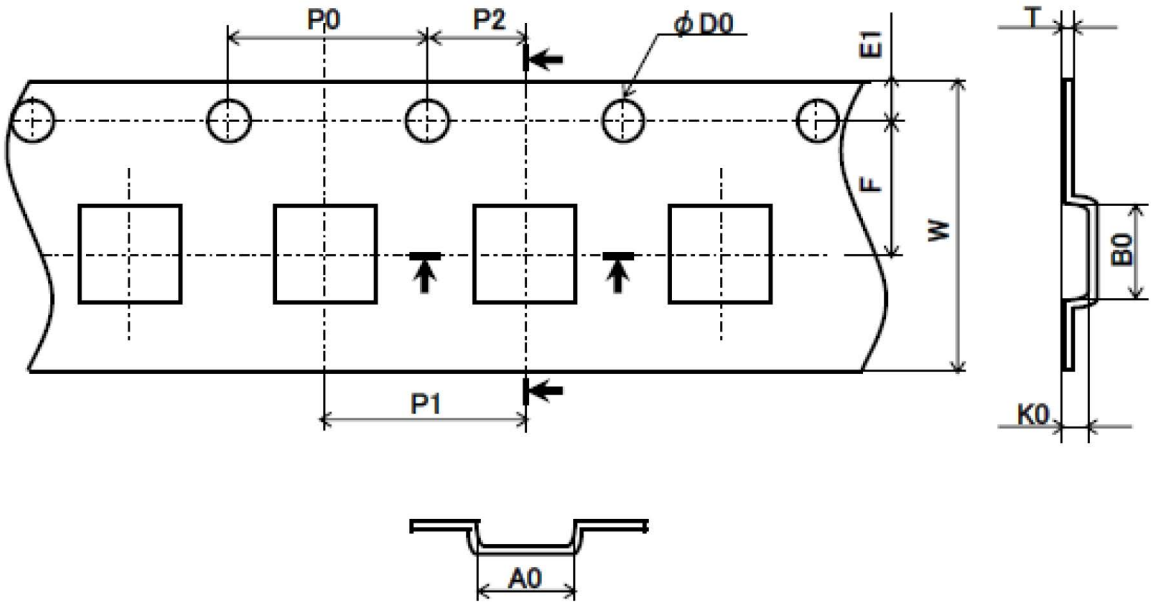
Unit: mm



2. Reel



■ EMBOSS CARRIER TAPE DRAWING



Unit: mm

Dimensions of Emboss carrier tape					
W	A0	B0	K0	T	P0
8.0 ± 0.3	2.25 ± 0.05	3.25 ± 0.05	0.60 ± 0.05	0.25 ± 0.05	4 ± 0.1
P1	P2	ϕD0	E1	F	
4 ± 0.1	2 ± 0.05	1.5 + 0.1 − 0	1.75 ± 0.1	3.5 ± 0.05	

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