

Memory FeRAM

4 M (256 K × 16) Bit

MS85R4M2TA

■ DESCRIPTIONS

The MS85R4M2TA is an FeRAM (Ferroelectric Random Access Memory) chip consisting of 262,144 words × 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MS85R4M2TA is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MS85R4M2TA can be used for 10^{14} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E2PROM. The MS85R4M2TA uses a pseudo-SRAM interface.

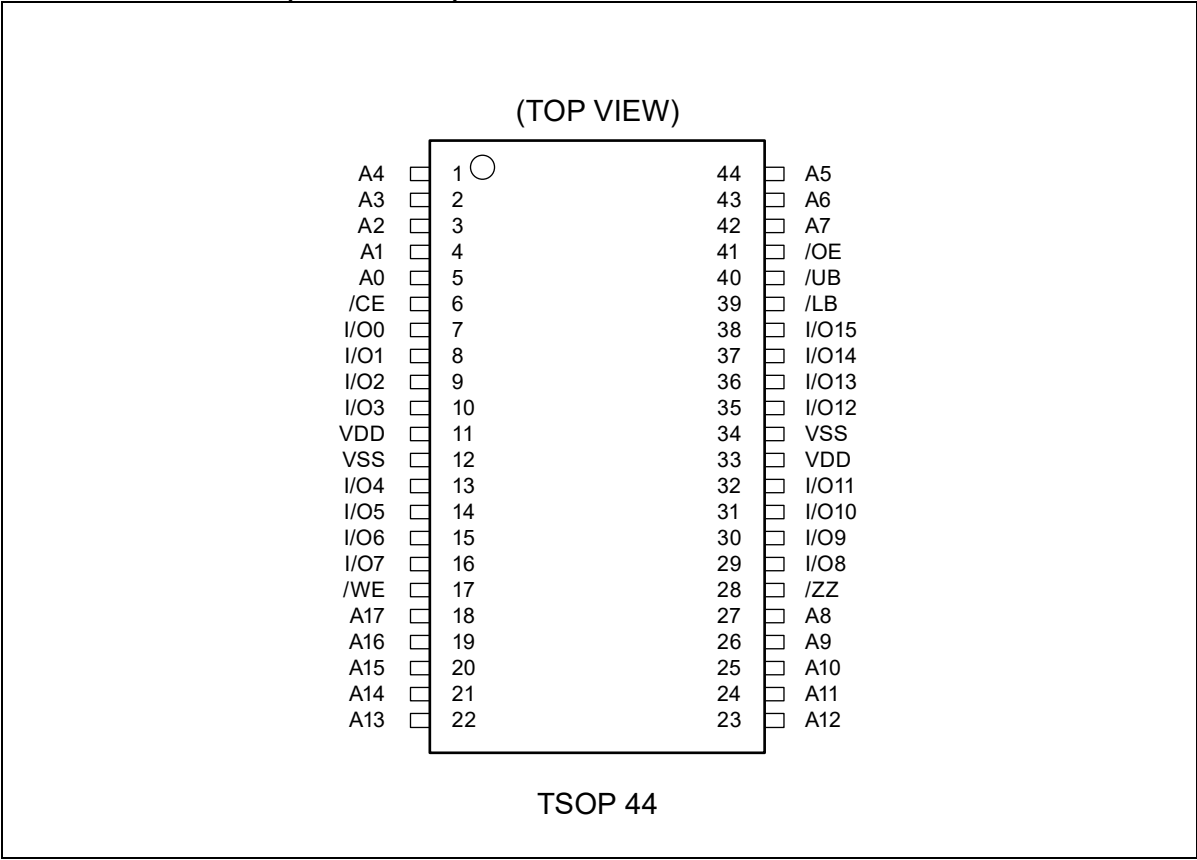
■ FEATURES

- Bit configuration : 262,144 words × 16 bits
- LB and UB data byte control : Available Configuration of 524,288 words × 8 bits
- Read/write endurance : 10^{14} times / 64 bits(+ 85 °C), 10^{13} times / 64 bits(+ 105 °C),
- Data retention : 10 years (+ 105 °C), 40 years (+ 85 °C), over 200 years (+ 35 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power operation : Operating power supply current 16 mA (Max)
Standby current 150 μA (Max)
Sleep current 12 μA (Max)
- Operation ambient temperature range : - 40 °C to + 105 °C
- Package : 44-pin plastic TSOP
RoHS compliant

MS85R4M2TA

PIN ASSIGNMENTS

PIN ASSIGNMENTS(Continued)



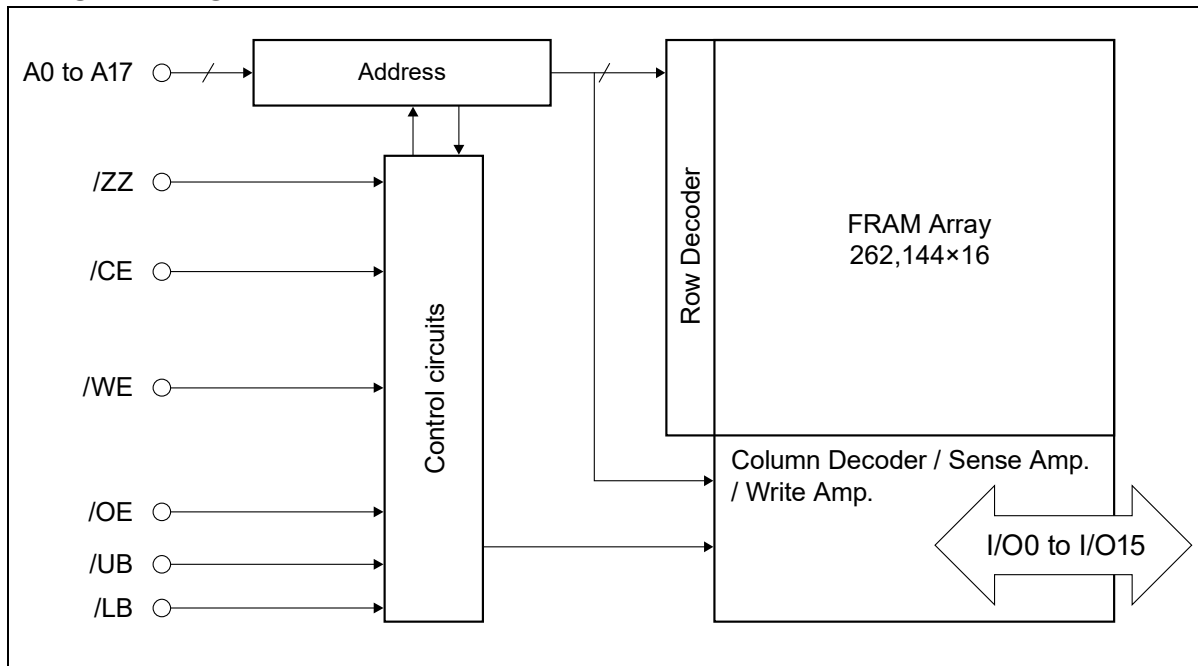
■ PIN DESCRIPTIONS

Pin Number(TSOP)	Pin Name	Functional Description
5 to 1, 44 to 42, 27 to 23, 22 to 18	A0 to A17	Address Input pins Select 262,144 words in FeRAM memory array by 18 Address Input pins. When these address inputs are changed during /CE equals to “L” level, reading operation of data selected in the address after transition will start.
7 to 10, 13 to 16, 29 to 32, 35 to 38	I/O0 to I/O15	Data Input/Output pins These are 16 bits bidirectional pins for reading and writing.
6	/CE	Chip Enable Input pin In case the /CE equals to “L” level and /ZZ equals to “H” level, device is activated and enables to start memory access. In writing operation, input data from I/O pins are latched at the rising edge of /CE and written to FeRAM memory array.
17	/WE	Write Enable Input pin Writing operation starts at the falling edge of /WE. Input data from I/O pins are latched at the rising edge of /WE and written to FeRAM memory array.
41	/OE	Output Enable Input pin When the /OE is “L” level, valid data are output to data bus. When the /OE is “H” level, all I/O pins become high impedance (High-Z) state.
28	/ZZ	Sleep Mode Input pin When the /ZZ becomes to “L” level, device transits to the Sleep Mode. During reading and writing operation, /ZZ pin shall be hold “H” level.
40, 39	/UB, /LB	Lower/Upper byte Control Input pins In case /LB or /UB equals to “L” level, it enables reading/writing operation of I/O0 to I/O7 or I/O8 to I/O15 respectively. In case /LB and /UB equal to “H” level, all I/O pins become High-Z state.
11, 33	VDD	Supply Voltage pins Connect all two pins to the power supply.
12, 34	VSS	Ground pins Connect all two pins to ground.

Note: Please refer to the timing diagram for functional description of each pin.

MS85R4M2TA

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Operation Mode	/CE	/WE	/OE	A0 to A1	A2 to A17	/ZZ	/UB,/LB
Sleep	×	×	×	×	×	L	×
Standby	H	×	×	×	×	H	×
Read(/CE Control)	↓	H	L	H or L	H or L	H	×
Address Access Read	L	H	L	H or L	↑ or ↓	H	×
Write(/CE Control)*1	↓	L	×	H or L	H or L	H	×
Write(/WE Control)*1*2	L	↓	×	H or L	H or L	H	×
Address Access Write*1*3	L	↓	×	H or L	↑ or ↓	H	×
Pre-charge	↑	×	×	×	×	H	×
Page Read	L	H	L	↑ or ↓	H or L	H	L
/UB,/LB Access Wright	L	L	H	H or L	H or L	H	↓
Page Address Write	L	↓	H	↑ or ↓	H or L	H	L

Note: H= "H" level, L= "L" level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑

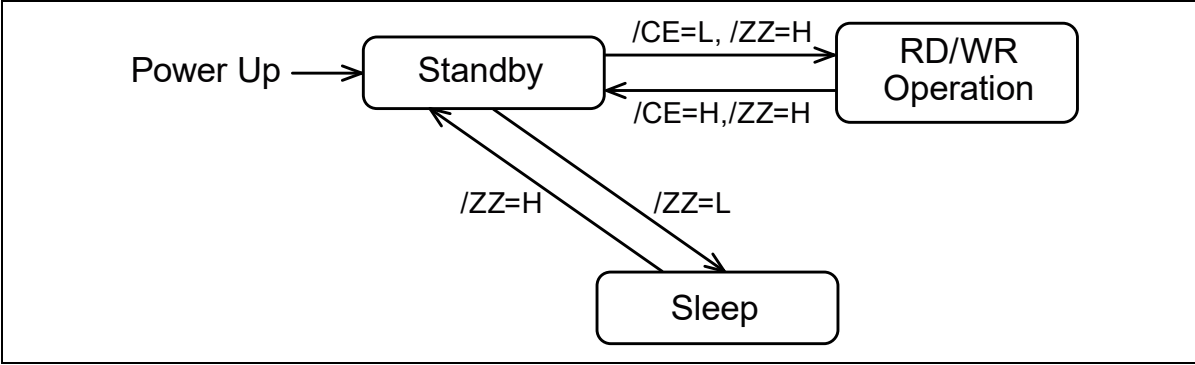
*1: In writing cycle, input data is latched at early rising edge of /CE or /WE.

*2: In writing sequence of /WE control, there exists time with data output of reading cycle at the falling edge of /CE.

*3: In writing sequence of Address Access Write, there exists time with data output of reading cycle at the address transition.

MS85R4M2TA

■ State Transition Diagram



■ FUNCTIONAL TRUTH TABLE OF BYTE CONTROL

Operation Mode	/WE	/OE	/LB	/UB	I/O0 to I/O7	I/O8 to I/O15
Read(Without Output)	H	H	×	×	Hi-Z	Hi-Z
	H	×	H	H	Hi-Z	Hi-Z
Read(I/O8 to I/O15)	H	L	H	L	Hi-Z	Output
Read(I/O0 to I/O7)			L	H	Output	Hi-Z
Read(I/O0 to I/O15)			L	L	Output	Output
Write(I/O8 to I/O15)	↑	×	H	L	×	Input
Write(I/O0 to I/O7)			L	H	Input	×
Write(I/O0 to I/O15)			L	L	Input	Input

Note: H= “H” level, L= “L” level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑
Hi-Z= High Impedance

In case the byte reading or writing are not selected, /LB and /UB pins shall be connected to GND pin.
In case the byte writing, while /CE=L, please don’t switch /LB and /UB.

■ ABABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V _{DD}	− 0.5	+ 4.0	V
Input Pin Voltage*	V _{IN}	− 0.5	V _{DD} + 0.5 (≤ 4.0)	V
Output Pin Voltage*	V _{OUT}	− 0.5	V _{DD} + 0.5 (≤ 4.0)	V
Operation Ambient Temperature	T _A	− 40	+ 105	°C
Storage Temperature	T _{stg}	− 55	+ 125	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage* ¹	V _{DD}	1.8	3.3	3.6	V
Operation Ambient Temperature* ²	T _A	− 40	—	+ 105	°C

*1: All voltages are referenced to VSS (ground 0 V).

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

MS85R4M2TA

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Sym-bol	Condition	Value				Unit
			Min	Typ	Max(TA ≤85°C)	Max(TA ≥ 85°C)	
Input Leakage Current	I _{LI}	V _{IN} = 0V to V _{DD}	—	—	5		μA
Output Leakage Current	I _{LO}	V _{OUT} = 0V to V _{DD} /CE = V _{IH} or /OE = V _{IH}	—	—	5		μA
Operating Power Supply Current*1	I _{DD}	/CE = 0.2 V, I _{out} = 0 mA	—	13.5	16	16	mA
Standby Current	I _{SB}	/ZZ ≥ V _{DD} - 0.2V /CE, /WE, /OE ≥ V _{DD} - 0.2V /LB, /UB ≥ V _{DD} - 0.2V Others ≥ V _{DD} - 0.2V or ≤ 0.2V	—	12	100	150	μA
Sleep Current	I _{ZZ}	/ZZ = V _{SS} /CE, /WE, /OE ≥ V _{DD} - 0.2V /LB, /UB ≥ V _{DD} - 0.2V Others ≥ V _{DD} - 0.2V or ≤ 0.2V	—	3.5	10	12	μA
High Level Input Voltage	V _{IH}	V _{DD} = 1.8V to 3.6V	V _{DD} × 0.8	—	V _{DD} + 0.3		V
Low Level Input Voltage	V _{IL}	V _{DD} = 1.8V to 3.6V	- 0.3	—	V _{DD} × 0.2		V
High Level Output Voltage	V _{OH1}	V _{DD} = 2.5V to 3.6V I _{OH} = - 1.0mA	V _{DD} × 0.8	—	—		V
	V _{OH2}	V _{DD} = 1.8V to 2.5V I _{OH} = - 100μA	V _{DD} - 0.2	—	—		
Low Level Output Voltage	V _{OL1}	V _{DD} = 2.5V to 3.6V I _{OL} = 2.0mA	—	—	0.4		V
	V _{OL2}	V _{DD} = 1.8V to 2.5V I _{OL} = 150μA	—	—	0.2		

*1: During the measurement of I_{DD}, all Address and I/O were taken to only change once per active cycle.

I_{out} : output current

MS85R4M2TA

2. AC Characteristics

• AC Test Conditions

Power Supply Voltage	: 1.8 V to 3.6 V
Operation Ambient Temperature	: - 40 °C to + 105 °C
Input Voltage Amplitude	: 0 V / V _{DD}
Input Rising Time	: 3 ns
Input Falling Time	: 3 ns
Input Evaluation Level	: V _{DD} /2
Output Evaluation Level	: V _{DD} /2
Output Load Capacitance	: 30 pF

(1) Read Cycle

Parameter	Symbol	TA≤+85°C				Unit
		Value (V _{DD} =1.8V to 2.5V)		Value (V _{DD} =2.5V to 3.6V)		
		Min	Max	Min	Max	
Read Cycle time(/CE control)	t _{RC}	120	—	120	—	ns
Read Cycle time(Address access)	t _{RCA}	135	—	120	—	ns
/CE Access Time	t _{CE}	—	65	—	65	ns
Address Access Time	t _{AA}	—	135	—	120	ns
/CE Output Data Hold time	t _{OH}	0	—	0	—	ns
Address Access Output Data Hold time	t _{OA} H	20	—	20	—	ns
/CE Active Time	t _{CA}	65	—	65	—	ns
Pre-charge Time	t _{PC}	55	—	55	—	ns
/LB, /UB Access Time	t _{BA}	—	35	—	20	ns
Address Setup Time	t _{AS}	0	—	0	—	ns
Address Hold Time	t _{AH}	65	—	65	—	ns
/CE↑ to Address Transition time*1	t _{CA} H	0	—	0	—	ns
/OE Access Time	t _{OE}	—	35	—	20	ns
/CE Output Floating Time*1	t _{HZ}	—	10	—	10	ns
/OE Output Floating Time	t _{OHZ}	—	10	—	10	ns
/LB, /UB Output Floating Time	t _{BHZ}	—	10	—	10	ns
Address Transition Time*1	t _{AX}	—	15	—	15	ns

*1: Same parameters with the Write cycle.

MS85R4M2TA

Parameter	Symbol	TA≥+85°C				Unit
		Value (V _{DD} =1.8V to 2.5V)		Value (V _{DD} =2.5V to 3.6V)		
		Min	Max	Min	Max	
Read Cycle time(/CE control)	t _{RC}	125	—	125	—	ns
Read Cycle time(Address access)	t _{RCA}	140	—	125	—	ns
/CE Access Time	t _{CE}	—	70	—	70	ns
Address Access Time	t _{AA}	—	140	—	125	ns
/CE Output Data Hold time	t _{OH}	0	—	0	—	ns
Address Access Output Data Hold time	t _{OA} H	20	—	20	—	ns
/CE Active Time	t _{CA}	70	—	70	—	ns
Pre-charge Time	t _{PC}	55	—	55	—	ns
/LB, /UB Access Time	t _{BA}	—	35	—	20	ns
Address Setup Time	t _{AS}	0	—	0	—	ns
Address Hold Time	t _{AH}	70	—	70	—	ns
/CE↑ to Address Transition time*1	t _{CA} H	0	—	0	—	ns
/OE Access Time	t _{OE}	—	35	—	20	ns
/CE Output Floating Time*1	t _{HZ}	—	10	—	10	ns
/OE Output Floating Time	t _{OHZ}	—	10	—	10	ns
/LB, /UB Output Floating Time	t _{BHZ}	—	10	—	10	ns
Address Transition Time*1	t _{AX}	—	15	—	15	ns

*1: Same parameters with the Write cycle.

(2) Write Cycle

Parameter	Symbol	TA≤+85°C				Unit
		Value (V _{DD} =1.8V to 2.5V)		Value (V _{DD} =2.5V to 3.6V)		
		Min	Max	Min	Max	
Write Cycle Time	t _{WC}	120	—	120	—	ns
/CE Active Time	t _{CA}	65	—	65	—	ns
/CE↓ to /WE↑ Time	t _{CW}	65	—	65	—	ns
Pre-charge Time	t _{PC}	55	—	55	—	ns
Write Pulse Width	t _{WP}	20	—	20	—	ns
Address Setup Time	t _{AS}	0	—	0	—	ns
Address Hold Time	t _{AH}	65	—	65	—	ns
/WE↓ to /CE↑ Time	t _{WLC}	20	—	20	—	ns
(/UB or /LB) ↓ to /CE ↑	t _{BLC}	20	—	20	—	ns
Address Transition to /WE↑ Time	t _{AWH}	135	—	120	—	ns
/WE↑ to Address Transition Time	t _{WHA}	0	—	0	—	ns
Data Setup Time	t _{DS}	10	—	10	—	ns
Data Hold Time	t _{DH}	0	—	0	—	ns
/WE Output Floating Time	t _{WZ}	—	10	—	10	ns
/WE Output Access Time*1	t _{WX}	10	—	10	—	ns
Write Setup Time*1	t _{WS}	0	—	0	—	ns
Write Hold Time*1	t _{WH}	0	—	0	—	ns
/CE Output Floating Time	t _{HZ}	—	10	—	10	ns
Address transition Time	t _{AX}	—	15	—	15	ns
/UB, /LB Write Pulse Width	t _{WP2}	20	—	20	—	ns
/WE=L to (/UB, /LB)=H period	t _{WP3}	20	—	20	—	ns

MS85R4M2TA

Parameter	Symbol	TA≥+85°C				Unit
		Value (V _{DD} =1.8V to 2.5V)		Value (V _{DD} =2.5V to 3.6V)		
		Min	Max	Min	Max	
Write Cycle Time	t _{WC}	125	—	125	—	ns
/CE Active Time	t _{CA}	70	—	70	—	ns
/CE↓ to /WE↑ Time	t _{CW}	70	—	70	—	ns
Pre-charge Time	t _{PC}	55	—	55	—	ns
Write Pulse Width	t _{WP}	20	—	20	—	ns
Address Setup Time	t _{AS}	0	—	0	—	ns
Address Hold Time	t _{AH}	70	—	70	—	ns
/WE↓ to /CE↑ Time	t _{WLC}	20	—	20	—	ns
(/UB or /LB) ↓ to /CE ↑	t _{BLC}	20	—	20	—	ns
Address Transition to /WE↑ Time	t _{AWH}	140	—	125	—	ns
/WE↑ to Address Transition Time	t _{WHA}	0	—	0	—	ns
Data Setup Time	t _{DS}	10	—	10	—	ns
Data Hold Time	t _{DH}	0	—	0	—	ns
/WE Output Floating Time	t _{WZ}	—	10	—	10	ns
/WE Output Access Time*1	t _{WX}	10	—	10	—	ns
Write Setup Time*1	t _{WS}	0	—	0	—	ns
Write Hold Time*1	t _{WH}	0	—	0	—	ns
/CE Output Floating Time	t _{HZ}	—	10	—	10	ns
Address transition Time	t _{AX}	—	15	—	15	ns
/UB, /LB Write Pulse Width	t _{WP2}	20	—	20	—	ns
/WE=L to (/UB, /LB)=H period	t _{WP3}	20	—	20	—	ns

(3) Page Mode Read/Write Cycle

Parameter	Symbol	Value (V _{DD} =1.8V to 2.5V)		Value (V _{DD} =2.5V to 3.6V)		Unit
		Min	Max	Min	Max	
Page Mode Write Cycle Time	t _{PWC}	25	—	25	—	ns
Page Mode Write Pulse Width	t _{WPP}	15	—	15	—	ns
Page Address Setup Time (/WE=L)	t _{ASP}	8	—	8	—	ns
Page Address Hold Time (/WE=L)	t _{AHP}	15	—	15	—	ns
Page Address Access Time	t _{AAP}	—	25	—	25	ns
Page Address Data Hold Time	t _{OHP}	3	—	3	—	ns
Page Mode Read Cycle Time	t _{PRCA}	25	—	25	—	ns
Page Mode Write Pre Charge Width	t _{WPHP}	7	—	7	—	ns

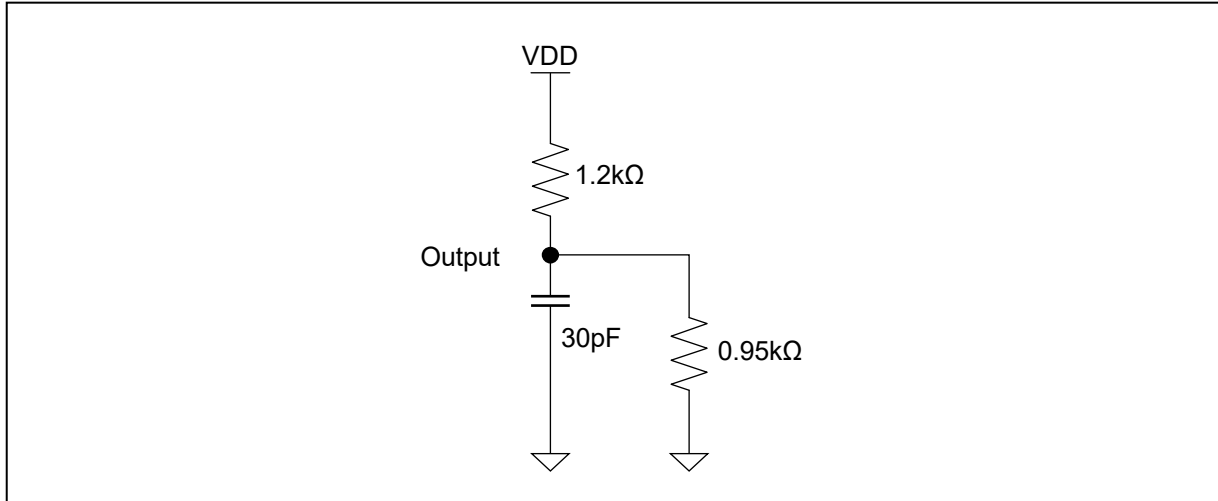
(4) Power ON/OFF Sequence and Sleep Mode Cycle

Parameter	Symbol	Value		Unit
		Min	Max	
/CE level hold time for Power ON	t _{PU}	450	—	μs
/CE level hold time for Power OFF	t _{PD}	85	—	ns
Power supply rising time	t _{VR}	50	—	μs/V
Power supply falling time	t _{VF}	100	—	μs/V
/ZZ active time	t _{ZZL}	1	—	μs
Sleep mode enable time	t _{ZZEN}	—	0	μs
/CE level hold time for Sleep mode release	t _{ZZEX}	450	—	μs

3. Pin Capacitance

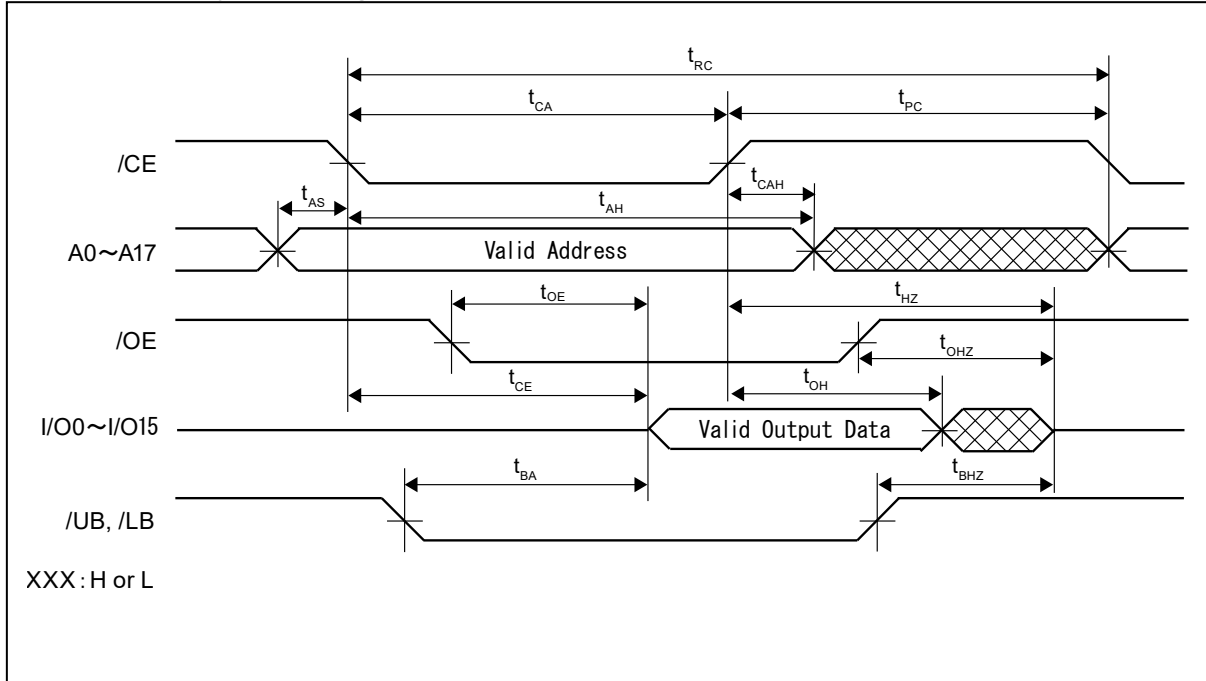
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	$V_{DD} = 3.3\text{ V}$, $f = 1\text{ MHz}$, $T_A = +25\text{ }^{\circ}\text{C}$	—	—	6	pF
Input/Output Capacitance (I/O pin)	$C_{I/O}$		—	—	8	pF
/ZZ Pin Input Capacitance	C_{ZZ}		—	—	8	pF

■ AC Test Load Circuit

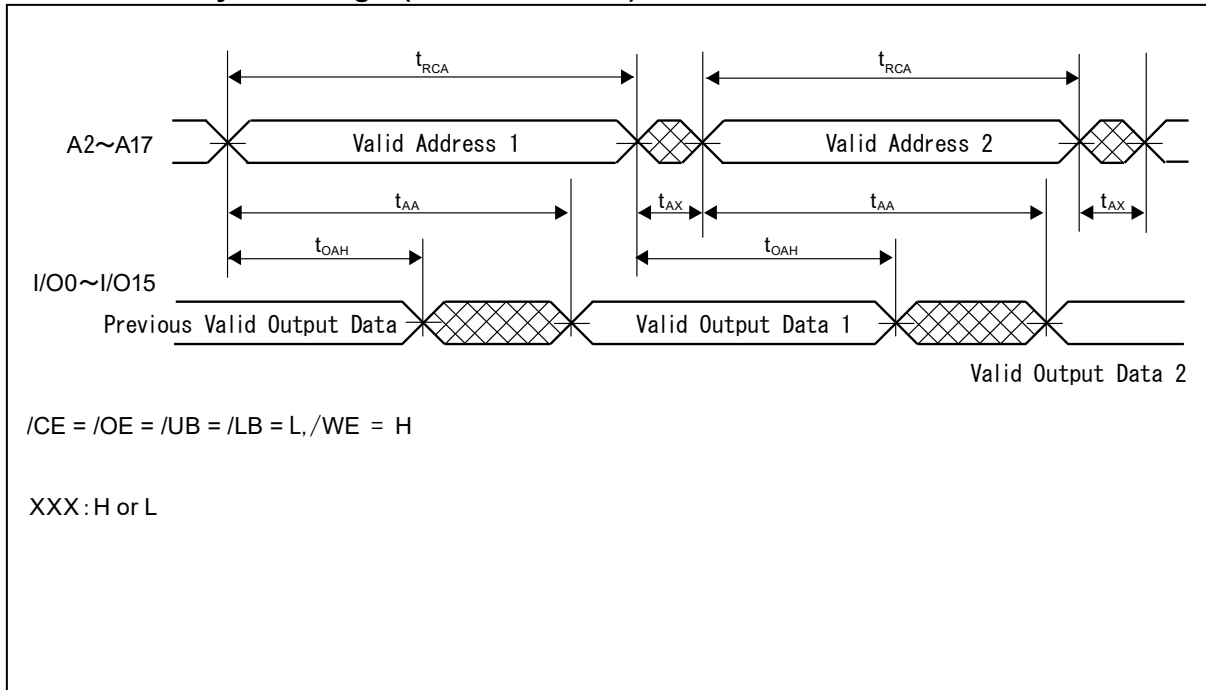


■ TIMING DIAGRAMS

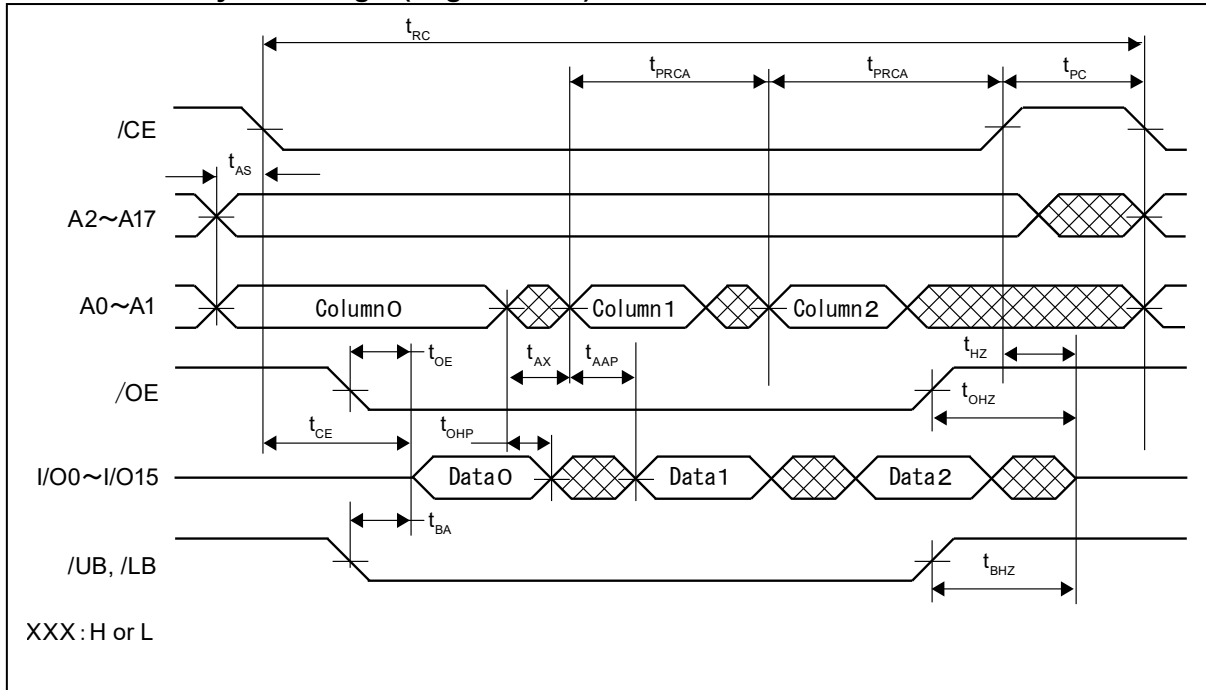
1. Read Cycle Timing 1 (/CE, /OE, /UB, /LB Control)



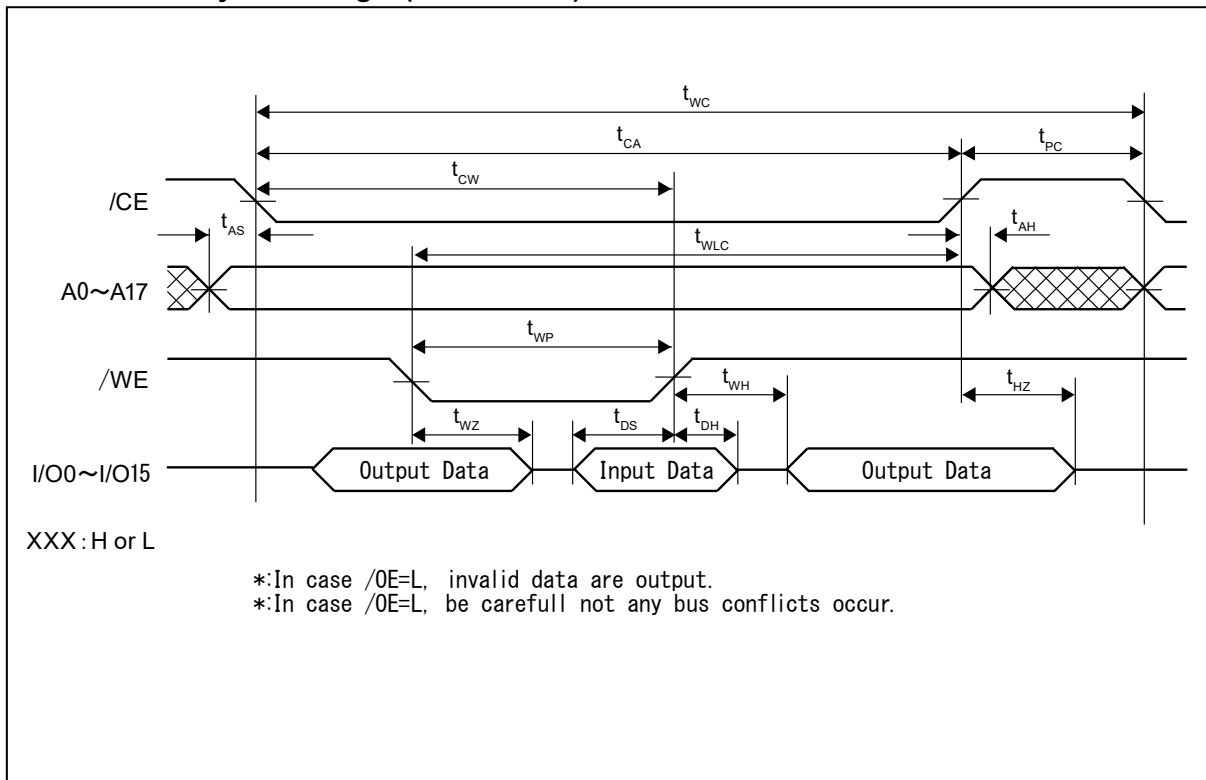
2. Read Cycle Timing 2 (Address Access)



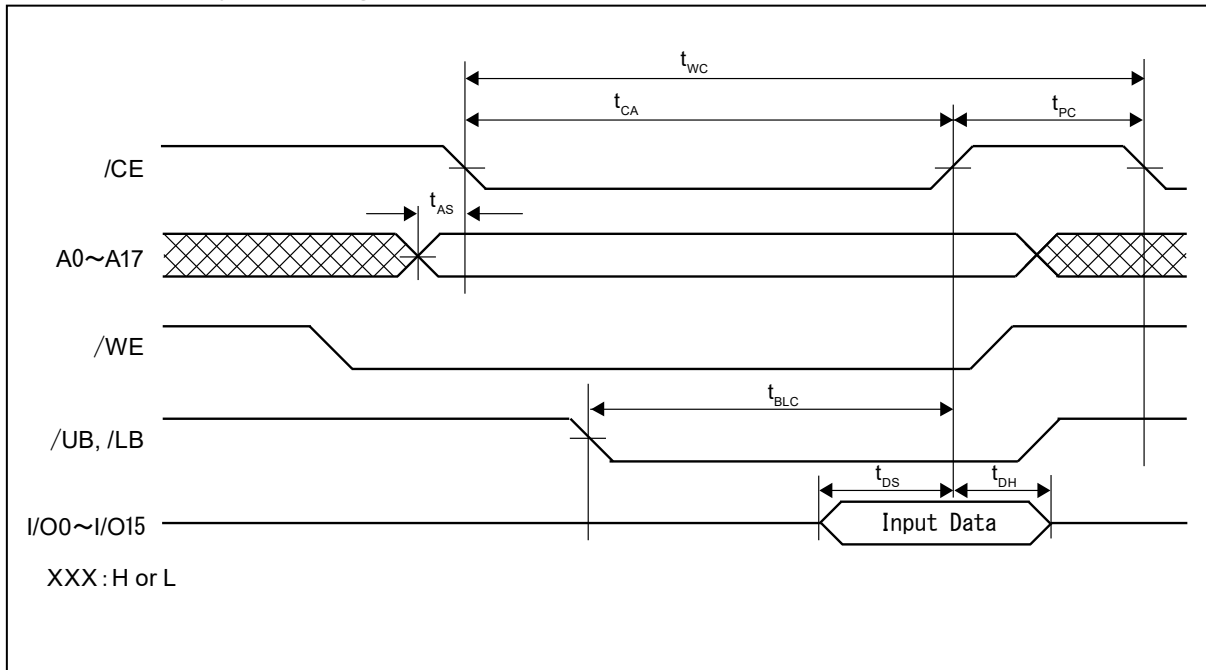
3. Read Cycle Timing 3 (Page Access)



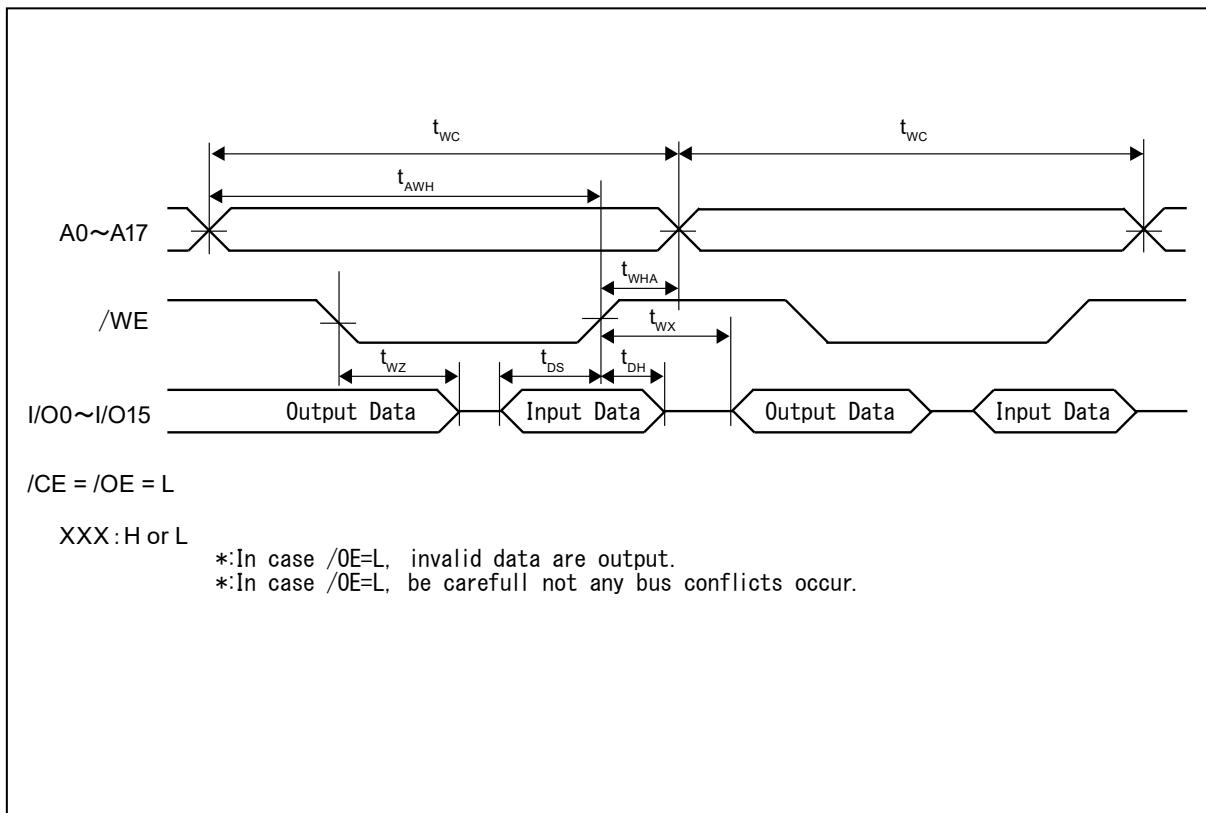
4. Write Cycle Timing 1 (/WE Control)



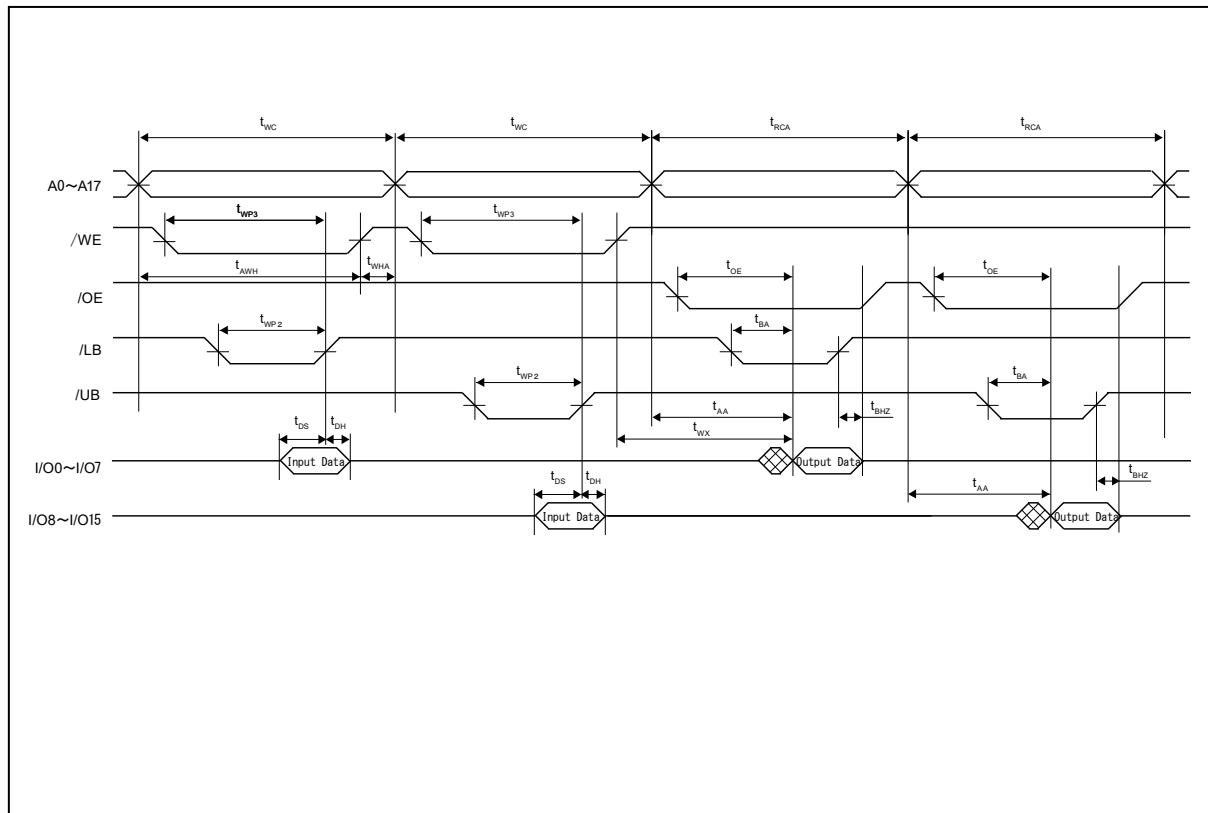
5. Write Cycle Timing 2 (/CE Control)



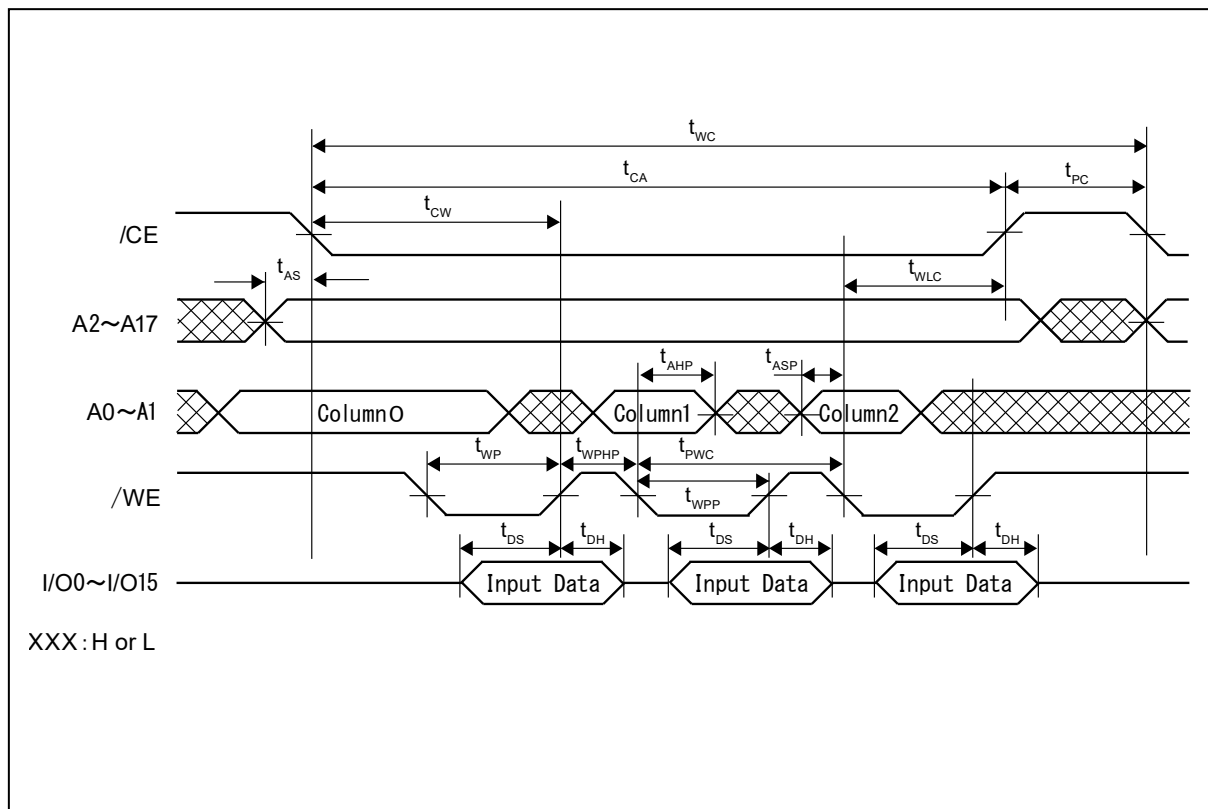
6. Write Cycle Timing 3 (Address Access and /WE Control)



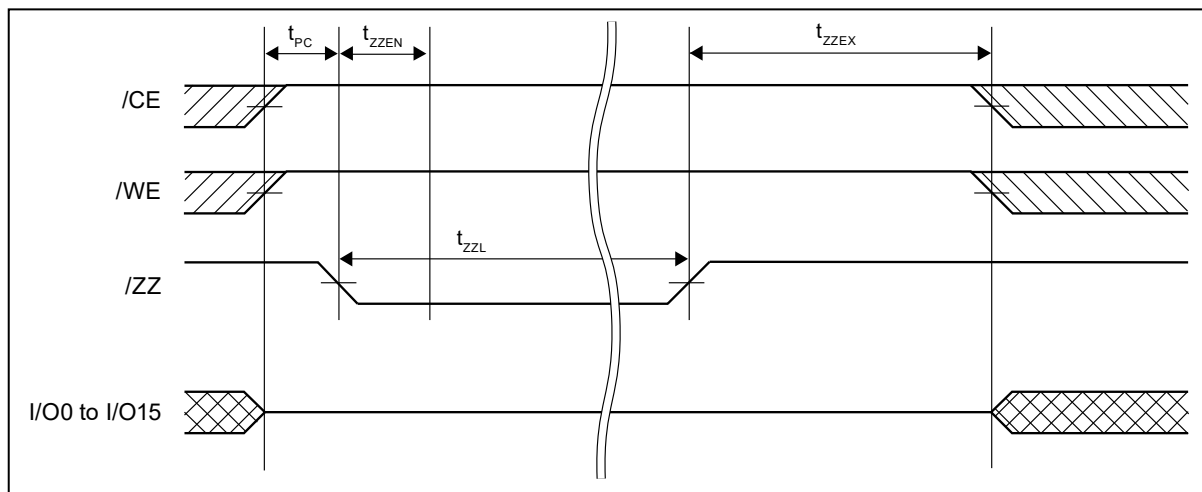
7. Write Cycle Timing 4 (/UB,/LB Access)



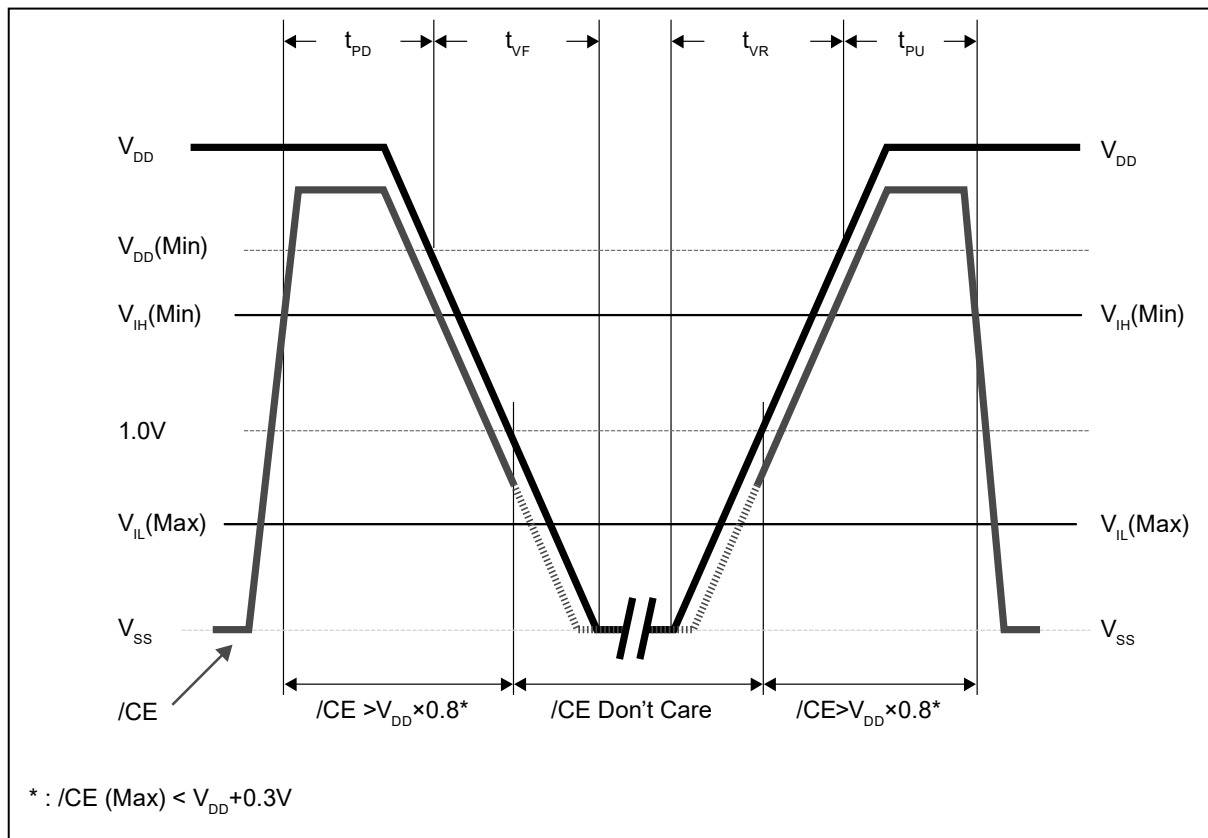
8. Write Cycle Timing 5 (Page Address Access)



9. Sleep Mode Timing



■ POWER ON/OFF SEQUENCE



When applying relatively short term VDD pulse whose peak is more than 1.7V, it is required to set falling time, t_{VF} more than 0.4ms/V. (In case VDD rises over 1.7V and falls just after that, if this term is short, device may lose its function.)

■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance ^{*1}	10^{13}	—	Times/64bits	Operation Ambient Temperature $T_A = +105\text{ }^{\circ}\text{C}$
	10^{14}	—		Operation Ambient Temperature $T_A = +85\text{ }^{\circ}\text{C}$
Data Retention ^{*2}	10	—	Years	Operation Ambient Temperature $T_A = +105\text{ }^{\circ}\text{C}$
	40	—		Operation Ambient Temperature $T_A = +85\text{ }^{\circ}\text{C}$
	95	—		Operation Ambient Temperature $T_A = +55\text{ }^{\circ}\text{C}$
	≥ 200	—		Operation Ambient Temperature $T_A = +35\text{ }^{\circ}\text{C}$

*1: Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

MS85R4M2TA

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MS85R4M2TAFN-G-JAE2	$\geq 2000 \text{ V} $
ESD CDM (Charged Device Model) JESD22-C101 compliant		$\geq 1000 \text{ V} $
Latch-Up (C-V Method) Proprietary method		$\geq 200 \text{ V} $

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

MS85R4M2TA

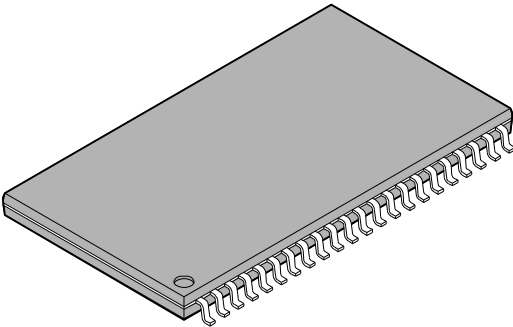
■ ORDERING INFORMATION

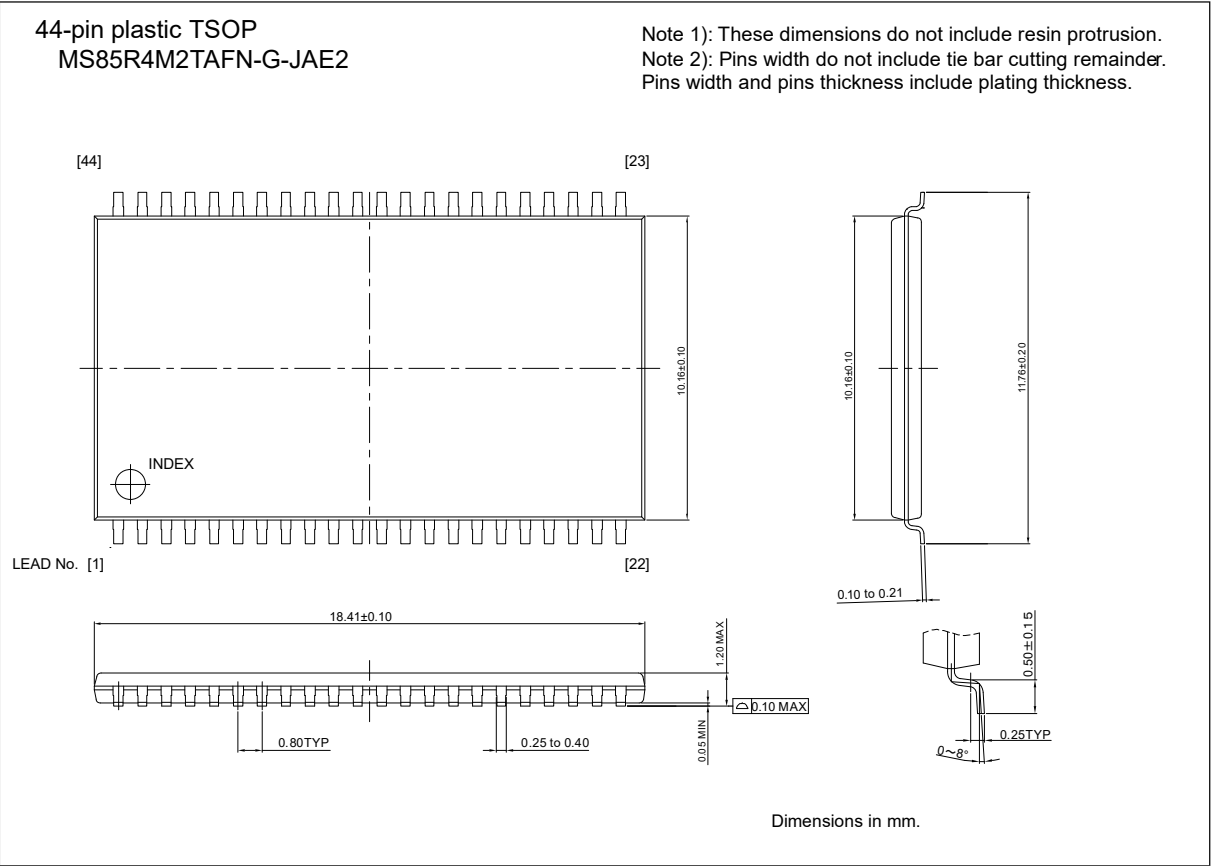
Part Number	Package	Shipping form	Minimum shipping quantity
MS85R4M2TAFN-G-JAE2	44-pin plastic TSOP	Tray	—*

*: Please contact our sales office about minimum shipping quantity.

MS85R4M2TA

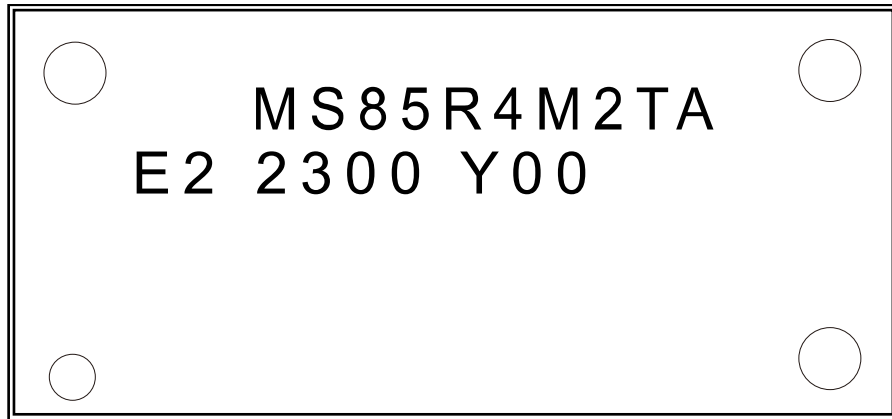
■ PACKAGE DIMENSIONS

<div>44-pin plastic TSOP</div> <div></div> <div>MS85R4M2TAFN-G-JAE2</div>	Lead pitch	0.8mm
	Package width × package length	10.16 × 18.41mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.2mm (max.)



■ MARKING(Examples)

[MS85R4M2TAFN-G-JAE2]



[44pin Plastic TSOP]

MS85R4M2TA: Product name

E2: (Lead free code)

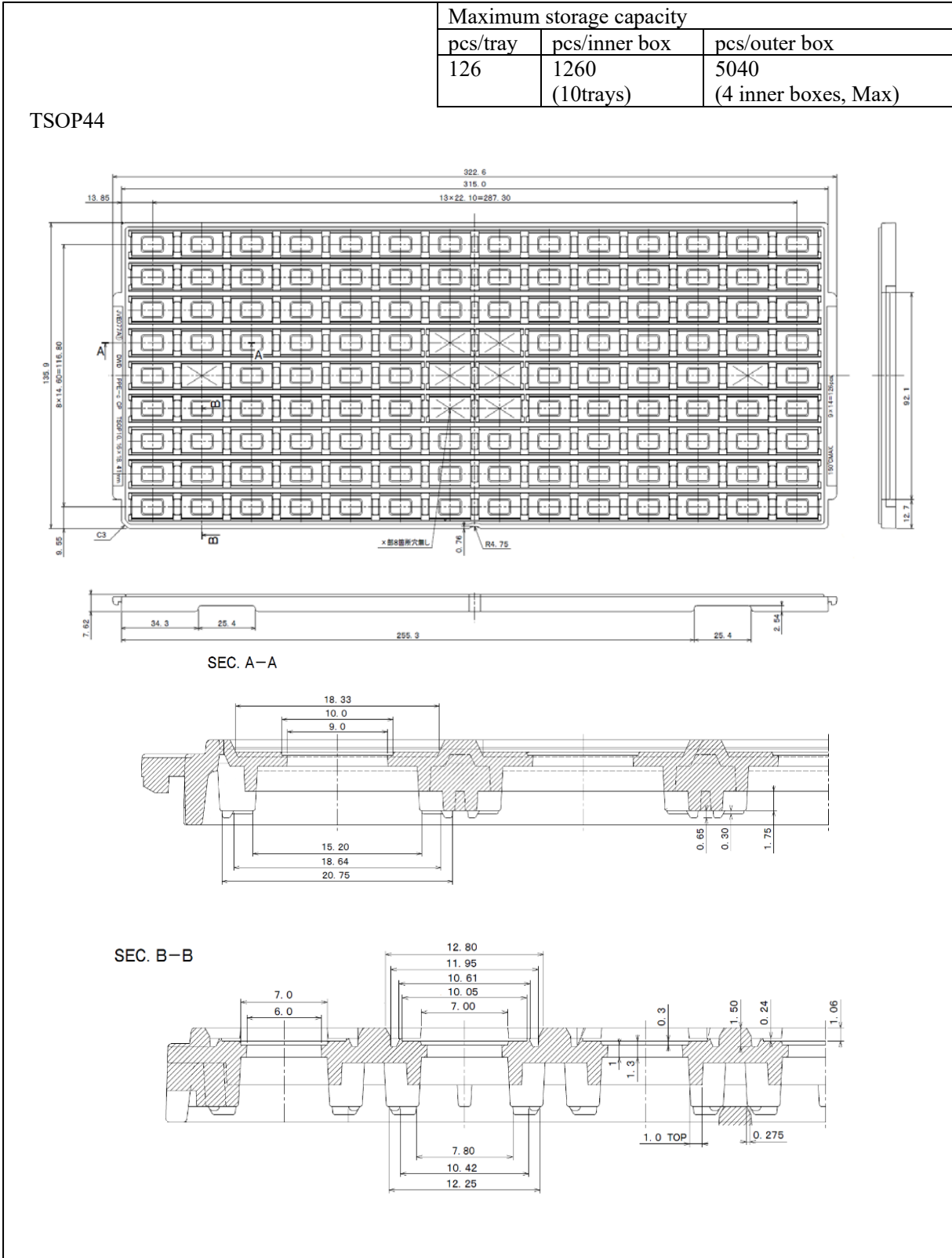
2300 Y00:2300(Year and Week code)+Y00 (Trace code)

MS85R4M2TA

■ PACKING

MS85R4M2AFN-G-JAE2

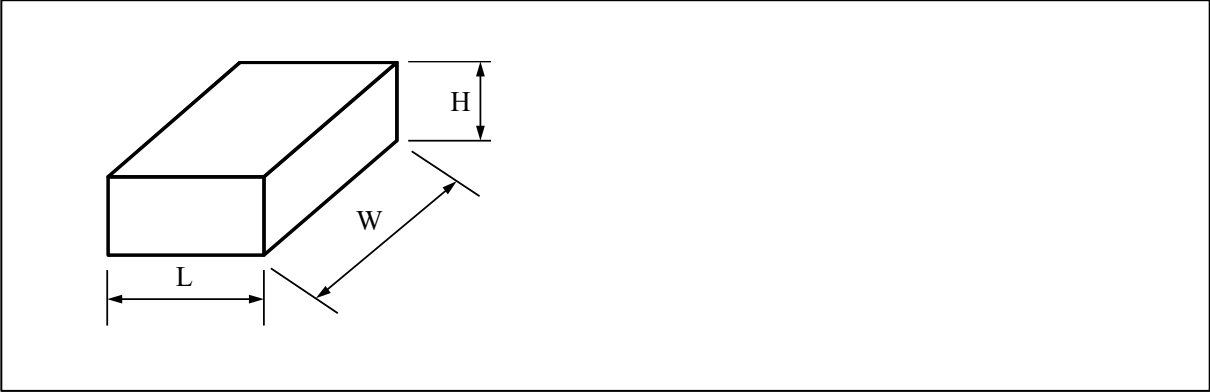
1.1 Tray dimensions



MS85R4M2TA

1.4 Dimensions for container

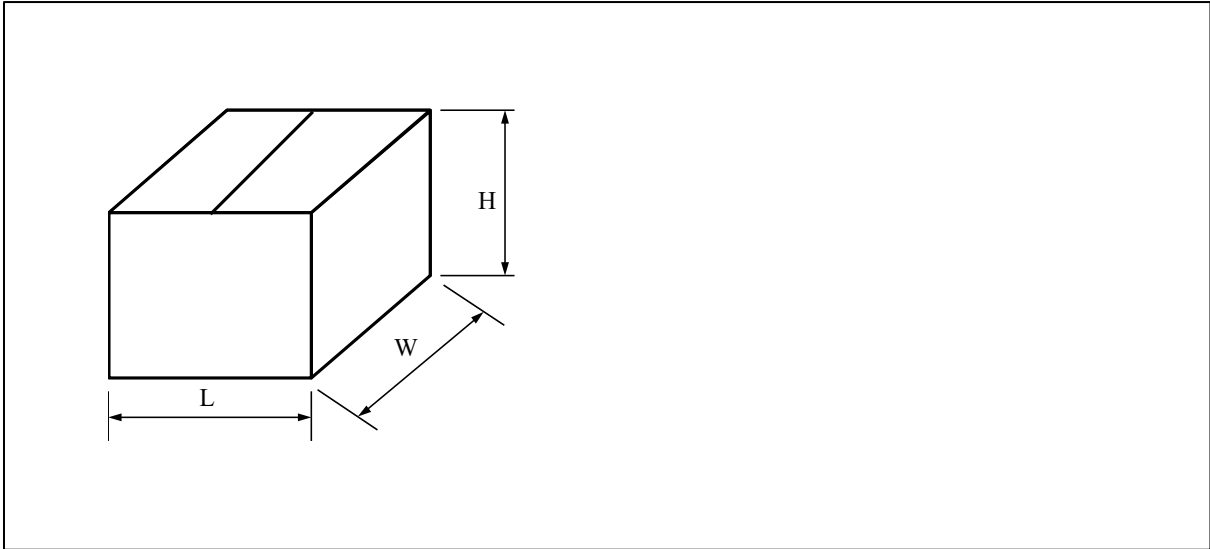
(1) Dimensions for inner box



L	W	H
162	360	90

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
410	375	225

(Dimensions in mm)

FUJITSU SEMICONDUCTOR MEMORY SOLUTION LIMITED

Shin-Yokohama Chuo Building, 2-100-45 Shin-Yokohama,
Kohoku-ku, Yokohama, Kanagawa 222-0033, Japan
<https://www.fujitsu.com/jp/fsm/en/>

All Rights Reserved.

FUJITSU SEMICONDUCTOR MEMORY SOLUTION LIMITED, its subsidiaries and affiliates (collectively, "FUJITSU SEMICONDUCTOR MEMORY SOLUTION") reserves the right to make changes to the information contained in this document without notice. Please contact your FUJITSU SEMICONDUCTOR MEMORY SOLUTION sales representatives before order of FUJITSU SEMICONDUCTOR MEMORY SOLUTION device.

Information contained in this document, such as descriptions of function and application circuit examples is presented solely for reference to examples of operations and uses of FUJITSU SEMICONDUCTOR MEMORY SOLUTION device. FUJITSU SEMICONDUCTOR MEMORY SOLUTION disclaims any and all warranties of any kind, whether express or implied, related to such information, including, without limitation, quality, accuracy, performance, proper operation of the device or non-infringement. If you develop equipment or product incorporating the FUJITSU SEMICONDUCTOR MEMORY SOLUTION device based on such information, you must assume any responsibility or liability arising out of or in connection with such information or any use thereof. FUJITSU SEMICONDUCTOR MEMORY SOLUTION assumes no responsibility or liability for any damages whatsoever arising out of or in connection with such information or any use thereof.

Nothing contained in this document shall be construed as granting or conferring any right under any patents, copyrights, or any other intellectual property rights of FUJITSU SEMICONDUCTOR MEMORY SOLUTION or any third party by license or otherwise, express or implied. FUJITSU SEMICONDUCTOR MEMORY SOLUTION assumes no responsibility or liability for any infringement of any intellectual property rights or other rights of third parties resulting from or in connection with the information contained herein or use thereof.

The products described in this document are designed, developed and manufactured as contemplated for general use including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high levels of safety is secured, could lead directly to death, personal injury, severe physical damage or other loss (including, without limitation, use in nuclear facility, aircraft flight control system, air traffic control system, mass transport control system, medical life support system and military application), or (2) for use requiring extremely high level of reliability (including, without limitation, submersible repeater and artificial satellite). FUJITSU SEMICONDUCTOR MEMORY SOLUTION shall not be liable for you and/or any third party for any claims or damages arising out of or in connection with above-mentioned uses of the products.

Any semiconductor devices fail or malfunction with some probability. You are responsible for providing adequate designs and safeguards against injury, damage or loss from such failures or malfunctions, by incorporating safety design measures into your facility, equipments and products such as redundancy, fire protection, and prevention of overcurrent levels and other abnormal operating conditions.

The products and technical information described in this document are subject to the Foreign Exchange and Foreign Trade Control Law of Japan, and may be subject to export or import laws or regulations in U.S. or other countries. You are responsible for ensuring compliance with such laws and regulations relating to export or re-export of the products and technical information described herein.

All company names, brand names and trademarks herein are property of their respective owners.