Memory FeRAM

$4 M (512 K \times 8) Bit$

MS85R4M1TA

■ DESCRIPTIONS

The MS85R4M1TA is an FeRAM (Ferroelectric Random Access Memory) chip consisting of 524,288 words × 8 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MS85R4M1TA is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MS85R4M1TA can be used for 10¹⁴ read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E2PROM. The MS85R4M1TA uses a pseudo-SRAM interface.

■ FEATURES

• Bit configuration : 524,288 words \times 8 bits

• Read/write endurance : 10¹⁴ times / 64 bits(+ 85 °C), 10¹³ times / 64 bits(+ 105 °C), • Data retention : 10 years (+ 105 °C), 40 years (+ 85 °C), over 200 years (+ 35 °C)

• Operating power supply voltage : 1.8 V to 3.6 V

• Low power operation : Operating power supply current 16 mA (Max)

Standby current 150 μA (Max) Sleep current 12 μA (Max)

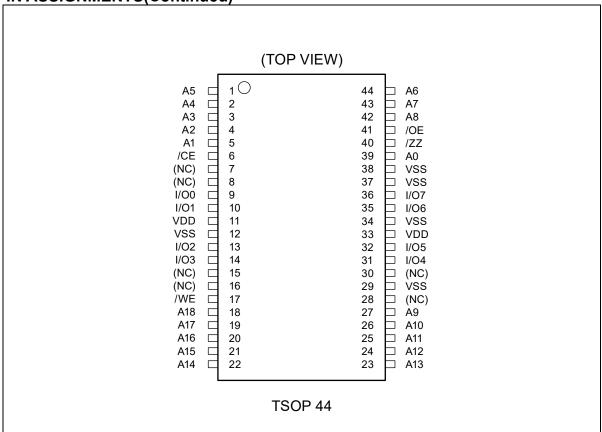
Operation ambient temperature range : -40 °C to + 105 °C
 Package : 44-pin plastic TSOP

RoHS compliant



■ PIN ASSIGNMENTS

PIN ASSIGNMENTS(Continued)

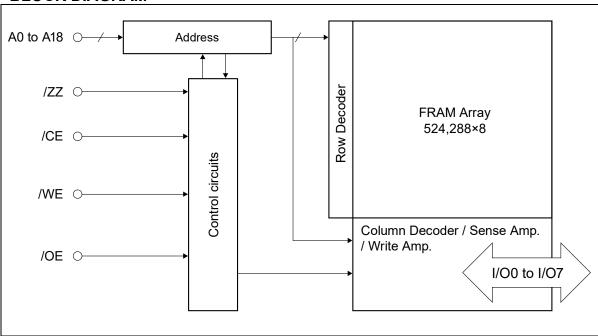


■ PIN DESCRIPTIONS

Pin Number(TSOP)	Pin Name	Functional Description
39, 5 to 1, 44 to 42,	A0 to A18	Address Input pins
27 to 18		Select 262,144 words in FeRAM memory array by 18
		Address Input pins. When these address inputs are changed
		during /CE equals to "L" level, reading operation of data
		selected in the address after transition will start.
9 to 10, 13 to 14,	I/O0 to I/O7	Data Input/Output pins
31 to 32, 35 to 36		These are 8 bits bidirectional pins for reading and writing.
6	/CE	Chip Enable Input pin
		In case the /CE equals to "L" level and /ZZ equals to "H" level,
		device is activated and enables to start memory access.
		In writing operation, input data from I/O pins are latched at
		the rising edge of /CE and written to FeRAM memory array.
17	/WE	Write Enable Input pin
		Writing operation starts at the falling edge of /WE.
		Input data from I/O pins are latched at the rising edge of /WE
		and written to FeRAM memory array.
41	/OE	Output Enable Input pin
		When the /OE is "L" level, valid data are output to data bus.
		When the /OE is "H" level, all I/O pins become high
		impedance (High-Z) state.
40	/ZZ	Sleep Mode Input pin
		When the /ZZ becomes to "L" level, device transits to the
		Sleep Mode.
		During reading and writing operation, /ZZ pin shall be hold
		"H" level.
11, 33	VDD	Supply Voltage pins
		Connect all two pins to the power supply.
12, 29, 34, 37, 38	VSS	Ground pins
		Connect all pins to ground.
7 to 8, 15 to 16, 28, 30	NC	No connected pins
		Leave them open or connect to VDD or VSS.

Note: Please refer to the timing diagram for functional description of each pin.

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Operation Mode	/CE	/WE	/OE	A0 to A2	A3 to A18	/ZZ
Sleep	×	×	×	×	×	L
Standby	Н	×	×	×	×	Н
Read(/CE Control)	\downarrow	Н	L	H or L	H or L	Н
Address Access Read	L	Н	L	H or L	↑ or ↓	Н
Write(/CE Control)*1	\downarrow	L	×	H or L	H or L	Н
Write(/WE Control)*1*2	L	\	×	H or L	H or L	Н
Address Access Write*1*3	L	\	×	H or L	↑ or ↓	Н
Pre-charge	↑	×	×	×	×	Н
Page Read	L	Н	L	↑ or ↓	H or L	Н
Page Address Write	L	\downarrow	Н	↑ or ↓	H or L	Н

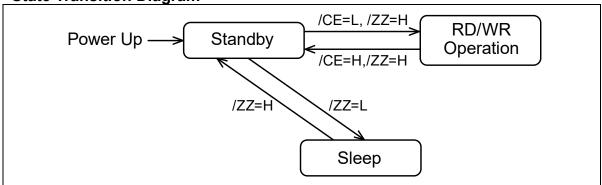
Note: H= "H" level, L= "L" level, \uparrow = Rising edge, \downarrow = Falling edge, \times = H, L, \downarrow or \uparrow

^{*1:} In writing cycle, input data is latched at early rising edge of /CE or /WE.

^{*2:} In writing sequence of /WE control, there exists time with data output of reading cycle at the falling edge of /CE.

^{*3:} In writing sequence of Address Access Write, there exists time with data output of reading cycle at the address transition.

■ State Transition Diagram



■ ABABSOLUTE MAXIMUM RATINGS

Parameter	Cumbal	Rat	ting	l lmi4
Parameter	Symbol	Min	Max	Unit
Power Supply Voltage*	V_{DD}	- 0.5	+ 4.0	V
Input Pin Voltage*	$V_{ m IN}$	- 0.5	$V_{DD} + 0.5 \ (\leq 4.0)$	V
Output Pin Voltage*	V_{OUT}	- 0.5	$V_{DD} + 0.5 \ (\leq 4.0)$	V
Operation Ambient Temperature	$T_{\mathbf{A}}$	- 40	+ 105	°C
Storage Temperature	Tstg	- 55	+ 125	°C

^{* :} All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Value		Unit
Parameter	Symbol	Min	Тур	Max	Ullit
Power Supply Voltage*1	$V_{ m DD}$	1.8	3.3	3.6	V
Operation Ambient Temperature*2	T_{A}	- 40	_	+ 105	°C

^{*1:} All voltages are referenced to VSS (ground 0 V).

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

^{*2:} Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

	Corre		(Within 18		alue	g conditions)	
Parameter	Sym -bol	Condition	Min	Тур	Max(TA ≤85°C)	Max(TA ≥ 85°C)	Unit
Input Leakage Current	$ \mathrm{I}_{\mathrm{LI}} $	$V_{IN} = 0V$ to V_{DD}	_	_	4	5	μΑ
Output Leakage Current	$ { m I_{LO}} $	$V_{OUT} = 0V$ to V_{DD} /CE = V_{IH} or /OE = V_{IH}	_	_		5	μΑ
Operating Power Supply Current*1	I_{DD}	$/CE = 0.2 \text{ V}, I_{out} = 0 \text{ mA}$	_	13.5	16	16	mA
Standby Current	I_{SB}	$\label{eq:ZZ} \begin{split} /ZZ \ge V_{DD} - 0.2V \\ /CE, /WE, /OE \ge V_{DD} - 0.2V \\ Others \ge V_{DD} - 0.2V \text{ or } \le 0.2V \end{split}$	_	12	100	150	μΑ
Sleep Current	I _{ZZ}	$\label{eq:ZZ=VSS} \begin{split} /ZZ &= V_{SS} \\ /CE, /WE, /OE &\geq V_{DD} - 0.2V \\ Others &\geq V_{DD} - 0.2V \text{ or } \leq 0.2V \end{split}$	_	3.5	10	12	μΑ
High Level Input Voltage	V_{IH}	$V_{DD} = 1.8V \text{ to } 3.6V$	$V_{DD} \times 0.8$		V_{DD}	+ 0.3	V
Low Level Input Voltage	V_{IL}	$V_{DD} = 1.8V \text{ to } 3.6V$	- 0.3		V_{DD}	× 0.2	V
High Level	V_{OH1}	$V_{DD} = 2.5V \text{ to } 3.6V$ $I_{OH} = -1.0\text{mA}$	$V_{DD} \times 0.8$	_	_	_	V
Output Voltage	V_{OH2}	$V_{DD} = 1.8V \text{ to } 2.5V$ $I_{OH} = -100\mu\text{A}$	$V_{DD} - 0.2$		_	_	V
Low Level	V_{OL1}	$V_{DD} = 2.5V \text{ to } 3.6V$ $I_{OL} = 2.0\text{mA}$	_	_	0	.4	V
Output Voltage	V_{OL2}	$V_{DD} = 1.8V \text{ to } 2.5V$ $I_{OL} = 150 \mu A$	_	_	0	.2	v

^{*1:} During the measurement of I_{DD}, all Address and I/O were taken to only change once per active cycle.

Iout: output current

2. AC Characteristics

AC Test Conditions

 $\begin{array}{ll} Power \ Supply \ Voltage & : 1.8 \ V \ to \ 3.6 \ V \\ Operation \ Ambient \ Temperature & : -40 \ ^{\circ}C \ to \ +105 \ ^{\circ}C \\ Input \ Voltage \ Amplitude & : 0 \ V \ / \ V_{DD} \end{array}$

 $\begin{array}{lll} \text{Input Voltage Amplitude} & : 0 \text{ V} / \text{V}_{DI} \\ \text{Input Rising Time} & : 3 \text{ ns} \\ \text{Input Falling Time} & : 3 \text{ ns} \\ \text{Input Evaluation Level} & : \text{V}_{DD}/2 \\ \text{Output Evaluation Level} & : \text{V}_{DD}/2 \\ \text{Output Load Capacitance} & : 30 \text{ pF} \\ \end{array}$

(1) Read Cycle

			TA≤+	85°C		
Parameter	Symbol		alue	Value		Unit
i didilictei	Cymbol	(V _{DD} =1.8	V to 2.5V)	(V _{DD} =2.5V t	o 3.6V)	01111
		Min	Max	Min	Max	
Read Cycle time(/CE control)	$t_{ m RC}$	120	_	120	_	ns
Read Cycle time(Address access)	t_{RCA}	135	_	120	_	ns
/CE Access Time	t_{CE}		65		65	ns
Address Access Time	t_{AA}		135		120	ns
/CE Output Data Hold time	t_{OH}	0	_	0	_	ns
Address Access Output Data Hold	tour	20		20		ne
time	t _{OAH}	20	_	20		ns
/CE Active Time	t_{CA}	65	_	65	_	ns
Pre-charge Time	$t_{\rm PC}$	55	_	55	_	ns
Address Setup Time	t_{AS}	0	_	0	_	ns
Address Hold Time	t_{AH}	65	_	65	_	ns
/CE↑ to Address Transition time*1	tcah	0	_	0	_	ns
/OE Access Time	t_{OE}	_	35	_	20	ns
/CE Output Floating Time*1	$t_{\rm HZ}$		10		10	ns
/OE Output Floating Time	t _{OHZ}		10	_	10	ns
Address Transition Time*1	t_{AX}	_	15	_	15	ns

^{*1:} Same parameters with the Write cycle.

			TA≥+	85 °C		
Parameter	Symbol	Symbol		Value	Unit	
i diametei	Symbol	(V _{DD} =1.8	V to 2.5V)	(V _{DD} =2.5V t	o 3.6V)	Oilit
		Min	Max	Min	Max	
Read Cycle time(/CE control)	$t_{ m RC}$	125	_	125	_	ns
Read Cycle time(Address access)	$t_{ m RCA}$	140	_	125	_	ns
/CE Access Time	$t_{\rm CE}$	_	70		70	ns
Address Access Time	t_{AA}	_	140		125	ns
/CE Output Data Hold time	t_{OH}	0	_	0	_	ns
Address Access Output Data Hold	+	20		20		na
time	t _{OAH} 20	20	_	20		ns
/CE Active Time	t_{CA}	70	_	70	_	ns
Pre-charge Time	t_{PC}	55	_	55	_	ns
Address Setup Time	t_{AS}	0	_	0	_	ns
Address Hold Time	$t_{ m AH}$	70	_	70	_	ns
/CE↑ to Address Transition time*1	tcah	0	_	0	_	ns
/OE Access Time	t_{OE}		35	_	20	ns
/CE Output Floating Time*1	$t_{\rm HZ}$	_	10	_	10	ns
/OE Output Floating Time	t _{OHZ}		10		10	ns
Address Transition Time*1	t_{AX}	_	15	_	15	ns

^{*1:} Same parameters with the Write cycle.

(2) Write Cycle

			TA≤+	85°C		
Parameter	Symbol		lue		lue	Unit
	Cymber .	(V _{DD} =1.8\	/ to 2.5V)	(V _{DD} =2.5)	/ to 3.6V)	
		Min	Max	Min	Max	
Write Cycle Time	$t_{ m WC}$	120	_	120		ns
/CE Active Time	t_{CA}	65		65	_	ns
/CE↓ to /WE↑ Time	$t_{\rm CW}$	65		65	_	ns
Pre-charge Time	t_{PC}	55		55	_	ns
Write Pulse Width	t_{WP}	20		20	_	ns
Address Setup Time	t_{AS}	0	_	0	_	ns
Address Hold Time	t_{AH}	65	_	65	_	ns
/WE↓ to /CE↑ Time	$t_{ m WLC}$	20		20	_	ns
Address Transition to /WE↑ Time	$t_{ m AWH}$	135		120	_	ns
/WE↑ to Address Transition Time	$t_{ m WHA}$	0		0	_	ns
Data Setup Time	$t_{ m DS}$	10		10	_	ns
Data Hold Time	$t_{ m DH}$	0		0	_	ns
/WE Output Floating Time	$t_{ m WZ}$		10	_	10	ns
/WE Output Access Time*1	t_{WX}	10		10	_	ns
Write Setup Time*1	$t_{ m WS}$	0		0	_	ns
Write Hold Time*1	$t_{ m WH}$	0		0		ns
/CE Output Floating Time	$t_{\rm HZ}$		10		10	ns
Address transition Time	t_{AX}	_	15	_	15	ns

			TA≥+	85 °C		
Parameter	Symbol	Va	lue	Va	lue	Unit
Parameter	Symbol	(V _{DD} =1.8\	/ to 2.5V)	(V _{DD} =2.5)	√ to 3.6V)	Ullit
		Min	Max	Min	Max	
Write Cycle Time	$t_{ m WC}$	125		125		ns
/CE Active Time	t_{CA}	70		70		ns
/CE↓ to /WE↑ Time	t_{CW}	70		70		ns
Pre-charge Time	t_{PC}	55		55		ns
Write Pulse Width	t_{WP}	20		20		ns
Address Setup Time	t_{AS}	0		0		ns
Address Hold Time	t_{AH}	70		70		ns
/WE↓ to /CE↑ Time	$t_{ m WLC}$	20		20		ns
Address Transition to /WE↑ Time	$t_{ m AWH}$	140		125		ns
/WE↑ to Address Transition Time	$t_{ m WHA}$	0		0		ns
Data Setup Time	$t_{ m DS}$	10		10	_	ns
Data Hold Time	$t_{ m DH}$	0		0		ns
/WE Output Floating Time	t_{WZ}		10		10	ns
/WE Output Access Time*1	t_{WX}	10		10		ns
Write Setup Time*1	t_{WS}	0		0		ns
Write Hold Time*1	$t_{ m WH}$	0	_	0	_	ns
/CE Output Floating Time	$t_{\rm HZ}$		10		10	ns
Address transition Time	t_{AX}		15		15	ns

(3) Page Mode Read/Write Cycle

Parameter	Symbol	Value (V _{DD} =1.8V to 2.5V)		Value (V _{DD} =2.5V to 3.6V)		Unit
		Min	Max	Min	Max	
Page Mode Write Cycle Time	t_{PWC}	25		25	_	ns
Page Mode Write Pulse Width	t_{WPP}	15		15	_	ns
Page Address Setup Time (/WE=L)	t_{ASP}	8	_	8	_	ns
Page Address Hold Time (/WE=L)	t_{AHP}	15	_	15	_	ns
Page Address Access Time	t_{AAP}		25	_	25	ns
Page Address Data Hold Time	$t_{ m OHP}$	3		3	_	ns
Page Mode Read Cycle Time	t _{PRCA}	25		25	_	ns
Page Mode Write Pre Charge Width	t_{WPHP}	7	_	7	_	ns

(4) Power ON/OFF Sequence and Sleep Mode Cycle

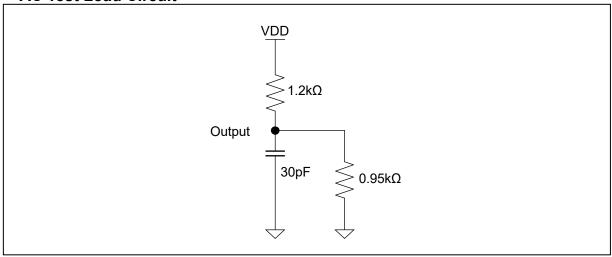
Davamatar	Cumbal	Va	lue	Hois
Parameter	Symbol	Min	Max	Unit
/CE level hold time for Power ON	$t_{ m PU}$	450	_	μs
/CE level hold time for Power OFF	$t_{ m PD}$	85	_	ns
Power supply rising time	$t_{ m VR}$	50	_	μs/V
Power supply falling time	$t_{ m VF}$	100	_	μs/V
/ZZ active time	t_{ZZL}	1	_	μs
Sleep mode enable time	t_{ZZEN}	-	0	μs
/CE level hold time for Sleep mode release	t_{ZZEX}	450	_	μs

10

3. Pin Capacitance

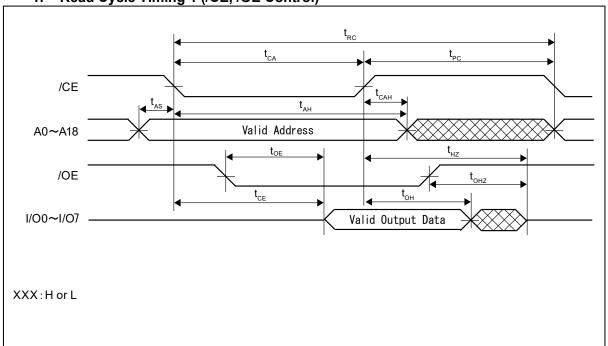
Parameter	Symbol	Condition		Value		Unit
Farailletei	Syllibol	Condition	Min	Тур	Max	Oilit
Input Capacitance	C_{IN}	N -22N	_	_	6	pF
Input/Output Capacitance (I/O pin)	C _{I/O}	$V_{DD} = 3.3 \text{ V},$ $f = 1 \text{ MHz}, T_A = +25 \text{ °C}$	_	_	8	pF
/ZZ Pin Input Capacitance	C_{ZZ}	$\begin{bmatrix} 1-1 \text{ MHz}, 1_A-+23 \end{bmatrix}$	_	_	8	pF

■ AC Test Load Circuit

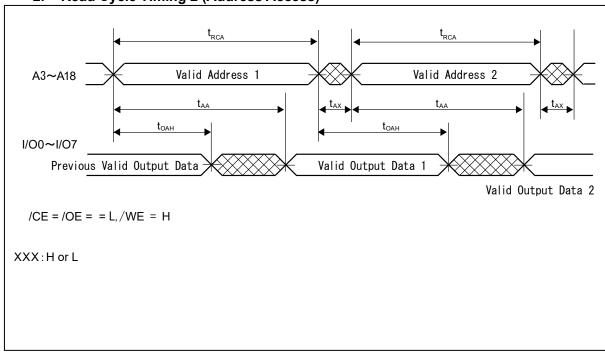


■ TIMING DIAGRAMS

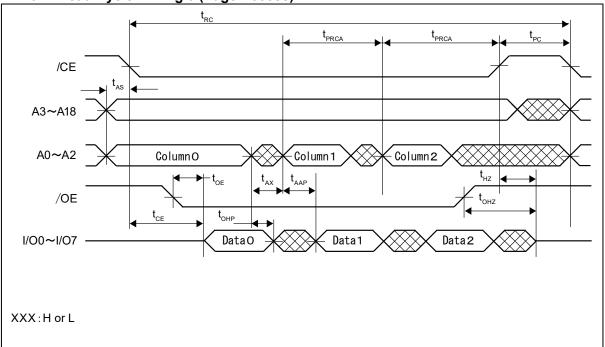
1. Read Cycle Timing 1 (/CE, /OE Control)



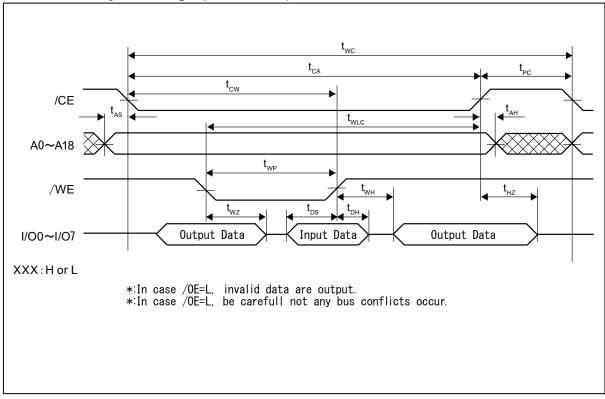
2. Read Cycle Timing 2 (Address Access)



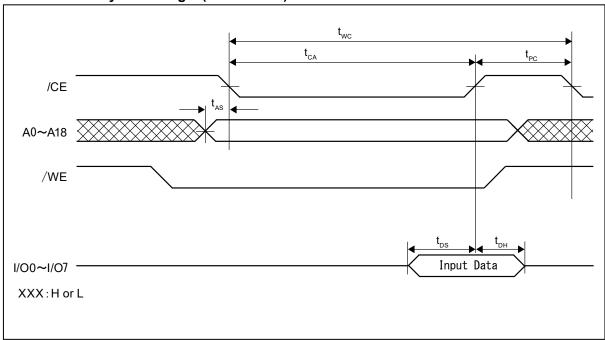
3. Read Cycle Timing 3 (Page Access)



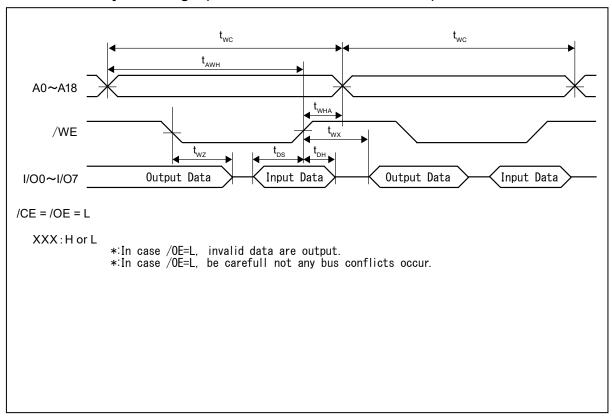
4. Write Cycle Timing 1 (/WE Control)



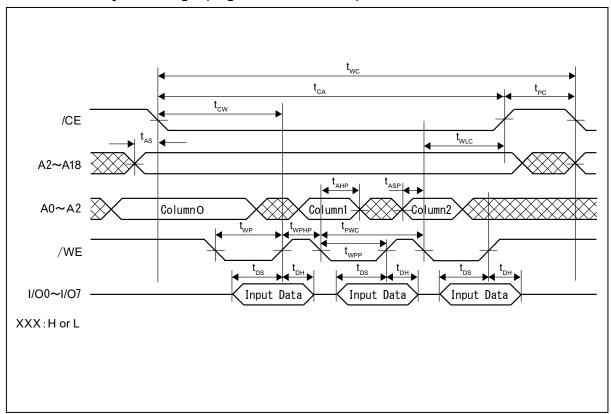
5. Write Cycle Timing 2 (/CE Control)



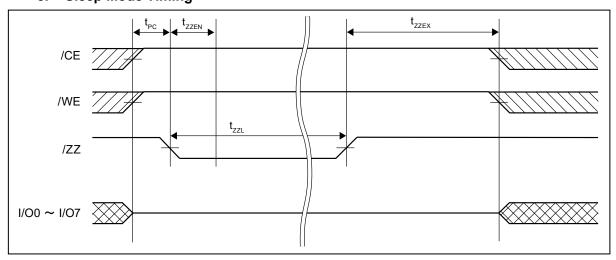
6. Write Cycle Timing 3 (Address Access and /WE Control)



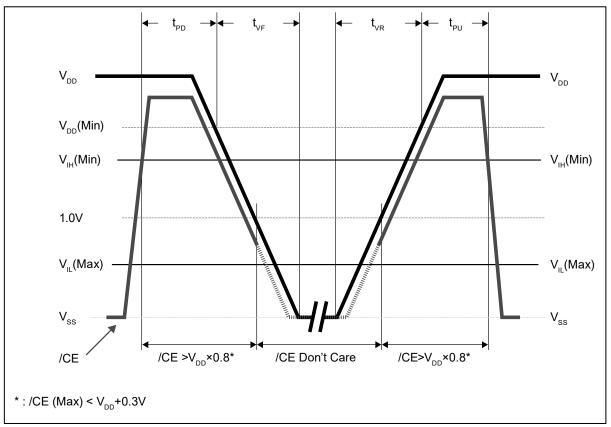
7. Write Cycle Timing 5 (Page Address Access)



8. Sleep Mode Timing



■ POWER ON/OFF SEQUENCE



When applying relatively short term VDD pulse whose peak is more than 1.7V, it is required to set falling time, t_{VF} more than 0.4ms/V. (In case VDD rises over 1.7V and falls just after that, if this term is short, device may lose its function.)

■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{13}		Time og /6 /lhita	Operation Ambient Temperature $T_A = +105 ^{\circ}\text{C}$
Read/Write Endurance	10^{14}	_	Times/64bits Operation Ambient Temperature $T_A = +85$ °C	
	10 —		Operation Ambient Temperature $T_A = +105 ^{\circ}\text{C}$	
Data Retention*2	40		Years	Operation Ambient Temperature $T_A = +85 ^{\circ}\text{C}$
	95			Operation Ambient Temperature $T_A = +55 ^{\circ}\text{C}$
	≥ 200	_		Operation Ambient Temperature $T_A = +35$ °C

^{*1:} Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

■ NOTE ON USE

• We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

^{*2:} Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model)		> 2000 V/
JESD22-A114 compliant		≥ 2000 V
ESD CDM (Charged Device Model)	MCOSDAMITAENIC IAES	≥ 1000 V
JESD22-C101 compliant	MS85R4M1TAFN-G-JAE2	
Latch-Up (C-V Method)		> 200 V
Proprietary method		≥ 200 V

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

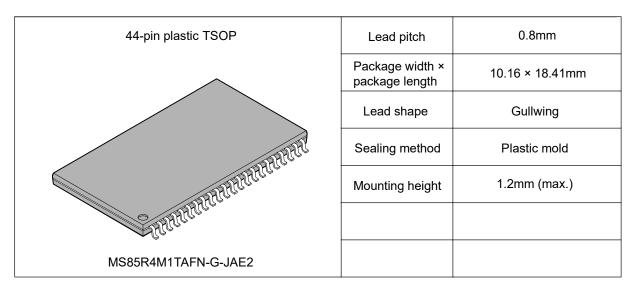
■ ORDERING INFORMATION

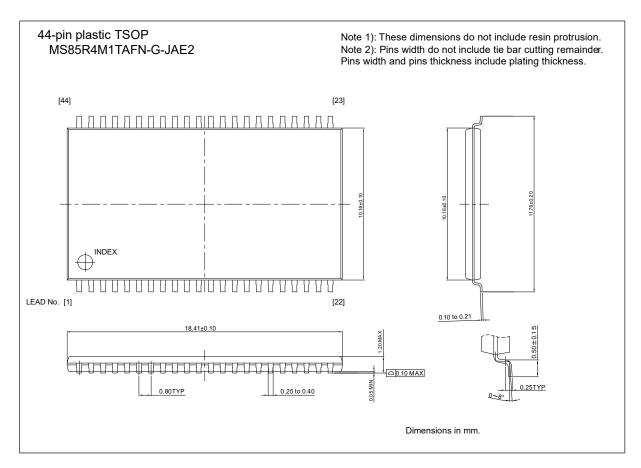
Part Number	Package	Shipping form	Minimum shipping quantity
MS85R4M1TAFN-G-JAE2	44-pin plastic TSOP	Tray	*

^{*:} Please contact our sales office about minimum shipping quantity.

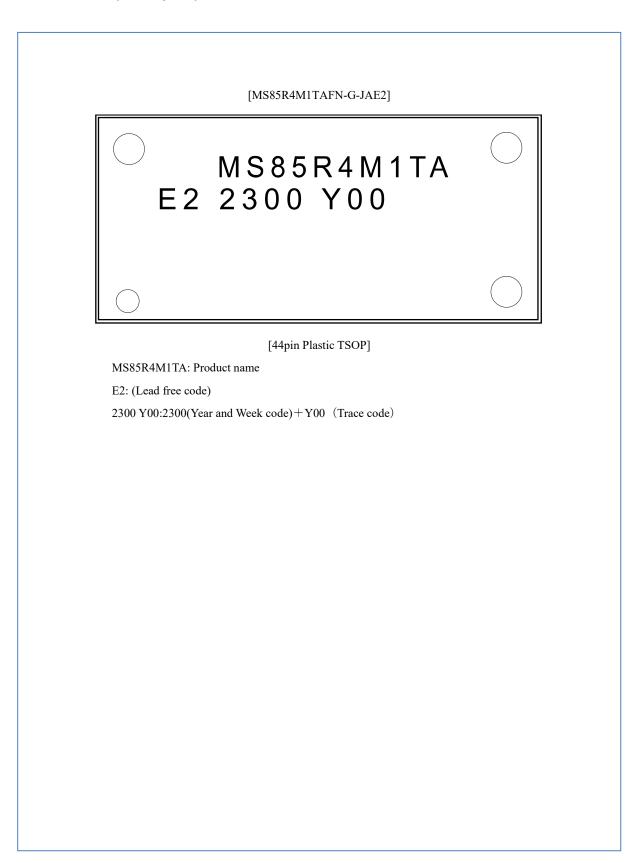


■ PACKAGE DIMENSIONS





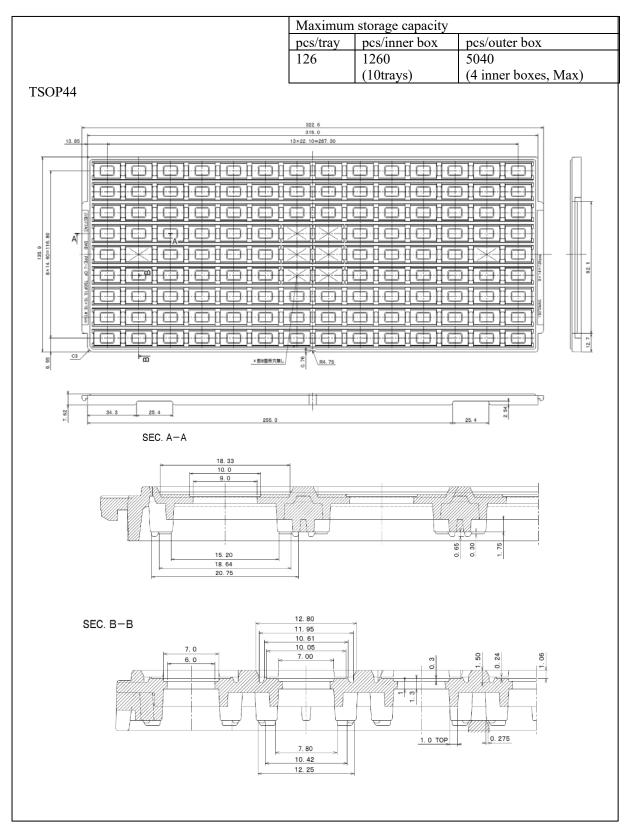
■ MARKING(Examples)



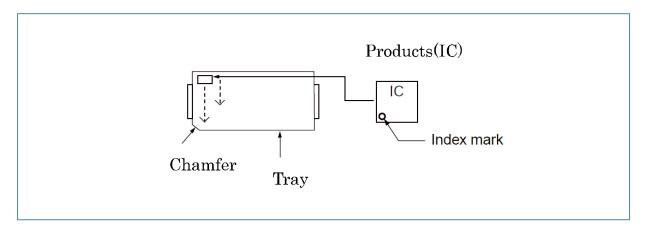
■ PACKING

MS85R4M1TAFN-G-JAE2

1.1 Tray dimensions

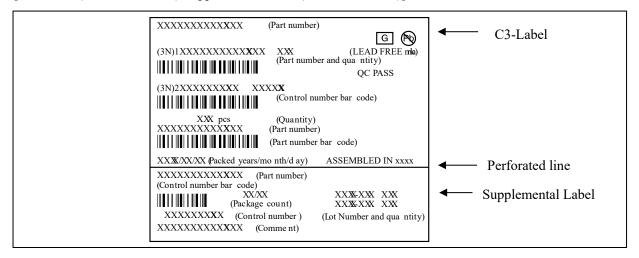


1.2 IC orientation



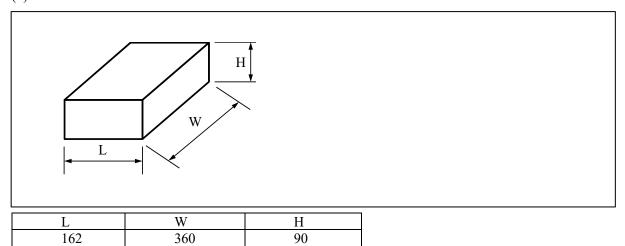
1.3 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping) [C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



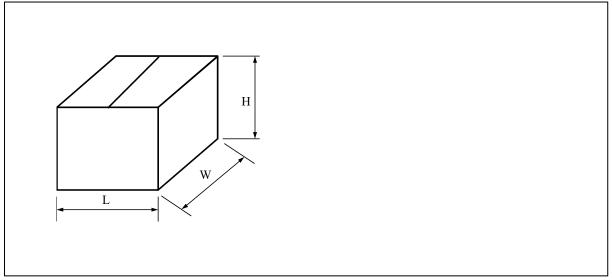
1.4 Dimensions for container

(1) Dimensions for inner box



(Dimensions in mm)

(2) Dimensions for outer box



L	W	Н
410	375	225

(Dimensions in mm)

FUJITSU SEMICONDUCTOR MEMORY SOLUTION LIMITED

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