

# Memory FeRAM

## 256K (32K × 8) Bit SPI

## MB85RS256LYA(AEC-Q100 Compliant)

### ■ DESCRIPTION

MB85RS256LYA is a FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 32,768 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells. This product is specifically targeted for high-temperature environment such as automobile applications.

MB85RS256LYA adopts the Serial Peripheral Interface (SPI).

The MB85RS256LYA is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85RS256LYA can be used for  $10^{13}$  read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E<sup>2</sup>PROM.

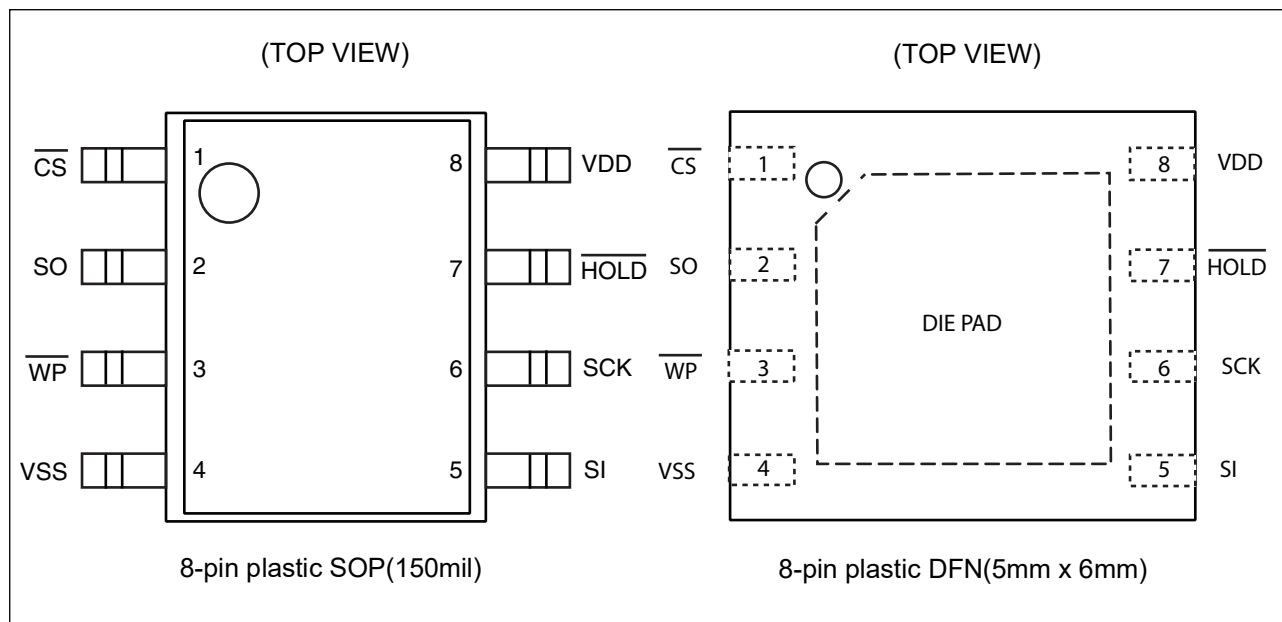
As MB85RS256LYA does not need any waiting time in writing process, the write cycle time of MB85RS256LYA is much shorter than that of Flash memories or E<sup>2</sup>PROM.

### ■ FEATURES

- Bit configuration : 32,768 words × 8 bits
- Special Sector Region : 256 words × 8 bits  
In this region, data storage after (by) three times reflow based on JEDEC MSL-3 standard condition is guaranteed.
- Unique ID
- Serial Number : 64 bits  
In this region, data storage after (by) three times reflow based on JEDEC MSL-3 standard condition is guaranteed.
- Serial Peripheral Interface : SPI (Serial Peripheral Interfaces)  
Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 50 MHz (Max)
- High endurance :  $10^{13}$  times / byte
- Data retention : 70.4 years (+85 °C)  
19.1 years (+105 °C)  
5.9 years (+125 °C) or more  
Under evaluation for more than 5.9 years(+125 °C)
- Operating power supply voltage : 1.7 V to 1.95 V
- Low power consumption : Operating power supply current 3.0mA (Max@50 MHz)  
Standby current 150μA (Max)
- Operation ambient temperature range : - 40 °C to +125 °C
- Package : 8-pin plastic SOP (150mil)  
8-pin plastic DFN (5mm x 6mm)  
RoHS compliant

# MB85RS256LYA(AEC-Q100 Compliant)

## PIN ASSIGNMENT

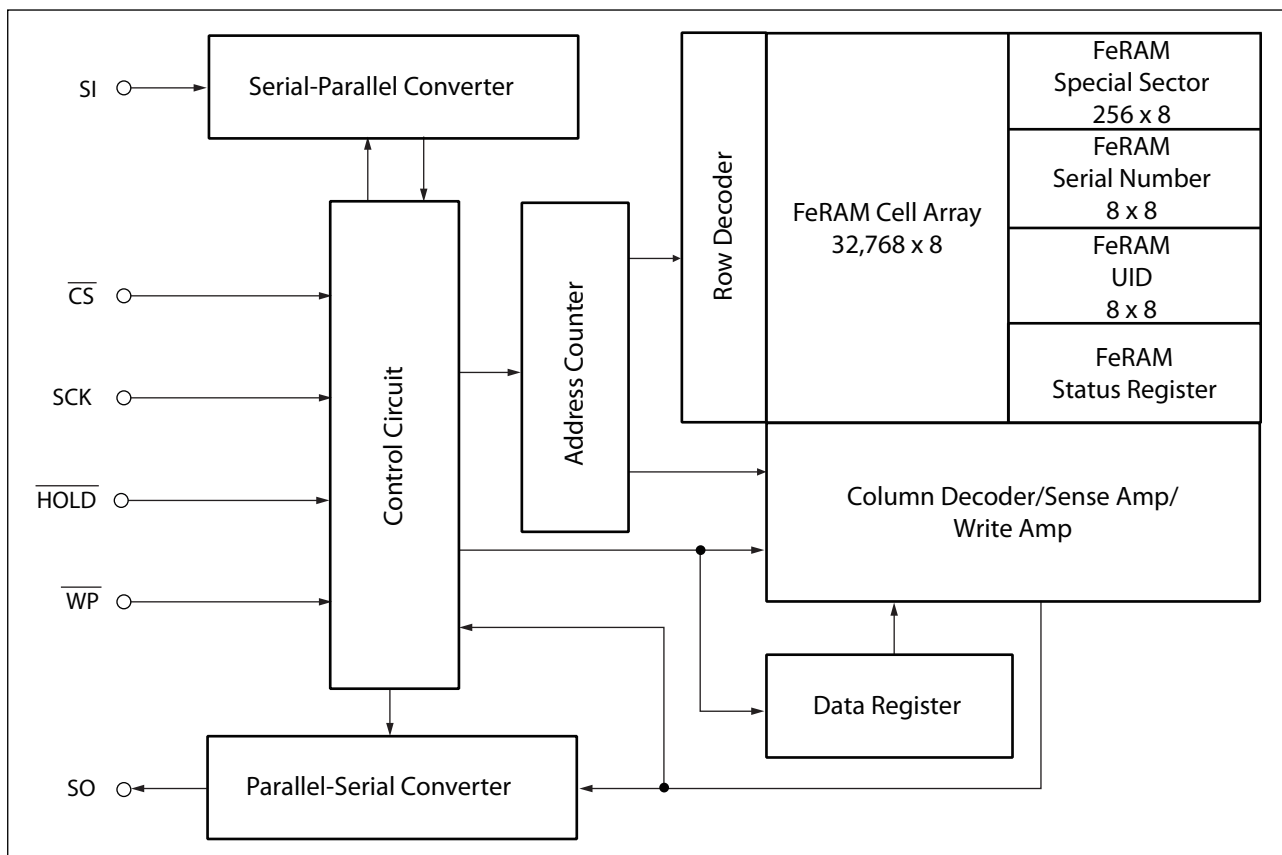


## PIN FUNCTIONAL DESCRIPTIONS

Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is "L" level, device is in select (active) status. $\overline{CS}$ has to be "L" level before inputting op-code.
3	$\overline{WP}$	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with $\overline{WP}$ and WPEN. See "■ WRITING PROTECT" for detail.
7	$\overline{HOLD}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. See "■ HOLD OPERATION" for detail. The Hold pin is pulled up internally to the VDD pin.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FeRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin

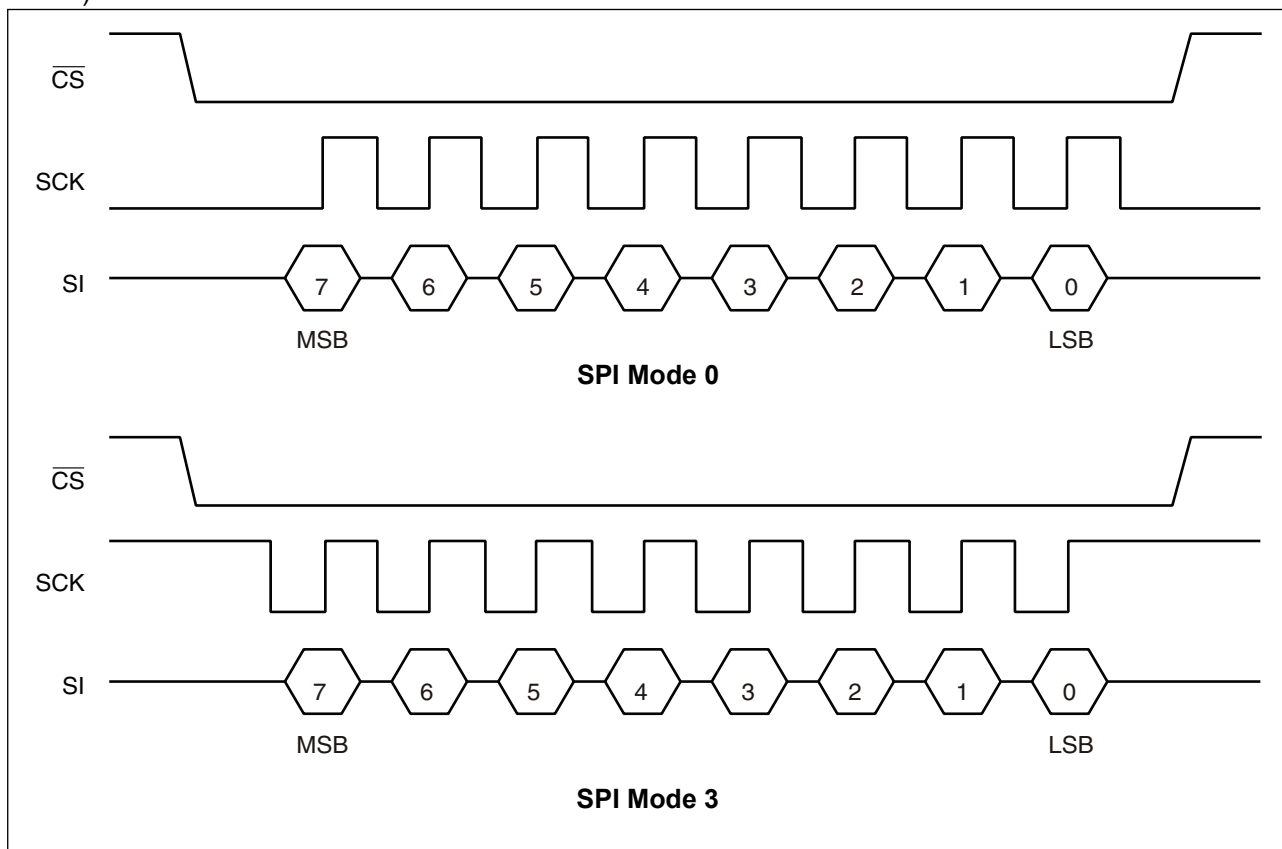
# MB85RS256LYA(AEC-Q100 Compliant)

## ■ BLOCK DIAGRAM



## ■ SPI MODE

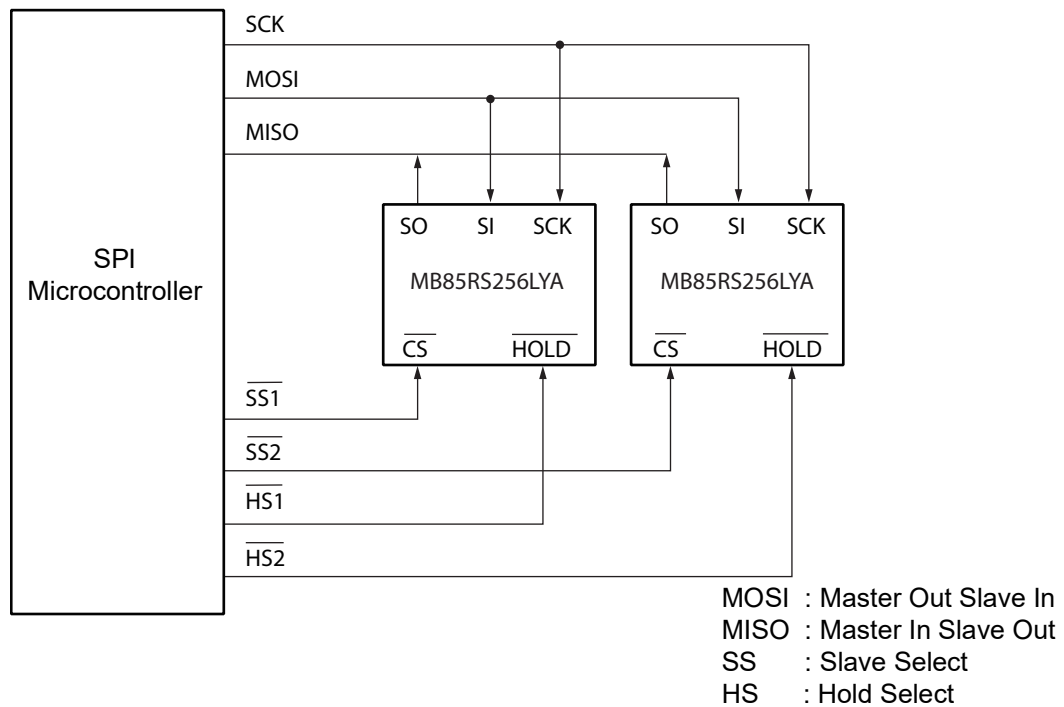
MB85RS256LYA corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0), and SPI mode 3 (CPOL = 1, CPHA = 1).



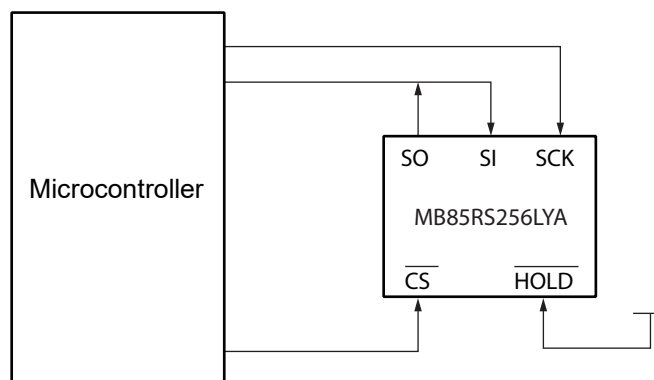
# MB85RS256LYA(AEC-Q100 Compliant)

## ■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS256LYA works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



**System Configuration with SPI Port**



**System Configuration without SPI Port**

# MB85RS256LYA(AEC-Q100 Compliant)

## ■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FeRAM). WPEN protects writing to a status register (refer to “■ WRITING PROTECT”) relating with $\overline{WP}$ input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to “■ BLOCK PROTECT”). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FeRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition. Achieving continuous writing mode, WEL is not reset after following operations making it possible to execute writing commands continuously. After WRSR command recognition. After WRITE command recognition. After WRSN command recognition. After SSWR command recognition.
0	0	This is a bit fixed to “0”.

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## ■ OP-CODE

MB85RS256LYA accepts 14 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If  $\overline{CS}$  is risen while inputting op-code, the command are not performed.

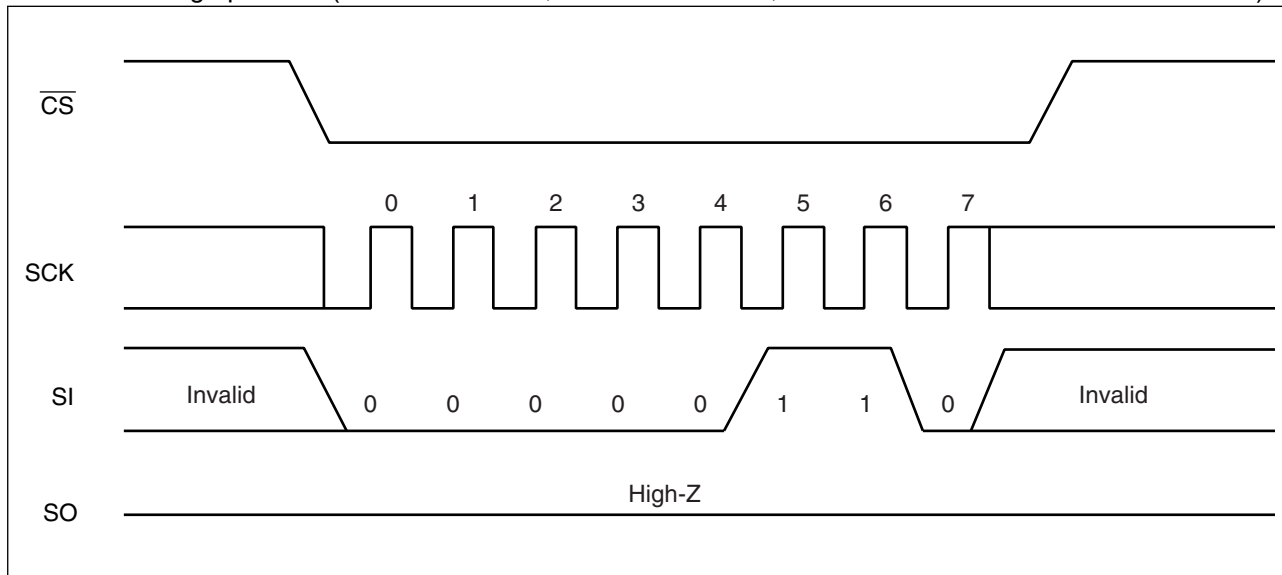
Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110 <sub>B</sub>
WRDI	Reset Write Enable Latch	0000 0100 <sub>B</sub>
RDSR	Read Status Register	0000 0101 <sub>B</sub>
WRSR	Write Status Register	0000 0001 <sub>B</sub>
READ	Read Memory Code	0000 0011 <sub>B</sub>
WRITE	Write Memory Code	0000 0010 <sub>B</sub>
FSTRD	Fast Read Memory Code	0000 1011 <sub>B</sub>
RDID	Read Device ID	1001 1111 <sub>B</sub>
RUID	Read Unique ID	0100 1100 <sub>B</sub>
WRSN	Write Serial Number	1100 0010 <sub>B</sub>
RDSN	Read Serial Number	1100 0011 <sub>B</sub>
SSWR	Write Special Sector	0100 0010 <sub>B</sub>
SSRD	Read Special Sector	0100 1011 <sub>B</sub>
FSSRD	Fast Read Special Sector	0100 1001 <sub>B</sub>
RFU	Reserved	1100 1110 <sub>B</sub>
		1100 1111 <sub>B</sub>
		1100 1100 <sub>B</sub>

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## ■ COMMAND

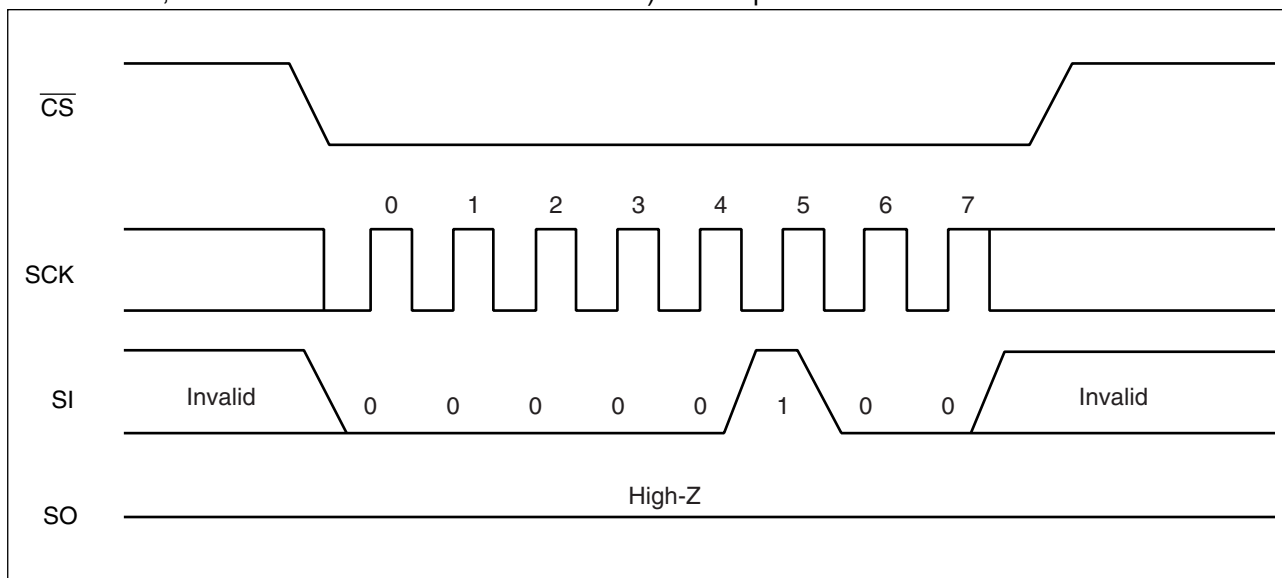
### • WREN

The WREN command sets WEL (Write Enable Latch) bit to 1. WEL has to be set with the WREN command before writing operation (WRSR command, WRITE command, WRSN command and SSWR command) .



### • WRDI

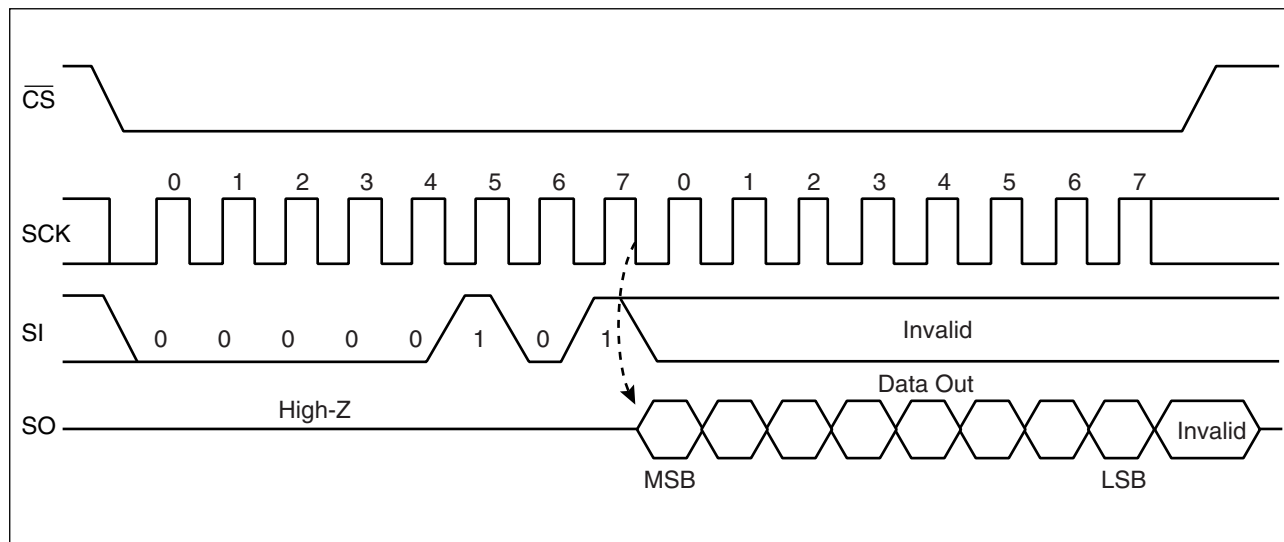
The WRDI command resets WEL (Write Enable Latch) bit to 0. Writing operation (WRSR command, WRITE command, WRSN command and SSWR command) are not performed when WEL is reset.



# MB85RS256LYA(AEC-Q100 Compliant)

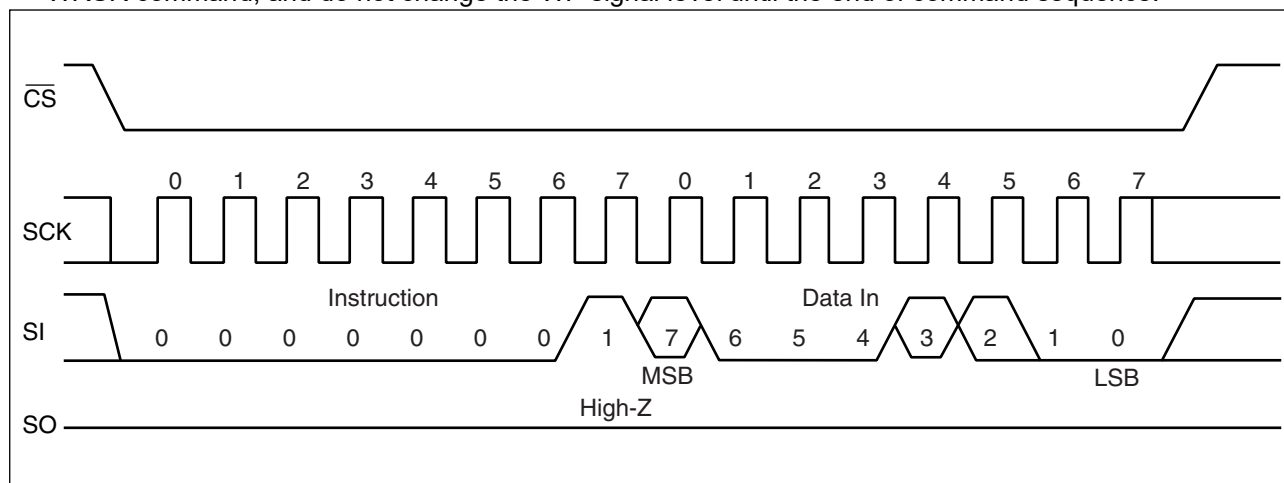
## • RDSR

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of  $\overline{CS}$ .



## • WRSR

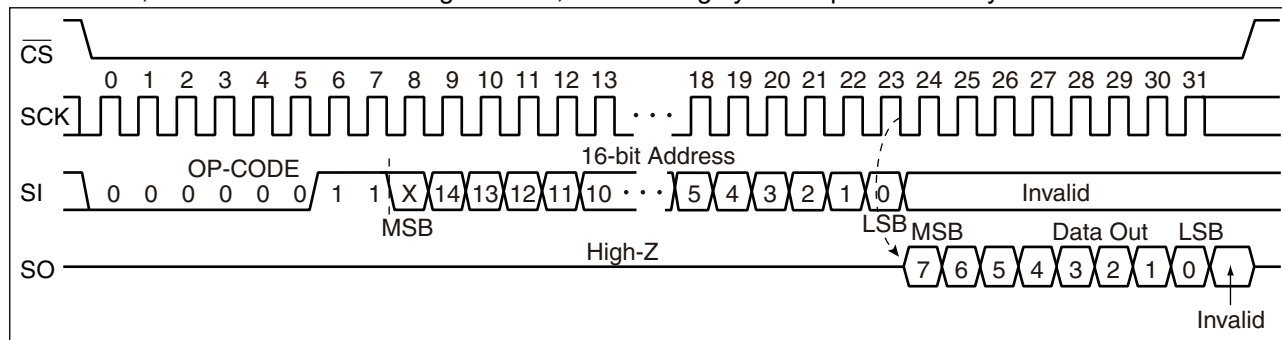
The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored.  $\overline{WP}$  signal level shall be fixed before performing WRSR command, and do not change the  $\overline{WP}$  signal level until the end of command sequence.



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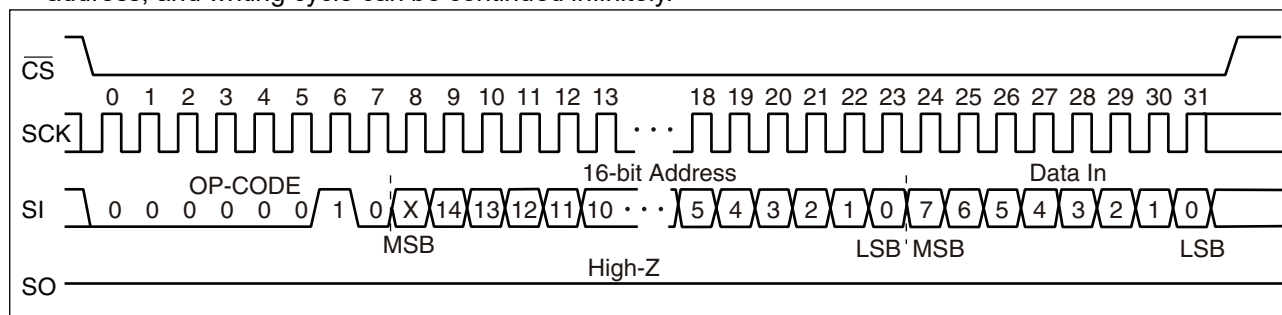
## • READ

The READ command reads FeRAM memory cell array data. Arbitrary 16 bits address and op-code of READ are input to SI. The most significant address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When  $\overline{CS}$  is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before  $\overline{CS}$  rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



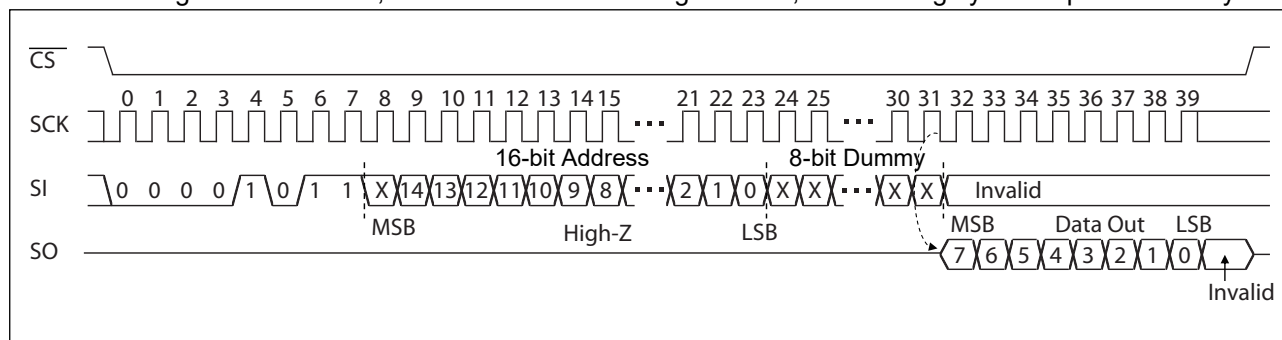
## • WRITE

The WRITE command writes data to FeRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The most significant address bit is invalid. When 8 bits of writing data is input, data is written to FeRAM memory cell array. Risen  $\overline{CS}$  will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before  $\overline{CS}$  rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely.



## • FSTRD

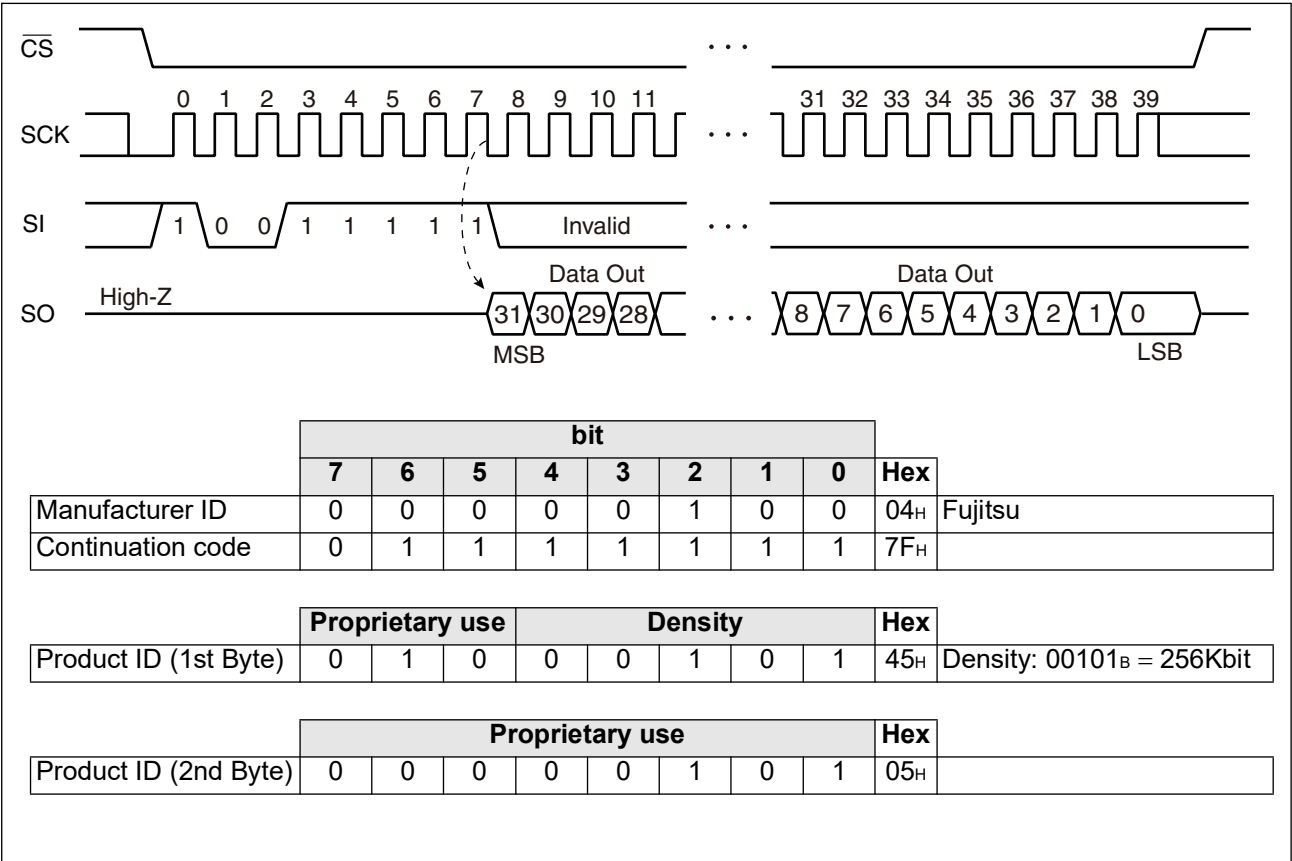
The FSTRD command reads FeRAM memory cell array data. Arbitrary 16bits address and op-code of FSTRD are input to SI followed by 8 bits dummy. The 1-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When  $\overline{CS}$  is risen, the FSTRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before  $\overline{CS}$  rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



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## • RDID

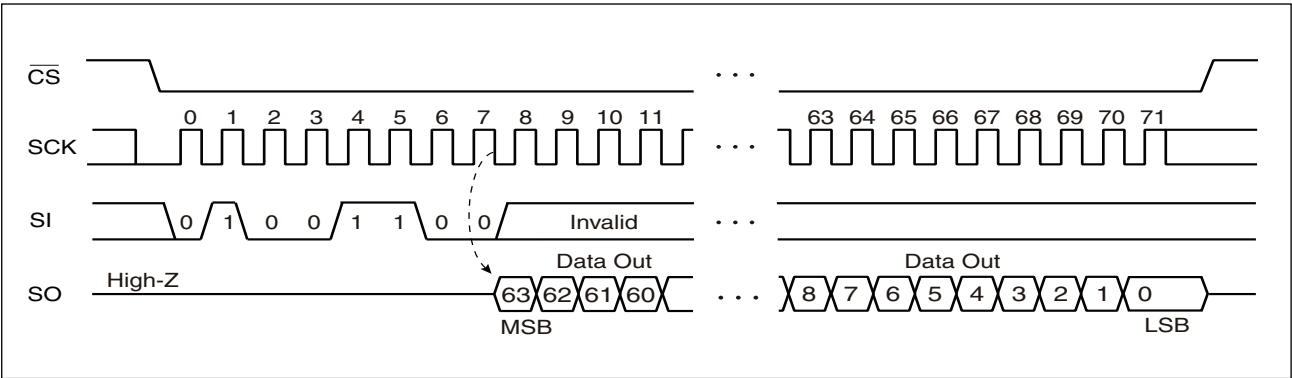
The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, 32-bit Device ID is output by continuously sending SCK clock, and SO holds the output state of the last bit until CS is risen.



## • RUID

The RUID command reads an unique ID which is defined in 64bits for each device. After performing RUID op-code to SI, 64-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK.

The unique ID is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.

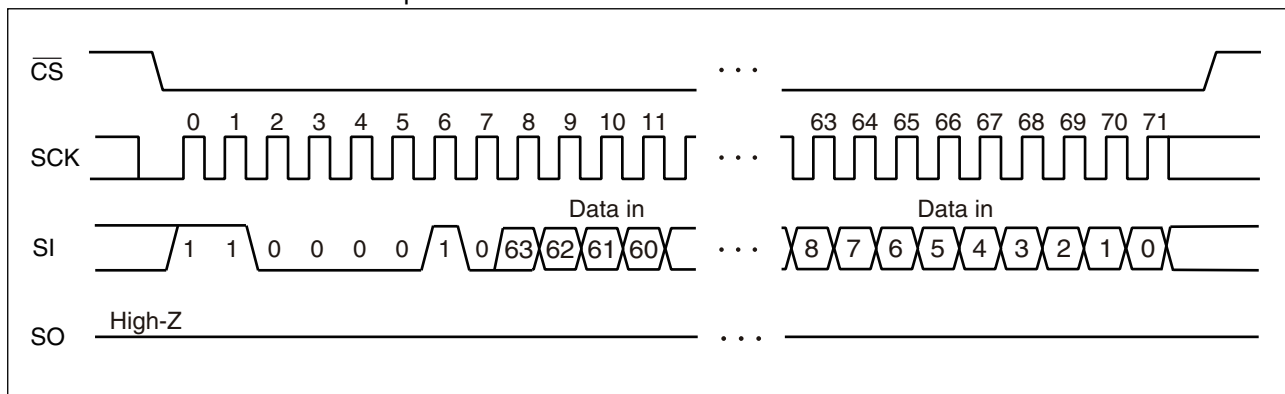


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## •WRSN

The WRSN command writes data to serial number region which is allowed to write only one time. After performing WRSN op-code to SI, 64bits of writing data is input. Once wrote, the serial number region is protected, disabling to overwrite even when issuing WRSN command.

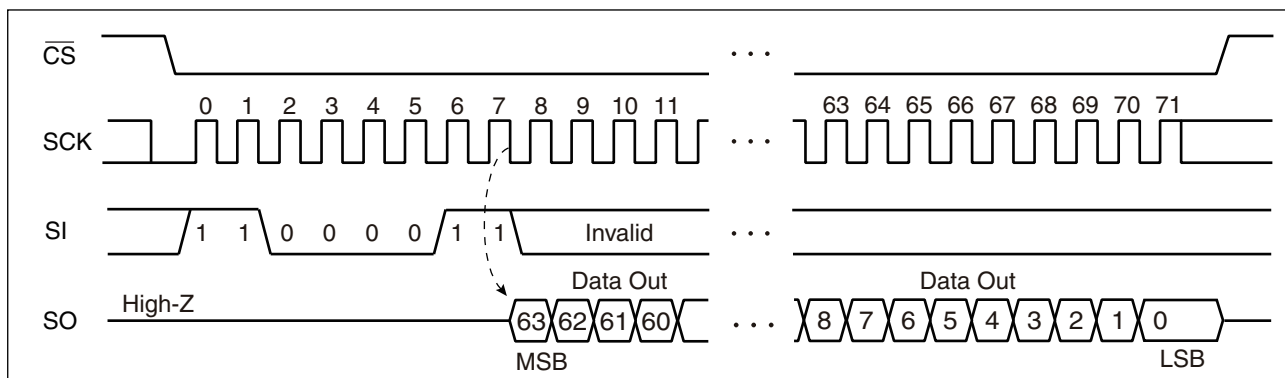
$\overline{WP}$  signal level shall be fixed before performing WRSN command, and do not change the  $\overline{WP}$  signal level until the end of command sequence.



## •RDSN

The RDSN command reads 64 bits of serial number which is written using WRSN command. After performing RDSN op-code to SI, 64-cycle clock to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. When reading serial number from devices which no WRSN command is executed, "0" for all bits are output.

The serial number is stable between before and after reflow. Refer "■ REFLOW CONDITIONS AND FLOOR LIFE" for the reflow condition.

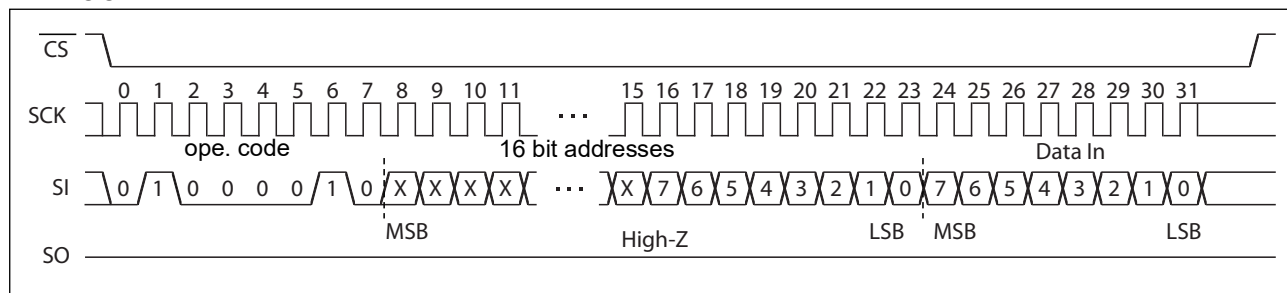


# MB85RS256LYA(AEC-Q100 Compliant)

## • SSWR

The SSWR command writes data to special sector (a special region of 256 Byte in FeRAM). SSWR op-code, arbitrary 16 bits address and 8-bit writing data are input to SI. The 8-bit upper address is invalid. When input of 8-bit writing data is completed, it starts writing data to special sector. Risen  $\overline{CS}$  will terminate the SSWR command, but if you continue the writing data for each before  $\overline{CS}$  rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, roll over is not happen, the data hereafter is ignored.

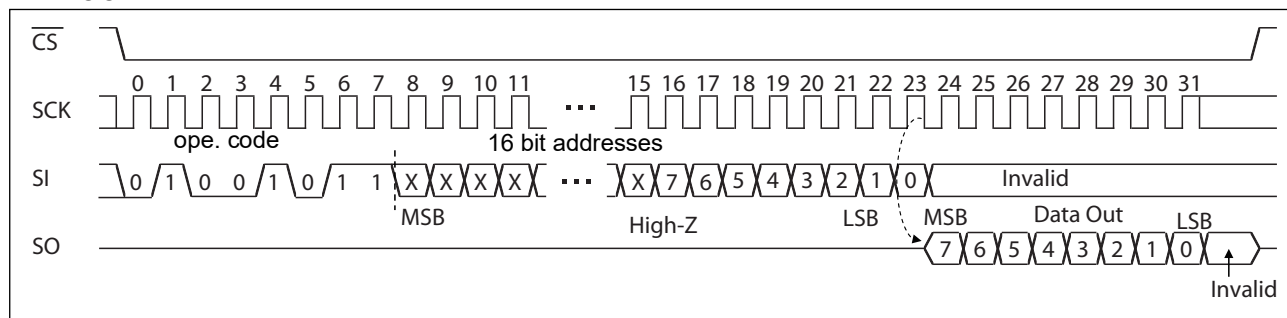
The data in special sector is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.



## • SSRD

The SSRD command reads data from special sector (a special region of 256 Byte in FeRAM). SSWR op-code and arbitrary 16 bits address are input to SI. The 8-bit upper address is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When  $\overline{CS}$  is risen, the SSRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before  $\overline{CS}$  rising. When it reaches the most significant address, roll over is not happen.

The data in special sector is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.

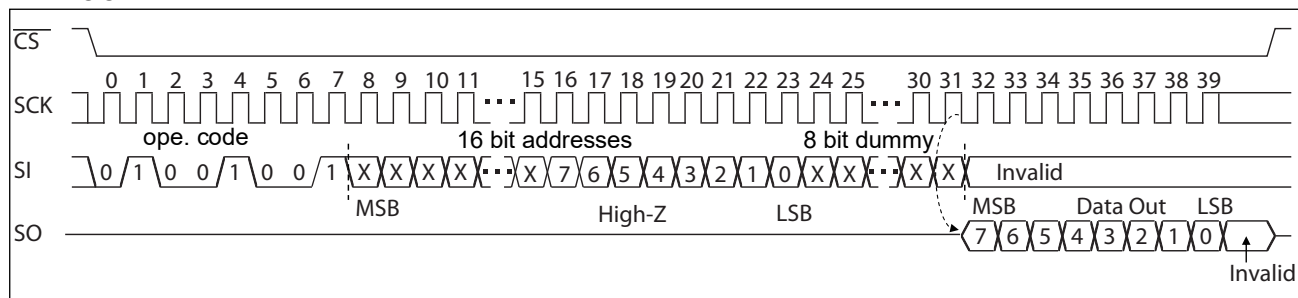


# MB85RS256LYA(AEC-Q100 Compliant)

## • FSSRD

The SSRD command reads data from special sector (a special region of 256 Byte in FeRAM). SSRD op-code and arbitrary 16 bits address are input to SI followed by 8 bits dummy. The 8-bit upper address is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When  $\overline{CS}$  is risen, the SSRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before  $\overline{CS}$  rising. When it reaches the most significant address, roll over is not happen.

The data in special sector is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.



## ■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	6000 <sub>H</sub> to 7FFF <sub>H</sub> (upper 1/4)
1	0	4000 <sub>H</sub> to 7FFF <sub>H</sub> (upper 1/2)
1	1	0000 <sub>H</sub> to 7FFF <sub>H</sub> (all)

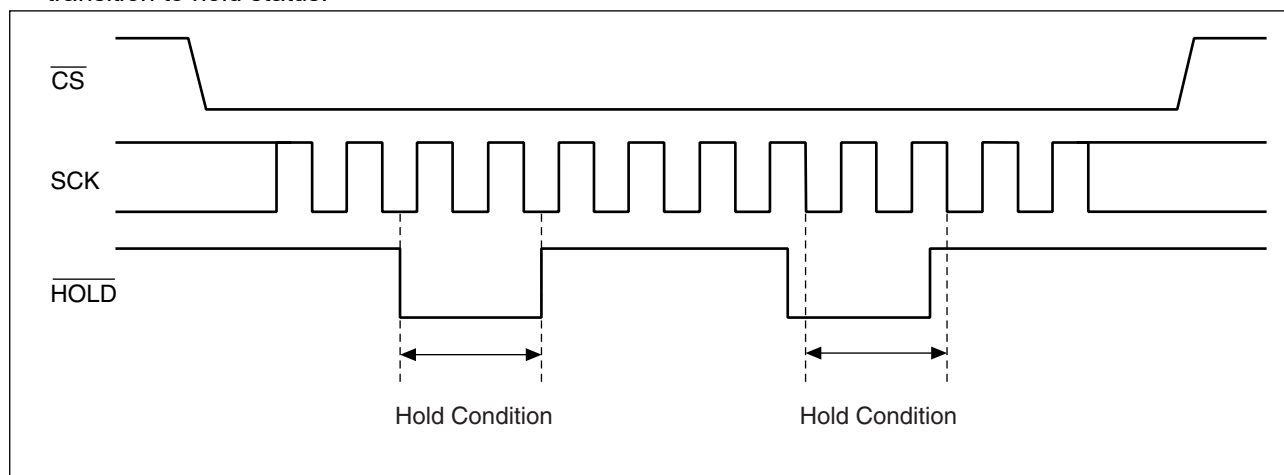
## ■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, WP as shown in the table.

WEL	WPEN	WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

## ■ HOLD OPERATION

Hold status is retained without aborting a command if  $\overline{\text{HOLD}}$  is "L" level while  $\overline{\text{CS}}$  is "L" level. The timing for starting and ending hold status depends on the SCK to be "H" level or "L" level when a  $\overline{\text{HOLD}}$  pin input is transitioned to the hold condition as shown in the diagram below. In case the  $\overline{\text{HOLD}}$  pin transitioned to "L" level when  $\overline{\text{SCK}}$  is "L" level, return the  $\overline{\text{HOLD}}$  pin to "H" level at  $\overline{\text{SCK}}$  being "L" level. In the same manner, in case the  $\overline{\text{HOLD}}$  pin transitioned to "L" level when  $\overline{\text{SCK}}$  is "H" level, return the  $\overline{\text{HOLD}}$  pin to "H" level at  $\overline{\text{SCK}}$  being "H" level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If  $\overline{\text{CS}}$  is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



# MB85RS256LYA(AEC-Q100 Compliant)

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	$V_{DD}$	- 0.5	+ 2.5	V
Input voltage*	$V_{IN}$	- 0.5	$V_{DD} + 0.5$	V
Output voltage*	$V_{OUT}$	- 0.5	$V_{DD} + 0.5$	V
Operation ambient temperature	$T_A$	- 40	+ 125	°C
Storage temperature	$T_{stg}$	- 55	+ 150	°C

\*: These parameters are based on the condition that  $V_{SS}$  is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	$V_{DD}$	1.70	1.80	1.95	V
Operation ambient temperature*2	$T_A$	- 40	—	+ 125	°C

\*1: These parameters are based on the condition that  $V_{SS}$  is 0 V.

\*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

# MB85RS256LYA(AEC-Q100 Compliant)

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ (T <sub>A</sub> =25 °C)	Max	
Input leakage current*1	I <sub>LI</sub>	$\overline{CS} = V_{DD}$	25 °C	—	—	1	μA
			125 °C	—	—	2	
		$\overline{WP}, \overline{SCK}, \overline{CS}$ SI = 0 V to V <sub>DD</sub>	25 °C	—	—	1	
			125 °C	—	—	2	
		HOLD = 0 V to V <sub>DD</sub>	25 °C	—	—	100	
			125 °C	—	—	100	
Output leakage current*2	I <sub>LO</sub>	SO = 0 V to V <sub>DD</sub>	25 °C	—	—	1	μA
			125 °C	—	—	2	
Operating power supply current*3	I <sub>DD</sub>	SCK = 50MHz	—	—	2.38	3.0	mA
Standby current	I <sub>SB</sub>	SCK = SI = $\overline{CS}$ = $\overline{WP} = V_{DD}$	—	—	5.0	150	μA
Input high voltage	V <sub>IH</sub>	V <sub>DD</sub> = 1.7 V to 1.95 V	V <sub>DD</sub> × 0.8	—	—	V <sub>DD</sub> + 0.5	V
Input low voltage	V <sub>IL</sub>	V <sub>DD</sub> = 1.7 V to 1.95 V	− 0.5	—	—	V <sub>DD</sub> × 0.2	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = − 2 mA	V <sub>DD</sub> − 0.5	—	—	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2 mA	—	—	—	0.4	V
Pull up resistance for HOLD	R <sub>P</sub>	—	36	66	230	—	kΩ

\*1 : Applicable pin :  $\overline{CS}$ ,  $\overline{WP}$ , SCK, SI

\*2 : Applicable pin : SO

\*3 : Input voltage magnitude : V<sub>DD</sub> − 0.2 V or V<sub>SS</sub>

# MB85RS256LYA(AEC-Q100 Compliant)

## 2. AC Characteristics

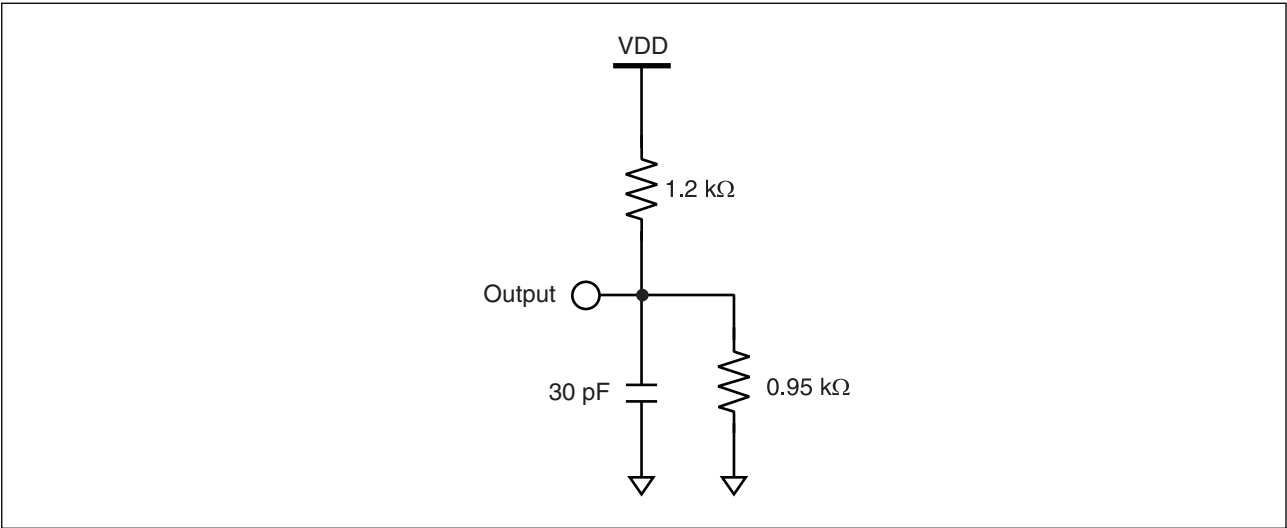
Parameter	Symbol	Value		Unit	Condition $V_{DD}$
		Min	Max		
SCK clock frequency	$f_{CK}$	—	50	MHz	all commands except for READ/SSRD
		—	40		READ command
		—	10		SSRD command
Clock high time	$t_{CH}$	9	—	ns	
Clock low time	$t_{CL}$	9	—	ns	
Chip select set up time	$t_{CSU}$	5	—	ns	
Chip select hold time	$t_{CSH}$	5	—	ns	
Output disable time	$t_{OD}$	—	10	ns	
Output data valid time	$t_{ODV}$	—	9	ns	*1
Output hold time	$t_{OH}$	0	—	ns	
Deselect time	$t_D$	40	—	ns	
Data in rising time	$t_R$	—	50	ns	
Data falling time	$t_F$	—	50	ns	
Data set up time	$t_{SU}$	5	—	ns	
Data hold time	$t_H$	5	—	ns	
HOLD set uptime	$t_{HS}$	10	—	ns	—
HOLD hold time	$t_{HH}$	10	—	ns	—
HOLD output floating time	$t_{HZ}$	—	20	ns	—
HOLD output active time	$t_{LZ}$	—	20	ns	—

\*1: In SSRD command, 60ns(max.)

### AC Test Condition

Power supply voltage	: 1.7 V to 1.95 V Operation
Operation ambient temperature	: -40 °C to +125 °C
Input voltage magnitude	: $V_{DD} \times 0.8 \leq V_{IH} \leq V_{DD}$ $0 \leq V_{IL} \leq V_{DD} \times 0.2$
Input rising time	: 5 ns
Input falling time	: 5 ns
Input judge level	: $V_{DD}/2$
Output judge level	: $V_{DD}/2$

AC Load Equivalent Circuit



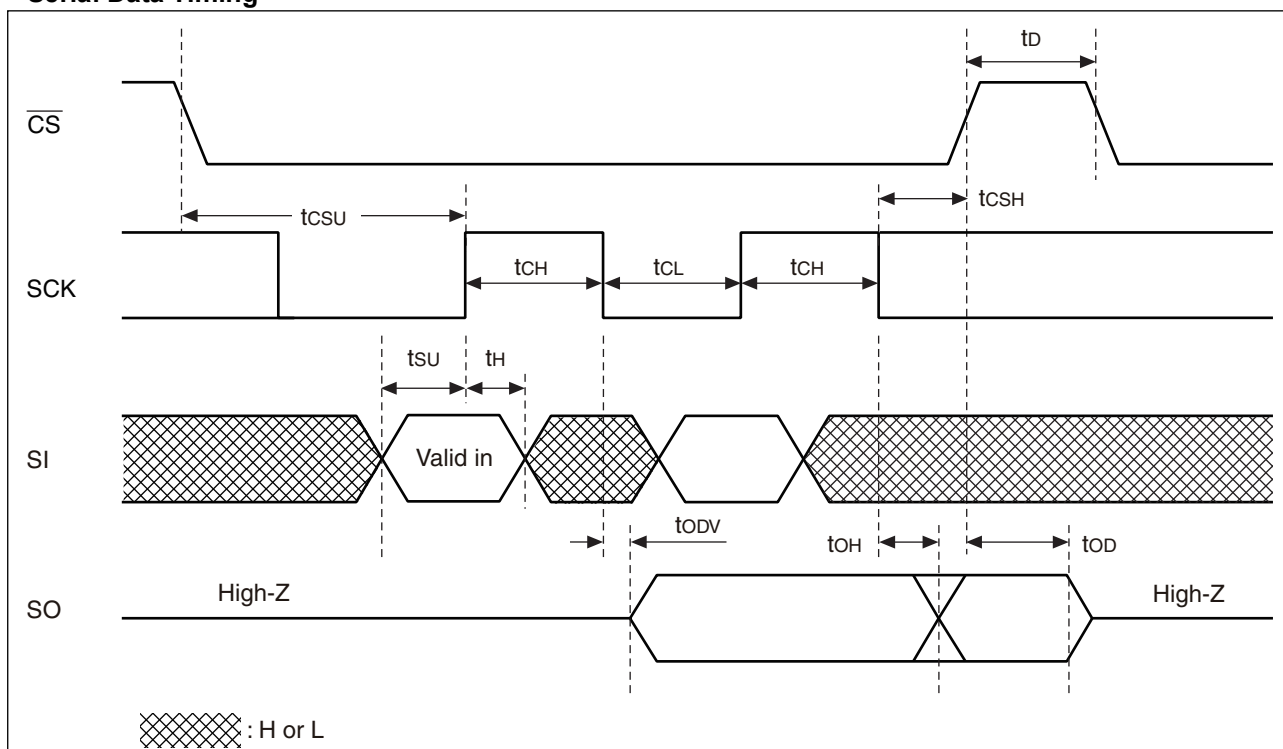
3. Pin Capacitance

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output capacitance	$C_O$	$V_{DD} = 1.8 \text{ V},$ $V_{IN} = V_{OUT} = 0 \text{ V to } V_{DD},$ $f = 1 \text{ MHz}, T_A = +25 \text{ }^\circ\text{C}$	—	8	pF
Input capacitance	$C_I$		—	6	pF

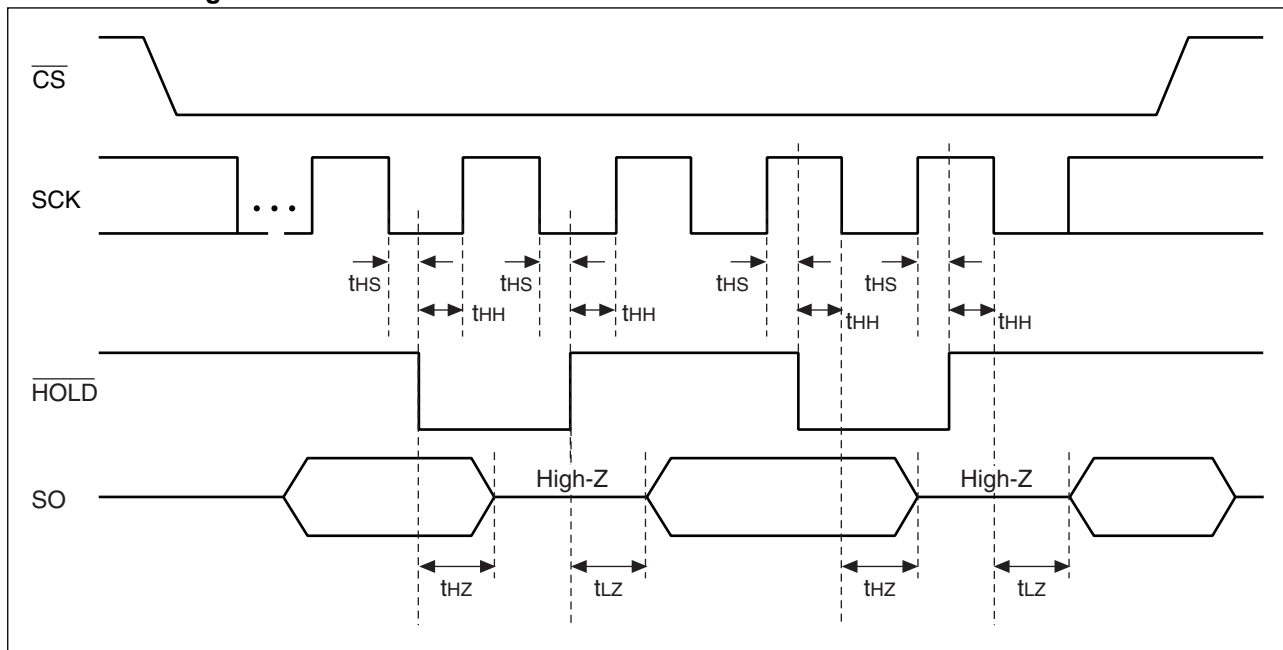
# MB85RS256LYA(AEC-Q100 Compliant)

## ■ TIMING DIAGRAM

### • Serial Data Timing

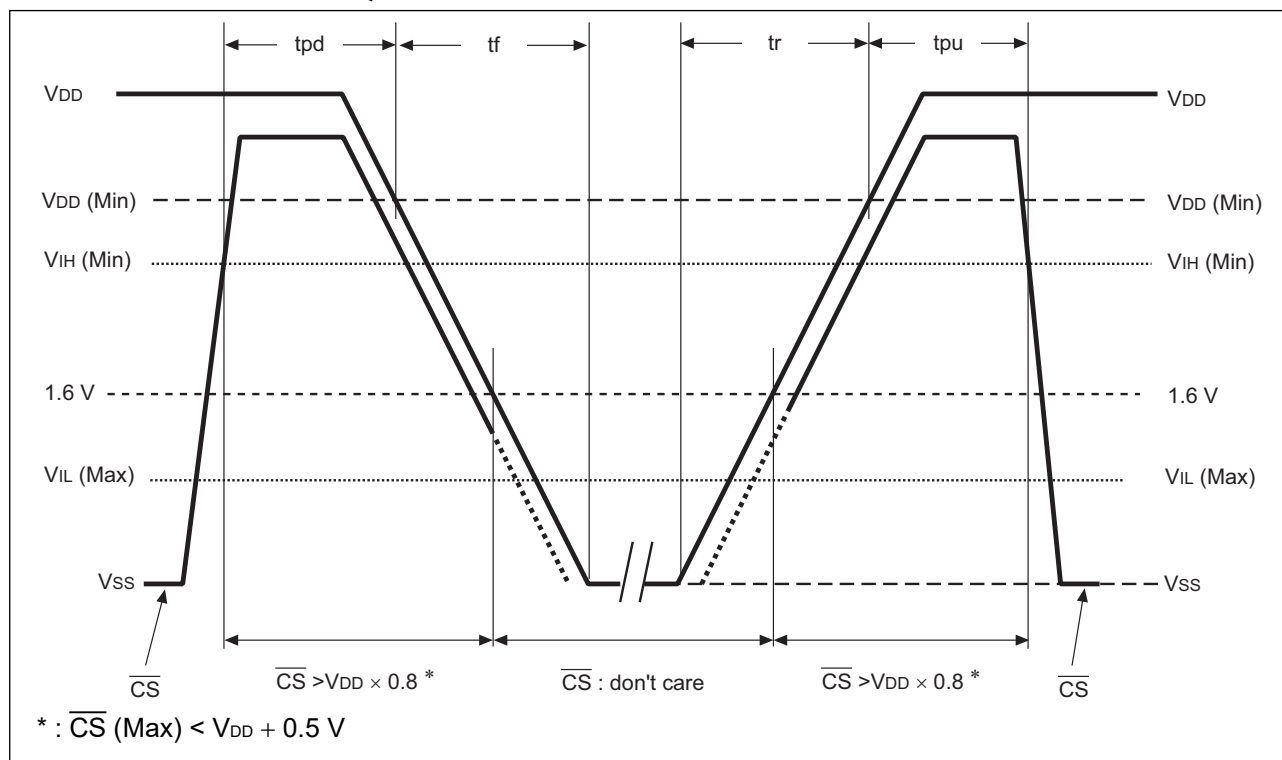


### • Hold Timing



# MB85RS256LYA(AEC-Q100 Compliant)

## ■ POWER ON/OFF SEQUENCE



In case relative short  $V_{DD}$  pulse whose peak level is beyond 1.6 is applied, please set  $V_{DD}$  falling time,  $t_f$ , longer than 0.4ms/V. (When  $V_{DD}$  rises beyond 1.6V, and falls just after, if this term is very short the device may loose its function.).

Parameter	Symbol	Value		Unit
		Min	Max	
$\overline{CS}$ level hold time at power OFF	tpd	400	—	ns
$\overline{CS}$ level hold time at power ON	tpu	450	—	μs
Power supply rising time	tr	0.05	—	ms/V
Power supply falling time	tf	0.1	—	ms/V

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

# MB85RS256LYA(AEC-Q100 Compliant)

## ■ FeRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Read/Write Endurance*1	10 <sup>13</sup>	—	Times/byte	Operation Ambient Temperature T <sub>A</sub> = + 125 °C
Data Retention*2	5.9 or more*3	—	Years	Operation Ambient Temperature T <sub>A</sub> = + 125 °C
	19.1	—		Operation Ambient Temperature T <sub>A</sub> = + 105 °C
	70.4	—		Operation Ambient Temperature T <sub>A</sub> = + 85 °C

\*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

\*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

\*3: Under evaluation for more than 5.9 years(+125 °C).

## ■ NOTE ON USE

We recommend programming of the device after reflow except for special sector region and serial number region. Data written before reflow cannot be guaranteed.

## ■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RS256LYAPNF-GS-BCE1 MB85RS256LYAPNF-GSBCERE1 MB85RS256LYAPN-GS-AWE1 MB85RS256LYAPN-GS-AWEWE1	≥  2000 V
ESD CDM (Charged Device Model) AEC-Q100-011(FI-CDM) compliant		≥  1000 V
Latch-Up (I-test) JESD78 compliant		≥  125mA
Latch-Up (V <sub>supply</sub> overvoltage test) JESD78 compliant		≥ 5.4V

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

## ■ Current status on Contained Restricted Substances

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

## MB85RS256LYA(AEC-Q100 Compliant)

### ■ ORDERING INFORMATION :

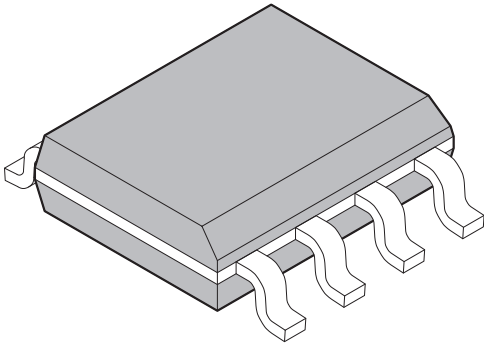
Part number	Package	Shipping form	Minimum shipping quantity
MB85RS256LYAPNF-GS-BCE1	8-pin plastic SOP	Tube	— *
MB85RS256LYAPNF-GSBCERE1	8-pin plastic SOP	Embossed Carrier tape	1500
MB85RS256LYAPN-GS-AWE1	8-pin plastic DFN	Tray	— *
MB85RS256LYAPN-GS-AWEWE1	8-pin plastic DFN	Embossed Carrier tape	1500

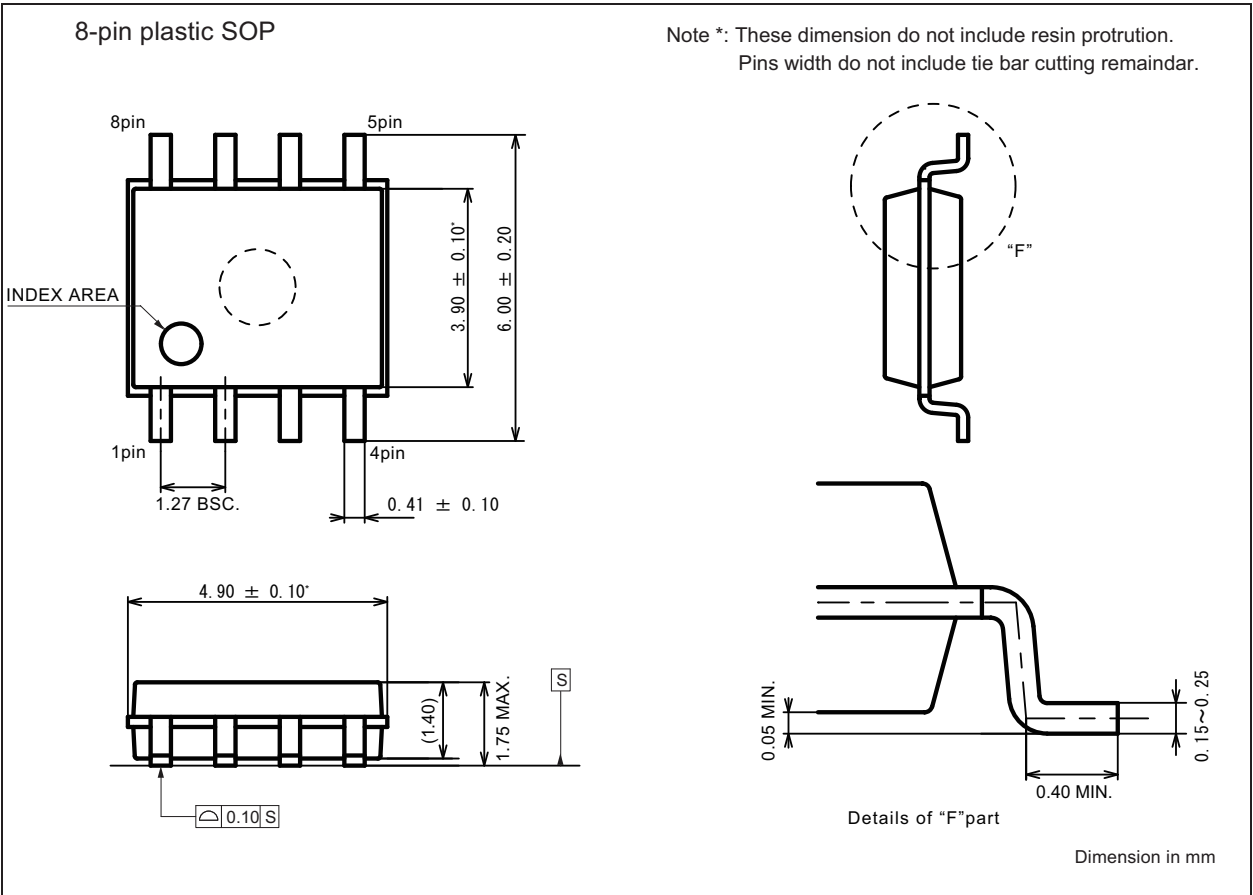
\* : Please contact our sales office about minimum shipping quantity.

# MB85RS256LYA(AEC-Q100 Compliant)

## ■ PACKAGE DIMENSION

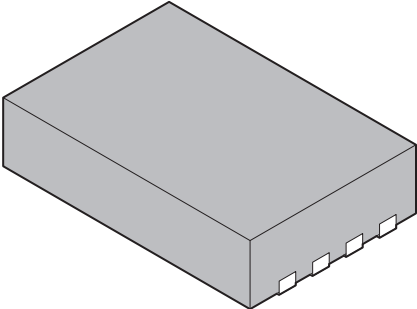
(1) MB85RS256LYAPNF-GS-BCE1/MB85RS256LYAPNF-GSBCERE1

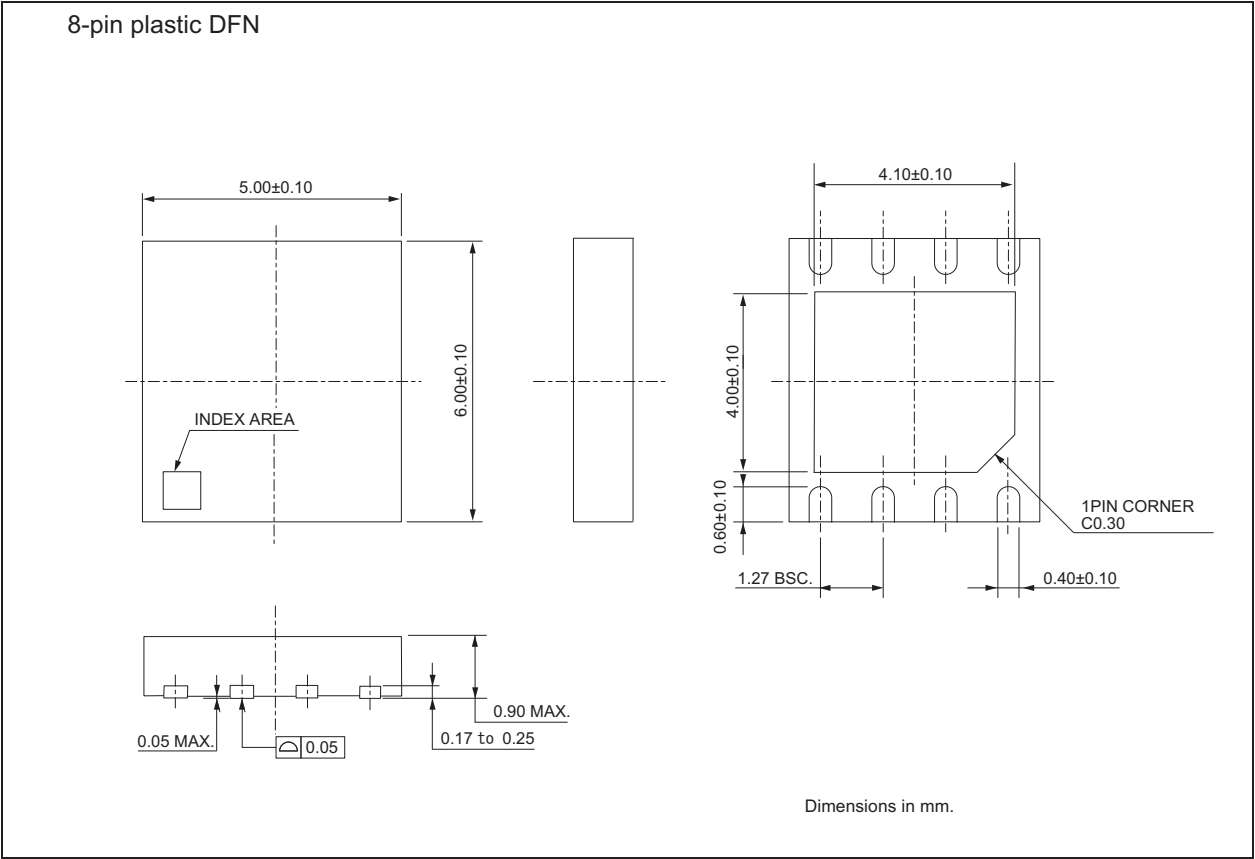
<div>8-pin plastic SOP</div>  <div>MB85RS256LYAPNF-GS-BCE1 MB85RS256LYAPNF-GSBCERE1</div>	Lead pitch	1.27mm
	Package width x Package length	3.90mm x 4.90mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75mm MAX.



# MB85RS256LYA(AEC-Q100 Compliant)

## (2) MB85RS256LYAPN-GS-AWE1/MB85RS256LYAPN-GS-AWEWE1

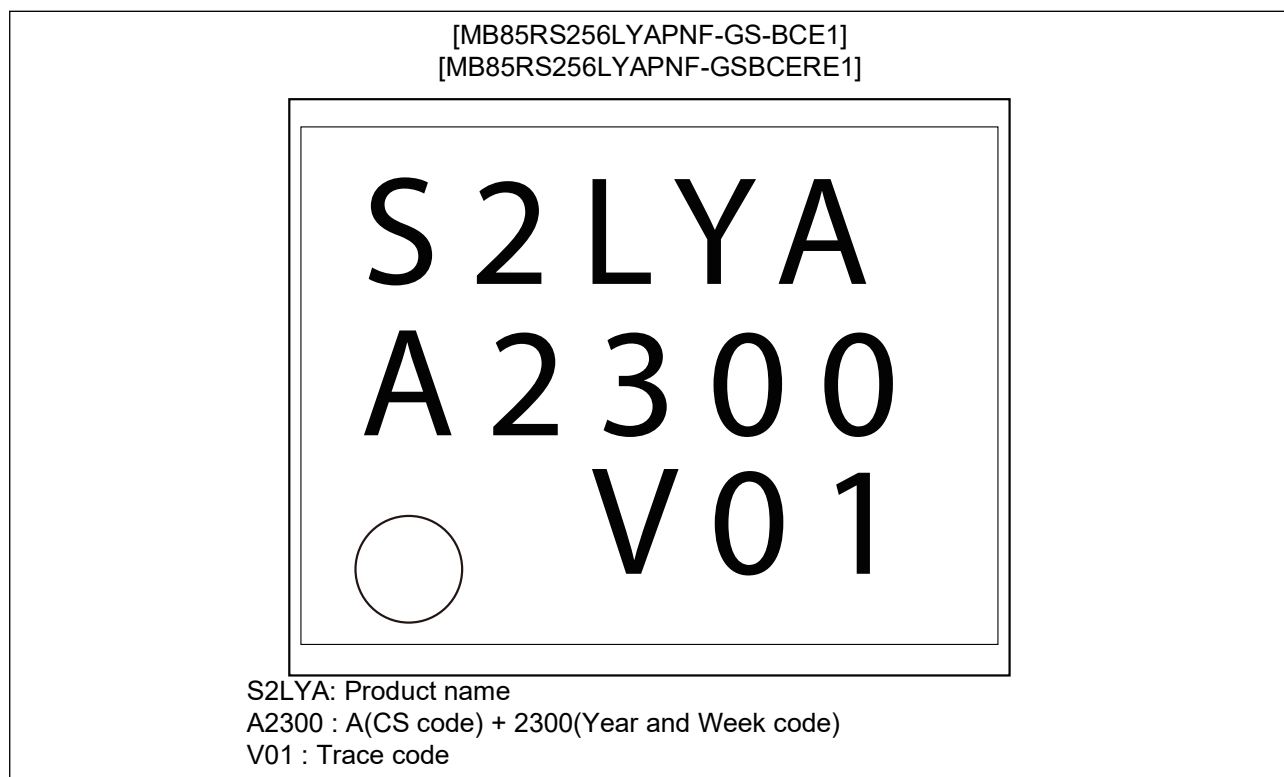
<p>8-pin plastic DFN</p>  <p>MB85RS256LYAPN-GS-AWE1 MB85RS256LYAPN-GS-AWEWE1</p>	Lead pitch	1.27 mm
	Package width x Package length	5.00 mm × 6.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX



# MB85RS256LYA(AEC-Q100 Compliant)

## ■ MARKING (Example)

(1) MB85RS256LYAPNF-GS-BCE1/MB85RS256LYAPNF-GSBCERE1



(2) MB85RS256LYAPN-GS-AWE1/MB85RS256LYAPN-GS-AWEWE1



# MB85RS256LYA(AEC-Q100 Compliant)

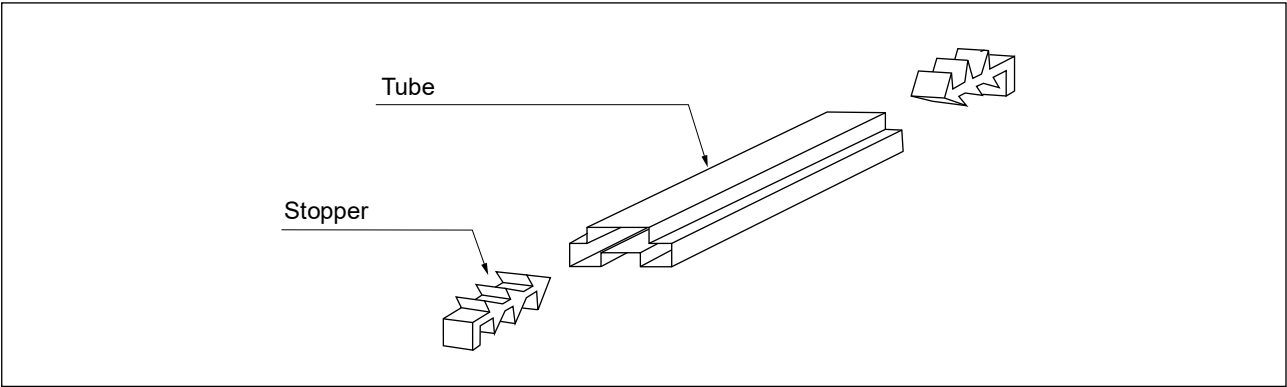
## ■ PACKING INFORMATION

(1) MB85RS256LYAPNF-GS-BCE1/MB85RS256LYAPNF-GSBCERE1

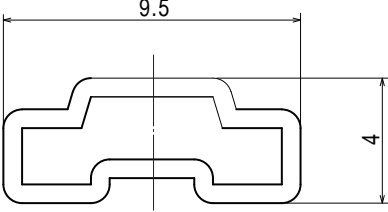
### 1. Tube (MB85RS256LYAPNF-GS-BCE1)

#### 1.1 Tube Dimensions

- Tube/stopper shape (example)



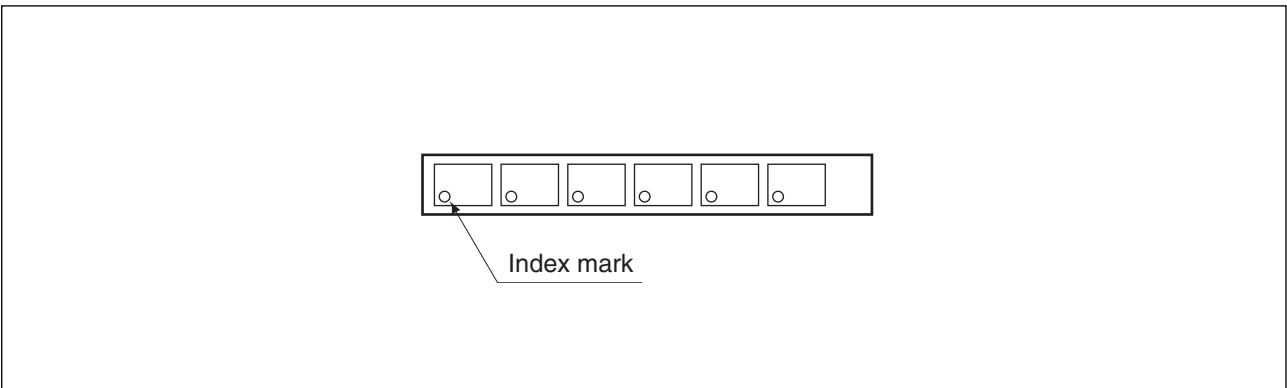
- Tube cross-sections and Maximum quantity

	Maximum quantity		
	pcs/tube(500mm)	pcs/inner box	pcs/outer box
	85	4,250	17,000

No heat resistance.  
Package should not be baked by using tube.

(Dimensions in mm)

- Direction of index in tube



# MB85RS256LYA(AEC-Q100 Compliant)

## 1.2 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss tapping)  
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

XXXXXXXXXXXXXX (Part number)

(3N)1 XXXXXXXXXXXXXXXX XXX (LEAD FREE mark)

XXX (Part number and quantity)

QC PASS

(3N)2 XXXXXXXXXXXXXXXX XXXXXX

XXX pcs (Quantity)

XXXXXXXXXXXXXXXXXX (Part number)

XXXXXXXXXXXXXXXXXX (Part number bar code)

XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx

XXXXXXXXXXXXXX (Part number)

XX/XX (Package count)

XXXX-XXX XXX

XXXXXXXXXXXXX (Control number ) XXXX-XXX XXX

XXXXXXXXXXXXXXXXXX (Lot Number and quantity)

XXXXXXXXXXXXXXXXXX (Comment)

← C-3 Label

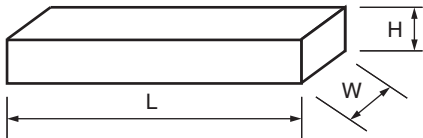
← Perforated line

← Supplemental Label

# MB85RS256LYA(AEC-Q100 Compliant)

## 1.3 Dimensions for Containers

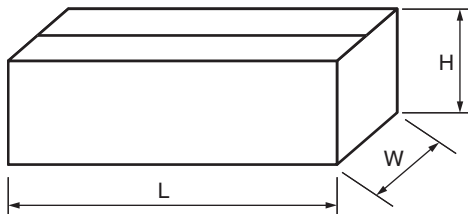
### (1) Dimensions for inner box



L	W	H
540	125	75

(Dimensions in mm)

### (2) Dimensions for outer box



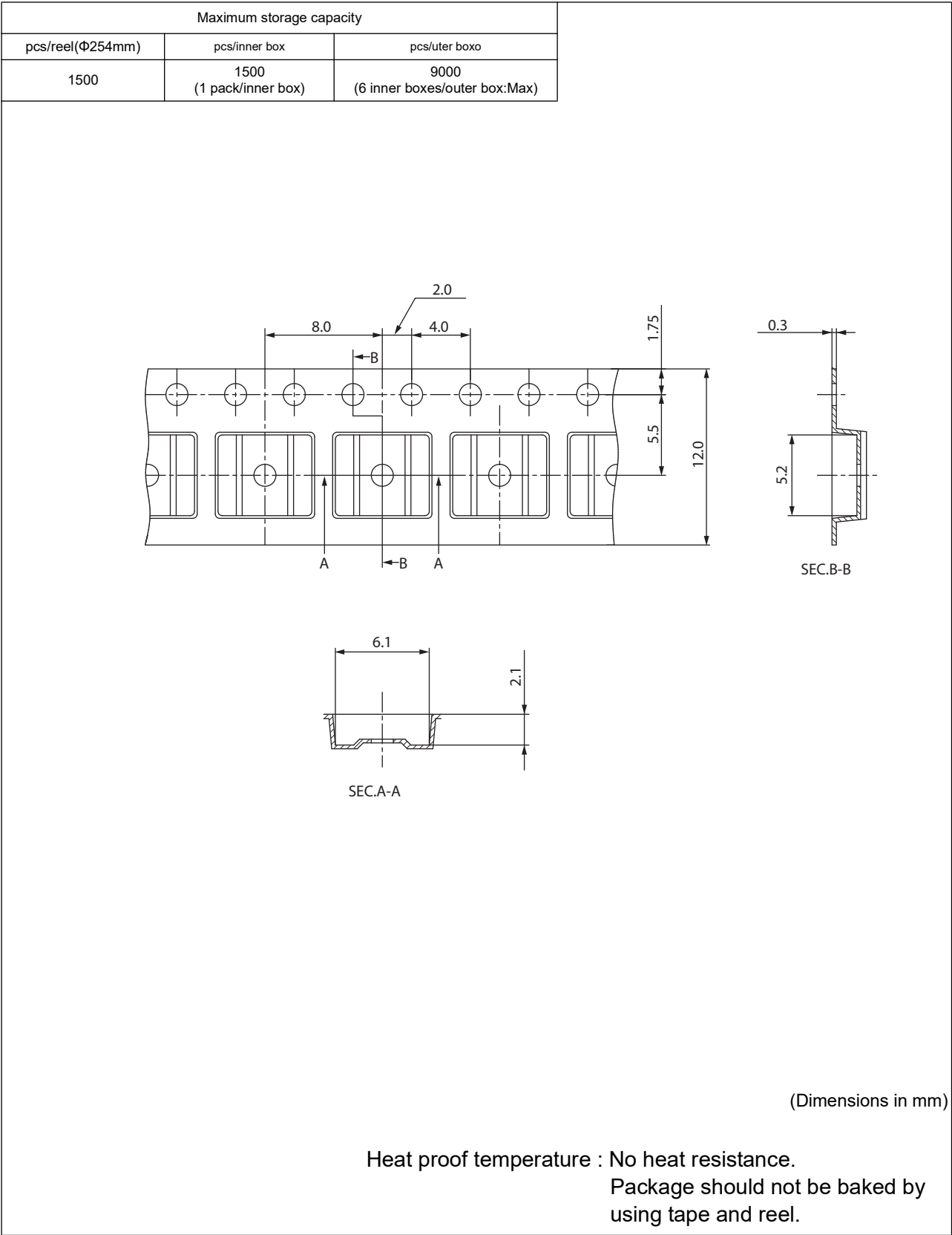
L	W	H
565	270	180

(Dimensions in mm)

# MB85RS256LYA(AEC-Q100 Compliant)

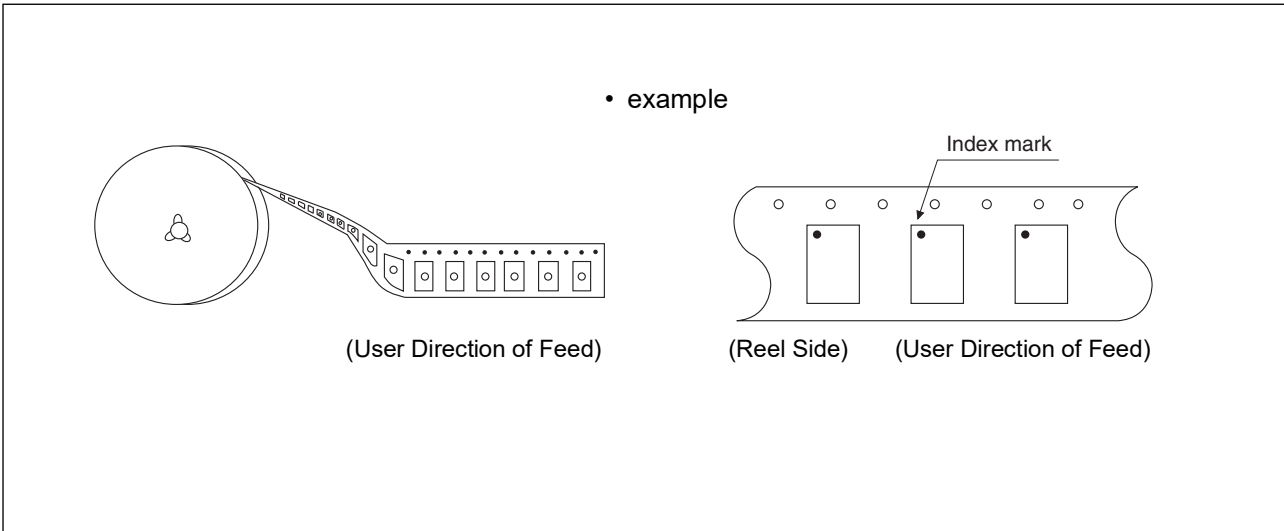
## 2. Emboss Tape (MB85RS256LYAPNF-GSBCERE1)

### 2.1 Tape Dimensions (not drawn to scale) (8-pin plastic SOP)

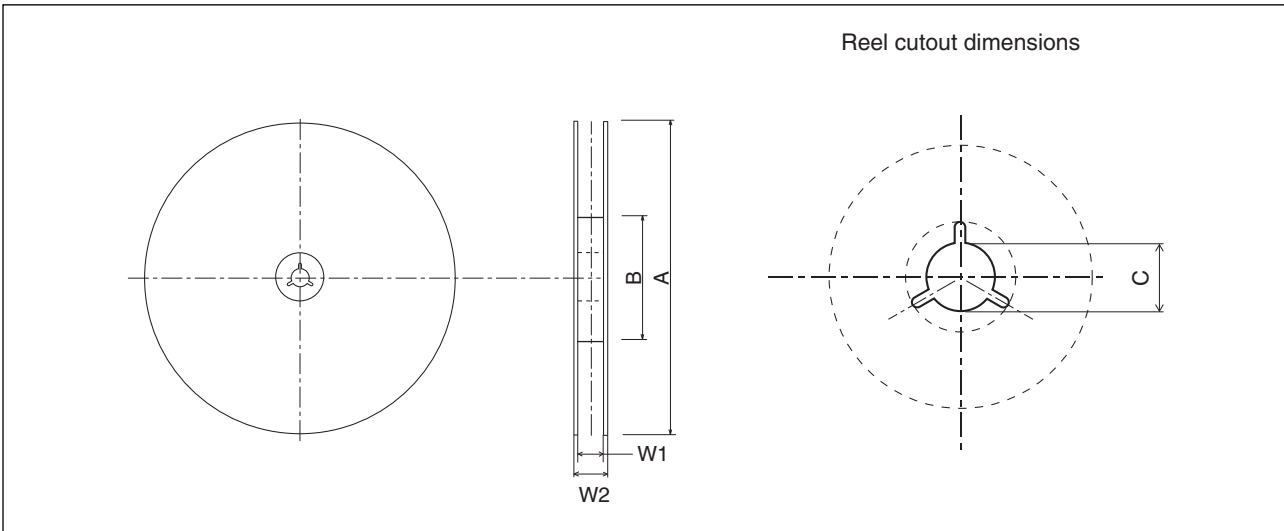


# MB85RS256LYA(AEC-Q100 Compliant)

## 2.2 IC orientation



## 2.3 Reel dimensions



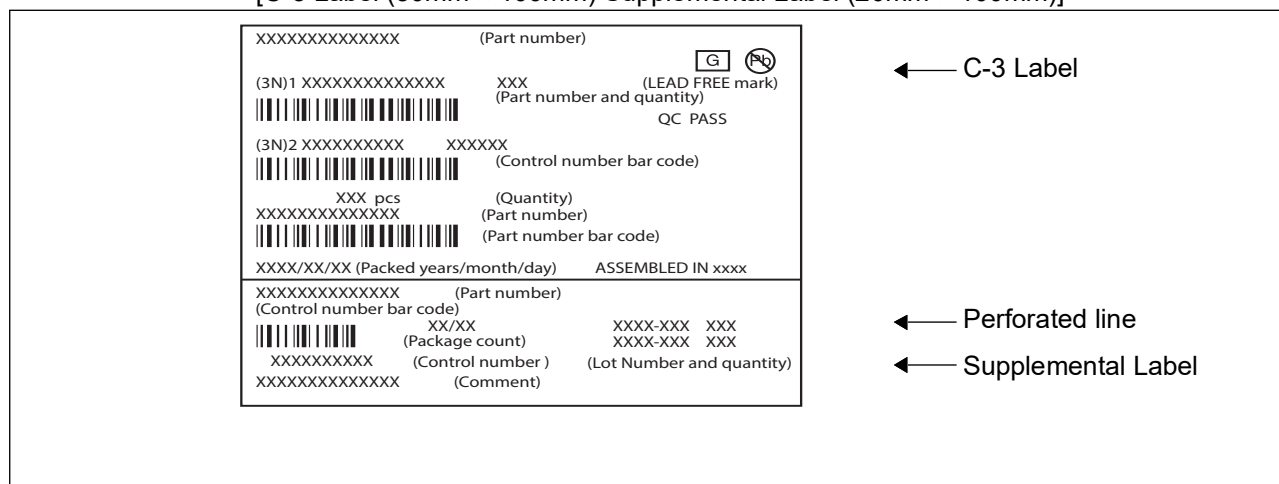
Dimensions in mm

A	B	C	W1	W2
254	100	13	13.5	17.5

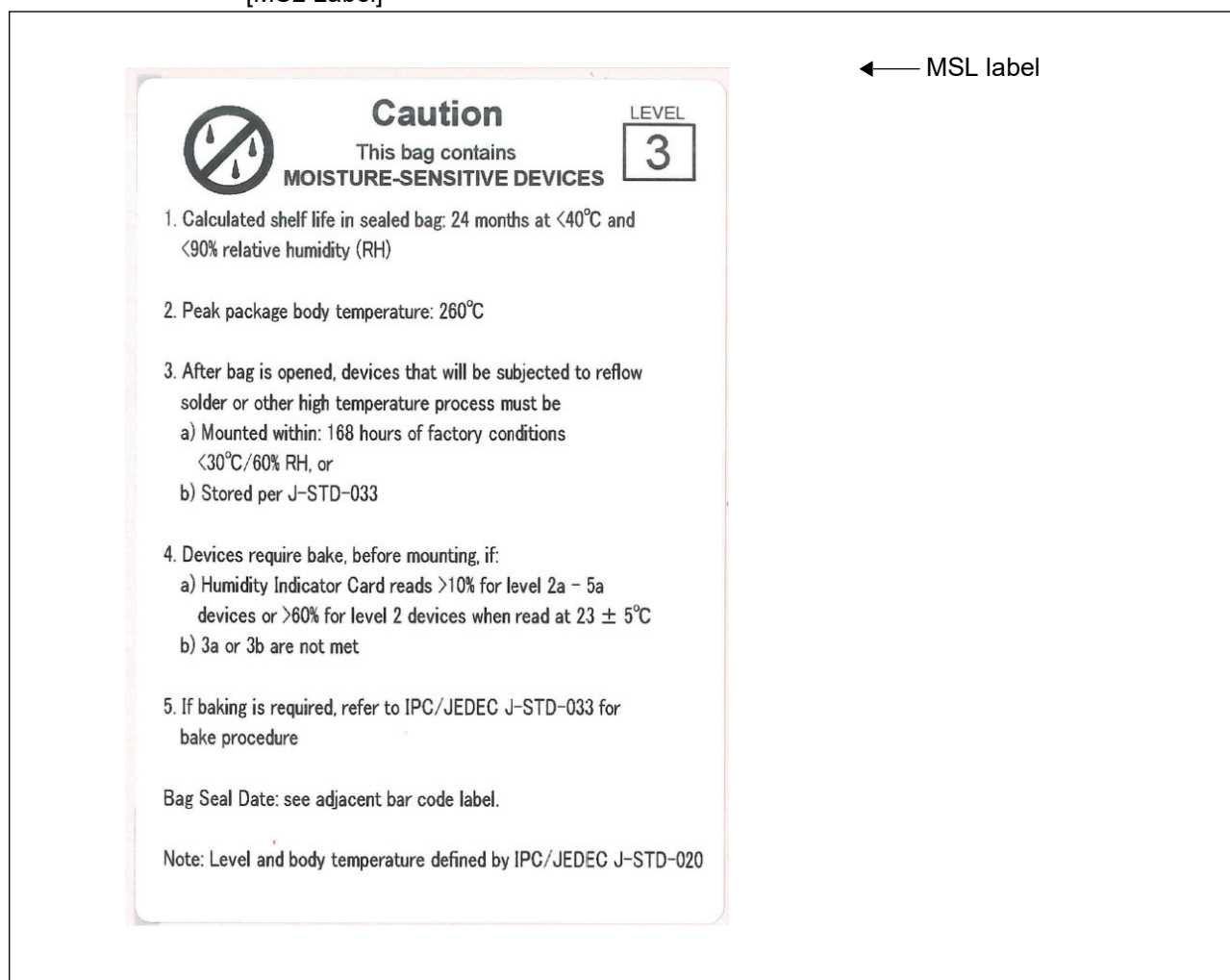
# MB85RS256LYA(AEC-Q100 Compliant)

## 2.4 Product label indicators (examples)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)  
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



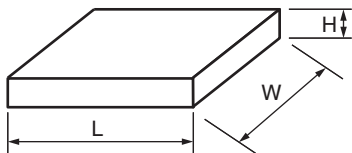
Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)  
[MSL Label]



# MB85RS256LYA(AEC-Q100 Compliant)

## 2.5 Dimensions for Containers

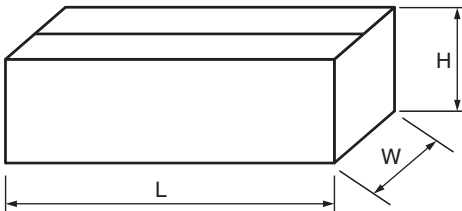
### (1) Dimensions for inner box



Tape width	L	W	H
12	266	263	52

(Dimensions in mm)

### (2) Dimensions for outer box



L	W	H
555	255	160

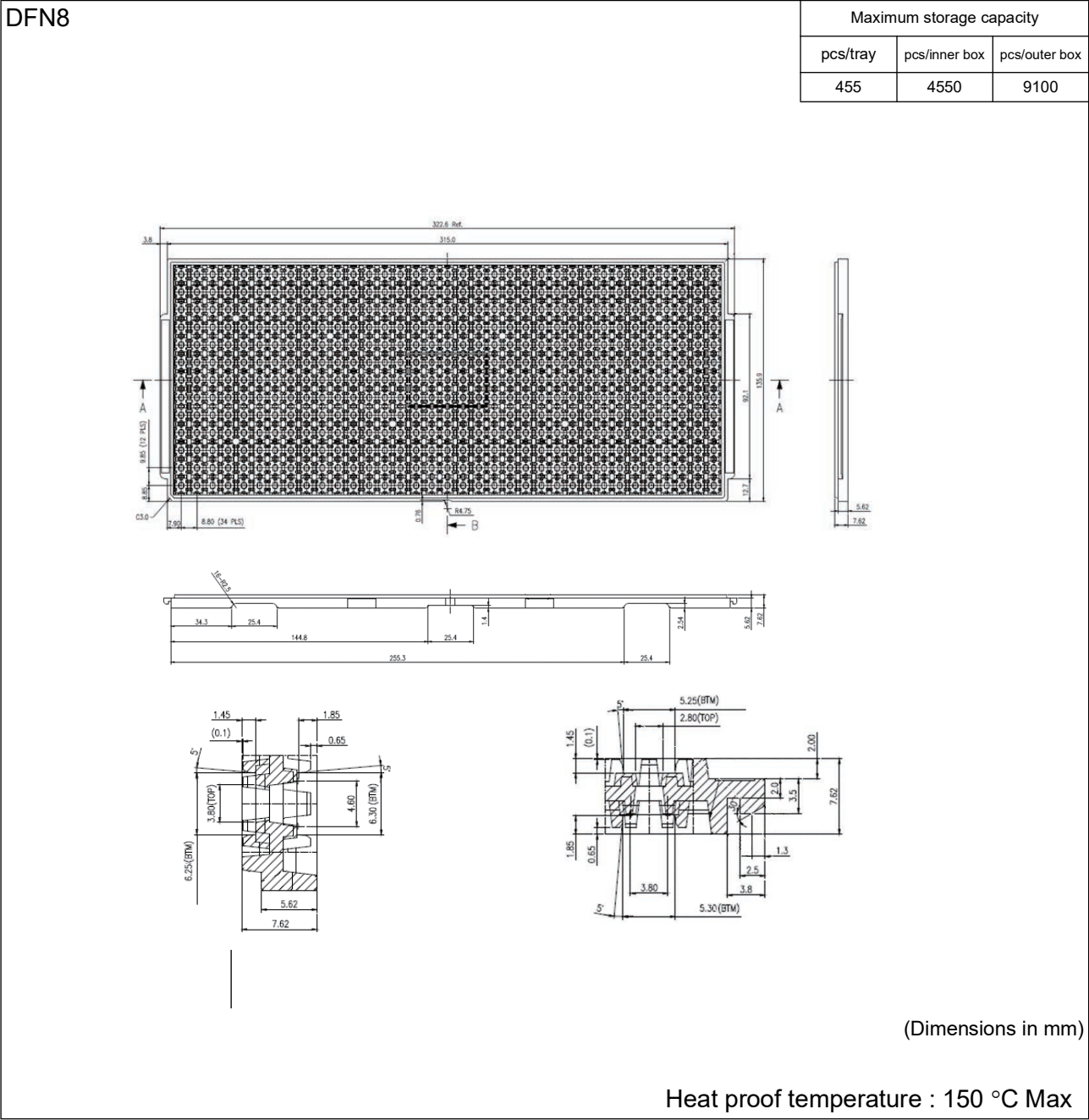
(Dimensions in mm)

# MB85RS256LYA(AEC-Q100 Compliant)

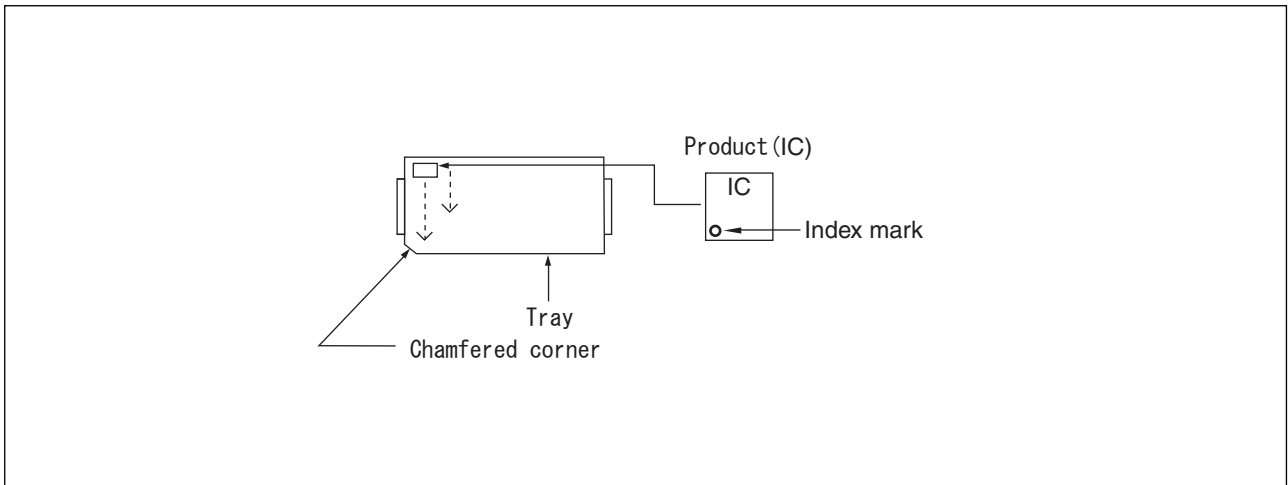
(2) MB85RS256LYAPN-GS-AWE1/MB85RS256LYAPN-GS-AWEWE1

## 1. Tray (MB85RS256LYAPN-GS-AWE1)

### 1.1 Tray Dimensions



## 1.2 IC orientation



# MB85RS256LYA(AEC-Q100 Compliant)

### 1.3 Product label indicators(example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)  
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

XXXXXXXXXXXXXX (Part number)

(3N)1 XXXXXXXXXXXXXXXX XXX (LEAD FREE mark)  
(Part number and quantity)

QC PASS

(3N)2 XXXXXXXXXXXXXXXX XXXXXX  
(Control number bar code)

XXX pcs (Quantity)

XXXXXXXXXXXXXXXXXX (Part number)

(Part number bar code)

XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx

XXXXXXXXXXXXXX (Part number)

XX/XX (Package count)

XXXX-XXX XXX

XXXX-XXX XXX

XXXXXXXXXXXXX (Control number ) (Lot Number and quantity)

XXXXXXXXXXXXXXXXXX (Comment)

← C-3 Label

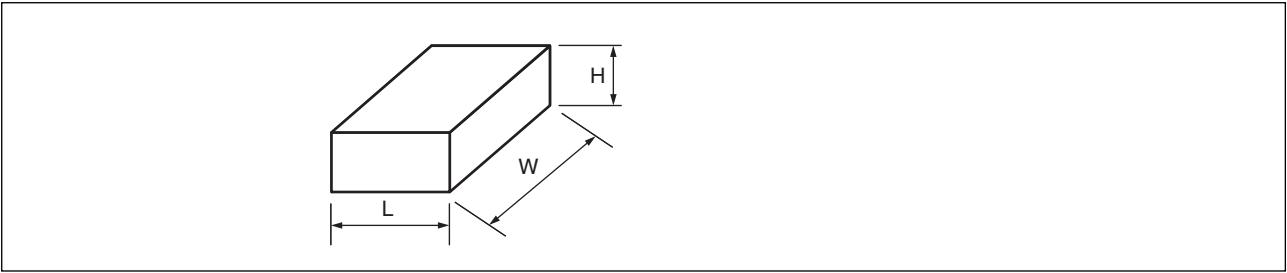
← Perforated line

← Supplemental Label

# MB85RS256LYA(AEC-Q100 Compliant)

## 1.4 Dimensions for Containers

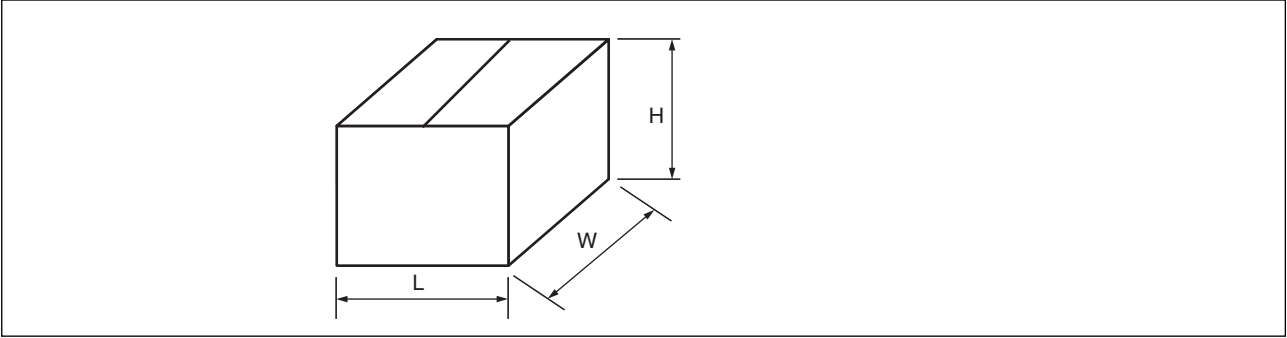
### (1) Dimensions for inner box



L	W	H
175	375	110

(Dimensions in mm)

### (2) Dimensions for outer box



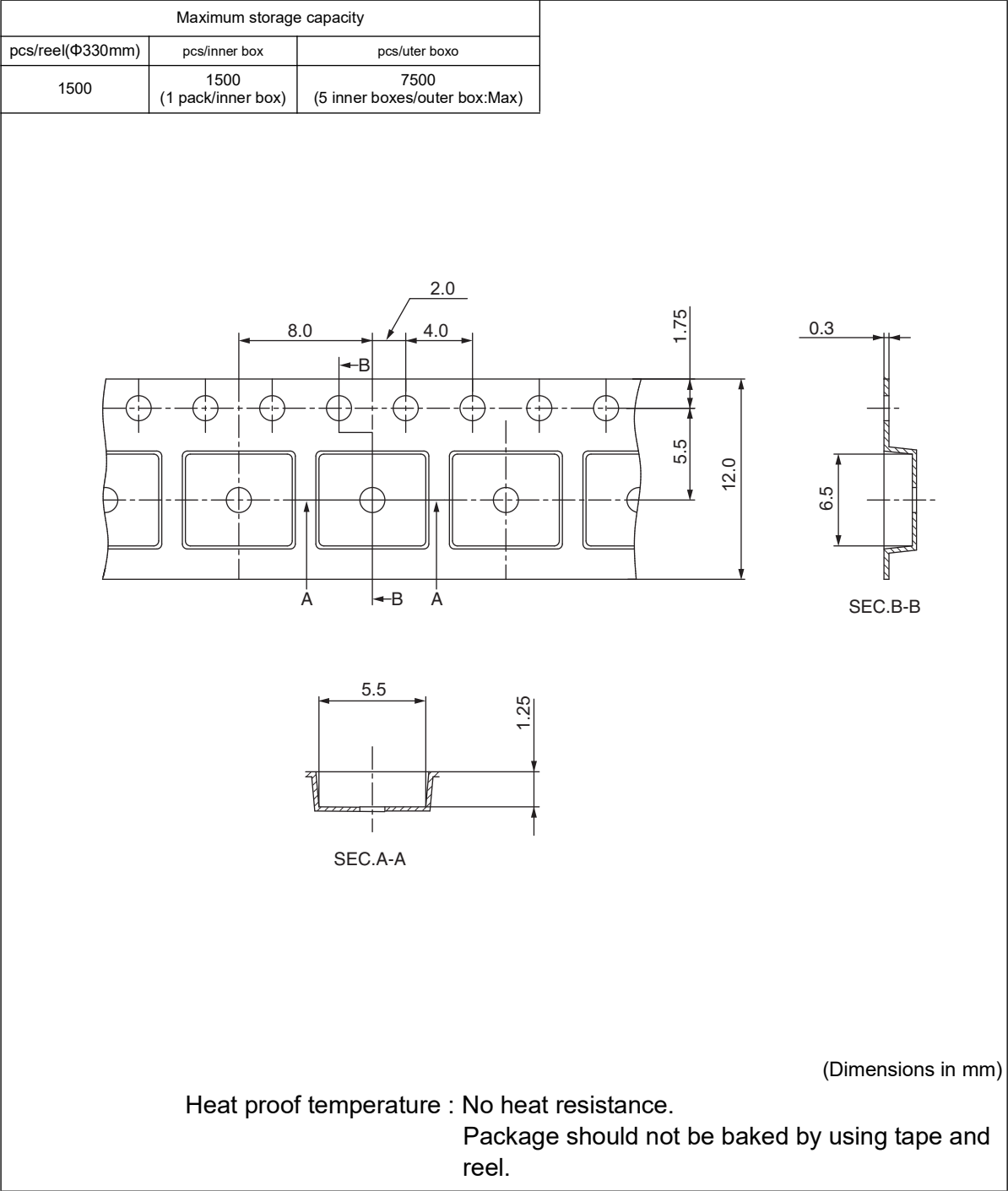
L	W	H
190	380	330

(Dimensions in mm)

# MB85RS256LYA(AEC-Q100 Compliant)

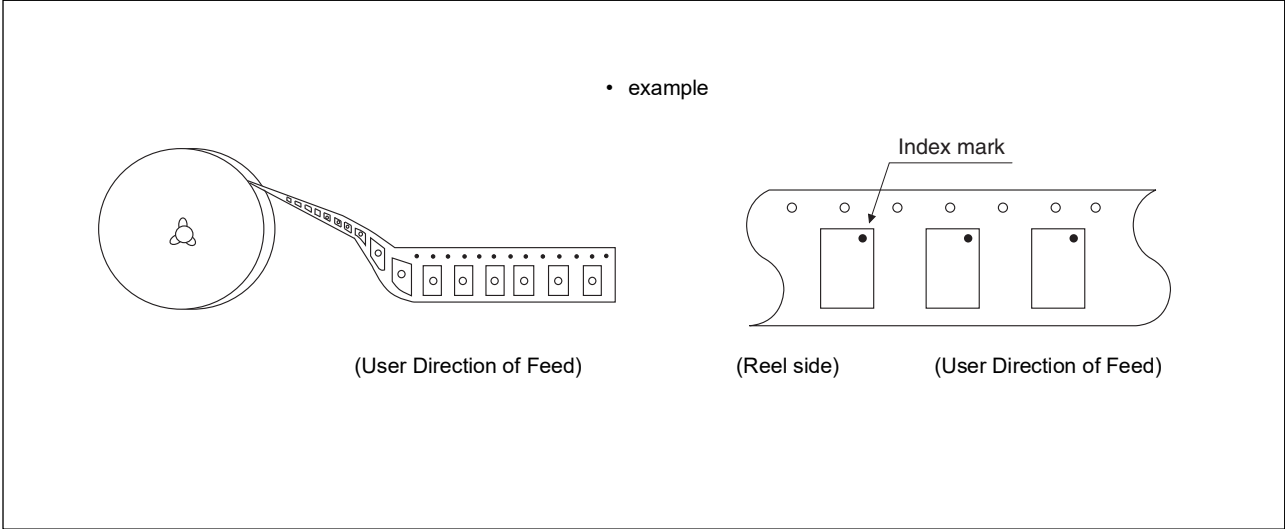
## 2. Emboss Tape (MB85RS256LYAPN-GS-AWEWE1)

### 2.1 Tape Dimensions (not drawn to scale)(8-pin plastic DFN 5mm × 6mm)

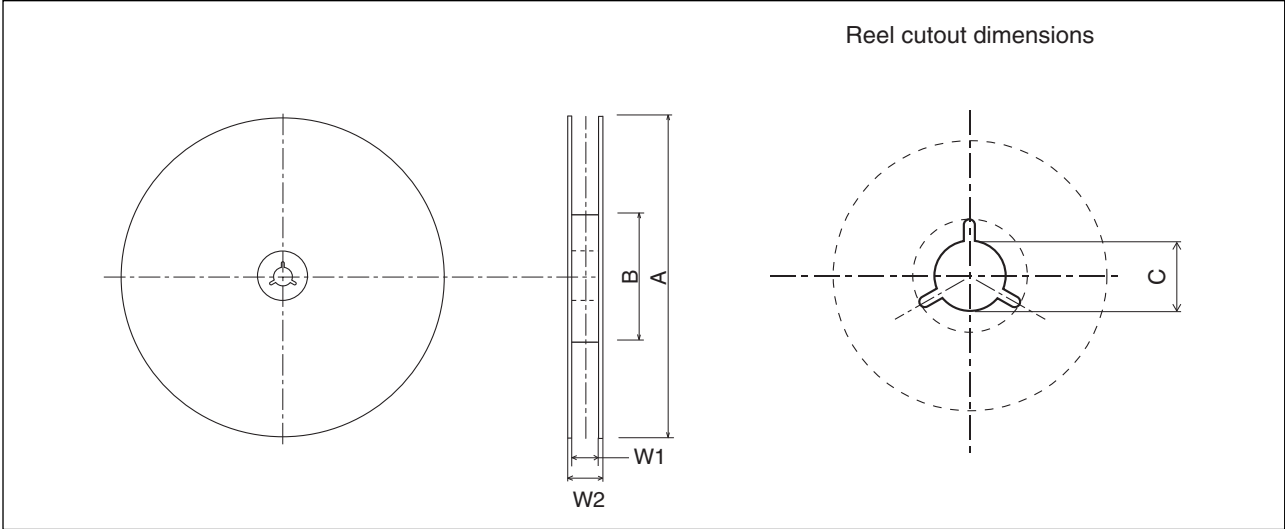


# MB85RS256LYA(AEC-Q100 Compliant)

## 2.2 IC orientation



## 2.3 Reel dimensions



Dimensions in mm

A	B	C	W1	W2
330	100	13	13.5	17.5

# MB85RS256LYA(AEC-Q100 Compliant)

## 2.4 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)  
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

XXXXXXXXXXXXXX (Part number)		G (LEAD FREE mark)	QC PASS
(3N)1 XXXXXXXXXXXXXXXX XXXXXXXXXXXXXX XXXXXXXXXXXXXX	XXX (Part number and quantity)		
(3N)2 XXXXXXXXXXXXXXXX XXXXXXXXXXXXXX XXXXXXXXXXXXXX	XXXXXX (Control number bar code)		
XXX pcs (Quantity)	XXXXXXXXXXXXXX (Part number)		
XXXXXXXXXXXXXX (Part number bar code)			
XXXX/XX/XX (Packed years/month/day)	ASSEMBLED IN xxxx		
XXXXXXXXXXXXXX (Part number)			
XXXXXXXXXXXXXX (Control number bar code)	XX/XX (Package count)	XXXX-XXX XXX	XXXX-XXX XXX
XXXXXXXXXXXXXX (Control number)	(Lot Number and quantity)		
XXXXXXXXXXXXXX (Comment)			

← C-3 Label

← Perforated line

← Supplemental Label

Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)

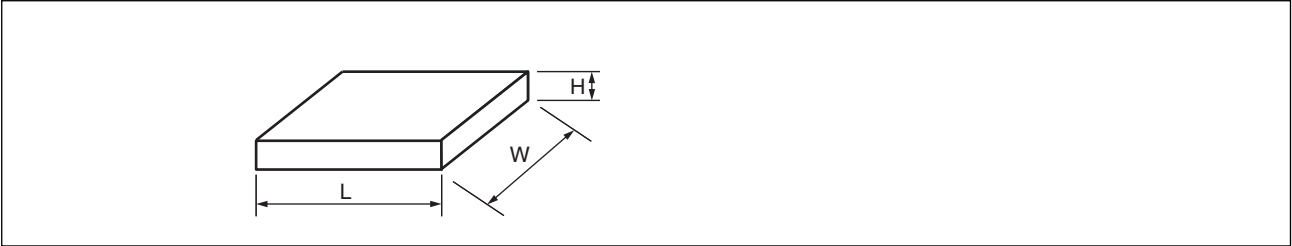
[MSL Label]

MOISTURE-SENSITIVE DEVICES		LEVEL
<b>注意</b>		3
<ol style="list-style-type: none"> <li>ドライバック包装の保管期限は、24ヶ月（25℃/80%RH未満）です。</li> <li>本製品の耐熱温度は、<u>260℃</u> です。</li> <li>袋開封後は、下記a) b)条件下で、ご使用ください。 <ol style="list-style-type: none"> <li><u>168</u> 時間以内（30℃/60%RH以下）</li> <li>J-STD-033条件</li> </ol> </li> <li>以下の条件の場合は、実装前にベークしてください。 <ol style="list-style-type: none"> <li>23±5℃の環境下でインジケータカードの10%を超えた場合</li> <li>3a、3bの条件に合致しない場合</li> </ol> </li> <li>ベーク必要の場合はIPC/JEDEC J-STD-033 参照してください。</li> </ol>		
<b>CAUTION</b>		
<ol style="list-style-type: none"> <li>Calculated shelf life in sealed bag: 24 months at &lt;25℃ / 80% RH</li> <li>Peak package body temperature: <u>260℃</u></li> <li>After bag is opened, devices that will be subjected to reflow solder or other high temperature process must <ol style="list-style-type: none"> <li>Mounted within: <u>168</u> hours of factory conditions ≤30℃/60%RH</li> <li>Stored per J-STD-033</li> </ol> </li> <li>Devices require bake, before mounting, if: <ol style="list-style-type: none"> <li>Humidity Indicator Card is &gt; 10% when read at 23±5℃</li> <li>3a or 3b not met.</li> </ol> </li> <li>If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.</li> </ol>		
包装日：品名ラベルをご確認下さい Bag Seal Date: See adjacent bar code label		 * F 0 0 0 1 *
Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

← MSL label

2.5 Dimensions for Containers

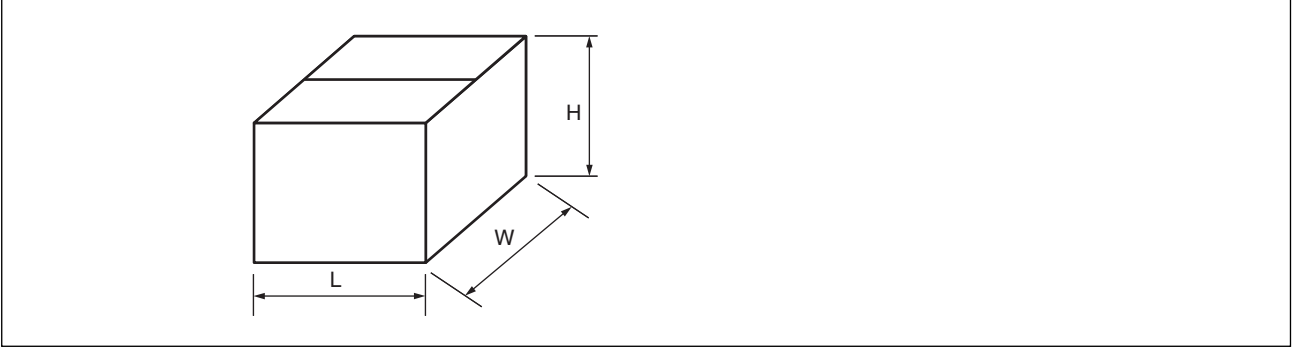
(1) Dimensions for inner box



Tape width	L	W	H
12	350	335	35

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
384	368	225

(Dimensions in mm)

# MB85RS256LYA(AEC-Q100 Compliant)

## FUJITSU SEMICONDUCTOR MEMORY SOLUTION LIMITED

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