Memory FeRAM

4 M Bit (256 K × 16)

MB85R4002A

DESCRIPTIONS

The MB85R4002A is an FeRAM (Ferroelectric Random Access Memory) chip consisting of 262,144 words \times 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85R4002A is able to retain data without using a back-up battery, as is needed for SRAM. The memory cells used in the MB85R4002A can be used for 10^{10} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E²PROM. The MB85R4002A uses a pseudo-SRAM interface.

FEATURES

Bit configuration	: 262,144 words \times 16 bits
 LB and UB data byte control 	
 Read/write endurance 	: 10 ¹⁰ times / byte
Data retention	: 10 years (+ 55 °C), 55 years (+ 35 °C)
 Operating power supply voltage 	: 3.0 V to 3.6 V
Low power operation	: Operating power supply current 15 mA (Typ)
	Standby current 50 μA (Typ)
· Operation ambient temperature range	e : − 40 °C to + 85 °C
Package	: 48-pin plastic TSOP
	RoHS compliant



■ PIN ASSIGNMENTS



PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 8, 17 to 25, 48	A0 to A17	Address Input pins
29 to 36, 38 to 45	I/O1 to I/O16	Data Input/Output pins
26	CE1	Chip Enable 1 Input pin
12	CE2	Chip Enable 2 Input pin
11	WE	Write Enable Input pin
28	ŌĒ	Output Enable Input pin
14, 15	LB, UB	Data Byte Control Input pins
16, 37	VDD	Supply Voltage pins Connect all two pins to the power supply.
13, 27, 46	VSS	Ground pins Connect all three pins to ground.
9, 47	NC	No Connect pins Leave these pins open, or connect to VDD or VSS.
10	DNU	Do Not Use pin Make sure to connect this pin to VDD.



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BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Mode	CE1	CE2	WE	OE	LB	UB	I/O1 to I/O8	I/O9 to I/O16	Supply Current		
	Н	Х	Х	Х	Х	Х					
Standby Procharge	Х	L	Х	Х	Х	Х			Standby		
	Х	Х	Н	Н	Х	Х	1 11-2	111-2	(Isв)		
	Х	Х	Х	Х	Н	Н					
					L	L	Data Output	Data Output			
		н	н	L	L	Н	Data Output	Hi-Z			
Bood					Н	L	Hi-Z	Data Output			
Read					L	L	Data Output	Data Output			
	L		Н	Н	L	L	н	Data Output	Hi-Z		
					Н	L	Hi-Z	Data Output			
Read			Н		L	L	Data Output	Data Output			
(Pseudo-SRAM,	L	н		Н	Н	T I	L	Н	Data Output	Hi-Z	
OE control*1)					Н	L	Hi-Z	Data Output	Operation		
					L	L	Data Input	Data Input	(Idd)		
		н	L	н	L	Н	Data Input	Hi-Z			
\\/rito					Н	L	Hi-Z	Data Input			
VVIILE					L	L	Data Input	Data Input			
	L	_√	L	н	L	н	Data Input	Hi-Z	-		
					Н	L	Hi-Z	Data Input			
Write					L	L	Data Input	Data Input	1		
(Pseudo-SRAM,	L	н	1	н	L	Н	Data Input	Hi-Z	1		
WE control*2)					Н	L	Hi-Z	Data Input	1		

Note: $L = V_{IL}$, $H = V_{IH}$, X can be either H, L, $\neg L$ or $\Box \Gamma$, Hi-Z = High Impedance

*1 : $\overline{\text{OE}}$ control of the Pseudo-SRAM means the valid address at the falling edge of $\overline{\text{OE}}$ to read.

*2 : $\overline{\text{WE}}$ control of the Pseudo-SRAM means the valid address and data at the falling edge of $\overline{\text{WE}}$ to write.

■ ABSOLUTE MAXIMUM RATINGS

Paramotor	Symbol	Rat	Unit	
	Symbol	Min	Мах	Unit
Power Supply Voltage*	Vdd	-0.5	+4.0	V
Input Pin Voltage*	Vin	-0.5	$V_{\text{DD}} + 0.5 \ (\le 4.0)$	V
Output Pin Voltage*	Vout	-0.5	$V_{\text{DD}} + 0.5 \ (\le 4.0)$	V
Operation Ambient Temperature	TA	-40	+85	٥C
Storage Temperature	Tstg	-55	+125	٥C

* : All voltages are referenced to VSS (ground 0 V).

WARNING:

RECOMMENDED OPERATING CONDITIONS

Paramotor	Symbol		Unit		
Falameter	Symbol	Min	Тур	Мах	Unit
Power Supply Voltage ^{*1}	Vdd	3.0	3.3	3.6	V
Operation Ambient Temperature*2	TA	-40		+85	°C

*1 : All voltages are referenced to VSS (ground 0 V).

*2 : Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING:



ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions) Value **Parameter** Symbol Condition Unit Max Min Typ $V_{IN} = 0 V to V_{DD}$ Input Leakage Current*1 |Lu| ____ 10 μA VOUT = $0 V \text{ to } V_{DD}$, Output Leakage Current 10 ILO μA $\overline{CE}1 = V_{IH} \text{ or } \overline{OE} = V_{IH}$ $\overline{CE}1 = 0.2 \text{ V}, \text{ CE}2 = \text{V}_{DD} - 0.2 \text{ V},$ **Operating Power Supply** 15 20 DD mΑ Current*2 $I_{out} = 0 \text{ mA}$ $\overline{CE}1 \ge V_{DD} - 0.2 V$ $CE2 \le 0.2 V$ Standby Current*3 50 150 lsв μA $\overline{OE} \ge V_{DD} - 0.2 \text{ V}, \ \overline{WE} \ge V_{DD} - 0.2 \text{ V}$ $\overline{LB} \ge V_{DD} - 0.2 \text{ V}, \ \overline{UB} \ge V_{DD} - 0.2 \text{ V}$ $V_{DD} + 0.5$ High Level Input Voltage $V_{DD} = 3.0 \text{ V to } 3.6 \text{ V}$ V Vн $V_{DD} \times 0.8$ (≤ 4.0) VIL V Low Level Input Voltage $V_{DD} = 3.0 V \text{ to } 3.6 V$ -0.5 +0.6Iон = - 1.0 mA $V_{DD} \times 0.8$ V High Level Output Voltage Vон ____ ____ V Low Level Output Voltage Vol IoL = 2.0 mA 0.4 _

*1 : This also applies to DNU pins.

*2 : During the measurement of IDD, the Address and Data In were taken to only change once per active cycle. Iout : output current

*3 : All pins other than setting pins shall be input at the CMOS level voltages such as H \geq V_{DD} – 0.2 V, L \leq 0.2 V.

2. AC Characteristics

 AC Test Conditions 							
Power Supply Voltage		:	3.0	V	to	3.6	V
Operation Ambient Temperature		:	-40	°C	to	+85	°C
Input Voltage Amplitude		:	0.3	V	to	2.7	V
Input Rising Time			:		5		ns
Input Falling Time			:		5		ns
Input Evaluation Level		:	2.0	V	/	0.8	V
Output Evaluation Level		:	2.0	V	/	0.8	V
Output Load Capacitance	: 50 pF						

(1) Read Cycle

Deremeter	Symbol	Va	Unit	
Parameter	Symbol	Min	Max	Unit
Read Cycle time	t _{RC}	150		ns
CE1 Active Time	t _{CA1}	120		ns
CE2 Active Time	tca2	120		ns
OE Active Time	t _{RP}	120		ns
LB, UB Active Time	tвр	120		ns
Precharge Time	t _{PC}	20		ns
Address Setup Time	tas	0		ns
Address Hold Time	tан	50		ns
OE Setup Time	tes	0		ns
LB, UB Setup Time	tвs	5		ns
Output Data Hold time	tон	0		ns
Output Set Time	t∟z	30		ns
CE1 Access Time	t _{CE1}		120	ns
CE2 Access Time	t _{CE2}		120	ns
OE Access Time	toe		120	ns
Output Floating Time	tонz		20	ns

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(2) Write Cycle

Parameter	Symbol	Va	Unit	
Falanelei	Symbol	Min	Max	Unit
Write Cycle Time	twc	150		ns
CE1 Active Time	t _{CA1}	120		ns
CE2 Active Time	tca2	120		ns
LB, UB Active Time	tвр	120		ns
Precharge Time	t _{PC}	20		ns
Address Setup Time	tas	0		ns
Address Hold Time	tан	50		ns
LB, UB Setup Time	t₿s	5		ns
Write Pulse Width	t wp	120		ns
Data Setup Time	t _{DS}	0		ns
Data Hold Time	tон	50		ns
Write Setup Time	tws	0		ns

3. Pin Capacitance

Paramotor	Symbol	Condition		Unit		
Falailletei	Symbol	Condition	Min	Тур	Мах	Unit
Input Capacitance	CIN				10	pF
Output Capacitance	Соит	$V_{DD} = V_{IN} = V_{OUT} = 0 V,$ f = 1 MHz T _A = + 25 °C			10	pF
DNU Pin Input Capacitance	CDNU	,			10	pF

■ TIMING DIAGRAMS

1. Read Cycle Timing (CE1 Control)



2. Read Cycle Timing (CE2 Control)



3. Read Cycle Timing (OE Control)



4. Write Cycle Timing (CE1 Control)



5. Write Cycle Timing (CE2 Control)



6. Write Cycle Timing (WE Control)



POWER ON/OFF SEQUENCE



Paramotor	Symbol		Unit			
Falameter	Symbol	Min	Тур	Max	Sint	
CE1 level hold time for Power OFF	t PD	85	—		ns	
CE1 level hold time for Power ON	t PU	85			ns	
Power supply rising time	t _R	0.05		200	ms	

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

In case the power is turned on or off, use the power supply reset IC and fix the CE2 to low level, to prevent unexpected writing. Use either of $\overline{CE1}$ or CE2, or both to disable control of the device.

■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter	
Read/Write Endurance*1	10 ¹⁰	_	Times/byte	Operation Ambient Temperature $T_A = +85 \ ^{\circ}C$	
Data Retention*2	Potention*2 10 — Voor		Operation Ambient Temperature $T_A = +55 \ ^{\circ}C$		
		55		rears	Operation Ambient Temperature $T_A = +35 \ ^{\circ}C$

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

NOTES ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.



■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant		≥ 2000 V
ESD MM (Machine Model) JESD22-A115 compliant		≥ 200 V
ESD CDM (Charged Device Model) JESD22-C101 compliant	-	
Latch-Up (I-test) JESD78 compliant	MB85R4002ANC-GE1	
Latch-Up (V _{supply} overvoltage test) JESD78 compliant		
Latch-Up (Current Method) Proprietary method		≥ 300 mA
Latch-Up (C-V Method) Proprietary method		

• Current method of Latch-Up Resistance Test



Note : The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow. Confirm the latch up does not occur under I_{IN} = ± 300 mA. In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement. • C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.

Repeat this process 5 times. However, if the latch-up condition occurs before completing 5 times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS. Please refer to the following web site for more details of current status on contained restricted substances in our products.

http://www.fujitsu.com/global/services/microelectronics/environment/products/

■ ORDERING INFORMATION

Part Number	Package	Shipping form	Minimum shipping quantity
MB85R4002ANC-GE1	48-pin plastic TSOP	Tray	*

*: Please contact our sales office about minimum shipping quantity.



■ PACKAGE DIMENSIONS







SHIPPING FORM

1. Tray

1.1 Tray Dimensions



1.2 IC orinentation





1.3 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping) [C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]





1.4 Dimensions for Containers

(1) Dimensions for inner box



L	W	Н
165	360	75
		(Dimensions in mm)

(2) Dimensions for outer box



L	W	Н
355	385	195
		(5) · · · ·

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
17	MARKING	New marking format is added.



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