Press Release

Fujitsu Microelectronics Limited

Fujitsu Launches SD Multi-Decoder LSI Supporting MPEG-2 & H.264

- For expanding H.264 SD broadcasts in Russia, Eastern Europe, China -

Tokyo, November 27, 2008 - Fujitsu Microelectronics Limited today announced the launch of multi-decoder LSI chips that support decoding of MPEG-2(1) and H.264(2) video compression formats for Standard Definition (SD) video, in particular for SD digital broadcasts in Russia, eastern Europe and China. Sample shipments of the new MB86H01 series will start from December 1, 2008.

These are system LSIs that are ideally suited to be used in TV and set-top-box(STB) equipment targeted for the Russian, eastern European and China markets. These new products support the DVB(3) broadcasting standard used in those regions, with MPEG-2 and H.264 decoders integrated into a single chip with the functionality necessary for receiving SD broadcasts. Proprietary H.264 decoder technology provides low power consumption, while the availability of small packaging makes these decoder LSIs ideal to be used in portable devices like personal navigation devices (PND) with built-in TV receivers.

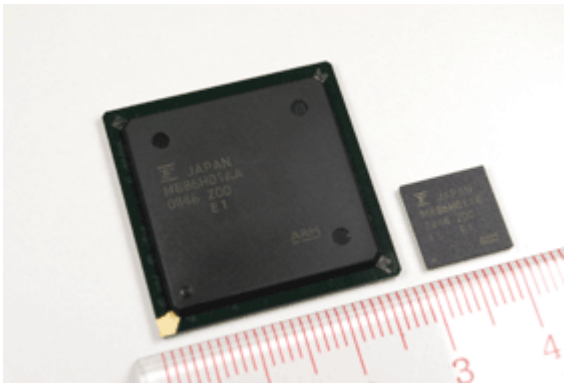

Figure 1: SD multi-decoder LSI, MB86H01

The DVB digital broadcasting standard is used in Europe, Russia, and by some broadcast systems in China. For SD broadcasting, the MPEG-2 compression format is widely used, however it is expected that the next-generation compression format H.264 will ramp up in eastern Europe including Russia. Also, the H.264 format is used in some cable TV services in China for interactive video-on-demand (VoD)(4).

Up until now, Fujitsu Microelectronics has had success with its SmartMPEG series of MPEG-2 decoder LSIs for SD digital TV broadcasts for the DVB standard. SmartMPEG has been implemented widely in TVs, STBs, and portable TV receivers especially in Europe.

With the shift of SD broadcasting to the H.264 format in Russia, eastern Europe, China, and elsewhere, TVs and STBs for these regions need to be able to handle decoding of both MPEG-2 and H.264 formats. Targeting such markets, Fujitsu Microelectronics is offering this new MB86H01 series, which consists of two (2) SD multi-decoder LSI products (MB86H01 AA / MB86H01 AB) that support both MPEG-2 and H.264 formats.

The new LSI multi-decoders include the necessary functionality for TVs and STBs to process SD digital broadcasts, including two (dual) MPEG-2 decoders and one H.264 decoder. The dual MPEG-2 decoders enable the processing of two (2) video streams that can be used in digital video recorders (DVR) with twin tuners. It also allows viewing of two (2) programs at the same time with picture-in–picture.

Using proprietary H.264 decoder technology, the power consumption for the H.264 decoder is

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reduced to a low level. Combined with the small 10 mm x 10mm package (FBGA 240-pin), the decoder is ideal for use in portable or small form-factor devices. A high-speed USB2.0 OTG controller is also integrated, giving excellent connectivity to external devices, such as digital cameras.

Leveraging Fujitsu's highly regarded expertise in image and video processing-related technologies and products, Fujitsu Microelectronics will continue to strengthen its video processing LSIs for the TV and set-top-box markets, focusing on video-processing ASSPs.

Sample Availability

MB86H01 Series

Product Name	Sample Availability
MB86H01 AA (PBGA 256-pin) MB86H01 AB (FBGA 240-pin)	From December 1, 2008

Key Features

1. **Includes MPEG-2 dual decoders & H.264 decoder for digital broadcasts in Russia, eastern Europe, China**
   Decodes both SD MPEG-2 and H.264 compression formats so it can handle not just the MPEG-2 SD broadcasts in Europe (in particular western Europe), but also supports the H.264 format for SD broadcasts which are expected to ramp-up in eastern Europe and Russia, as well as being used in some Chinese cable TV services for interactive Video-on-Demand (VoD). Having dual MPEG-2 decoders allows picture-in–picture on screen to enable viewing of two (2) programs simultaneously, as well as being suited to DVRs with twin tuners.

2. **Integrates on a single chip functions necessary for processing SD broadcasts**
   These LSIs integrate into a single chip a 202.5 MHz ARC Tangent-A4 CPU together with the necessary video and audio decode functions, as well as screen display functionality needed to receive digital broadcasts, thus enabling easy system creation by customers.

3. **Small form-factor, necessary for portable devices**
   The low power consumption was achieved with a proprietary developed H.264 decoder technology. The MB86H01 series offers a 27mm x 27mm package (PDGA 256-pin), as well as a small 10 mm x 10mm package (FBGA 240-pin) ideal for use in portable devices like personal navigation devices (PND) with built-in TV receivers.

4. **Succession to existing SmartMPEG series architecture**
   This LSI has package and pin compatibility with the existing SmartMPEG-C series, as well as maintaining architectural compatibility. This allows current SmartMPEG users to efficiently upgrade or develop their systems.

Glossary and Notes

1 **MPEG-2:**

A video compression format (codec) that is part of the MPEG standard for video compression. MPEG-2 is widely used in DVDs and other video products.

2 **H.264:**

A video compression standard defined by the International Telecommunication Union, Telecommunication Standardization Sector (ITU-T). A video-encoding format noted for offering more compression than MPEG-2 and other earlier formats. The International Organization for Standardization/International Electrotechnical Commission (ISO/IEC) has defined the MPEG-4 Part 10 Advanced Video Coding (MPEG-4 AVC), however it is the same as H.264.

3 **DVB:**

Digital Video Broadcasting. A set of internationally approved open standards for digital television broadcasts. DVB is used in many countries, especially in Europe.

4 **Interactive video on demand (VoD) service:**

A 2-way service where the video program selected by the user is transmitted directly to the user.

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For more information

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Fujitsu Microelectronics Ltd. - Video Processing LSIs

About Fujitsu Microelectronics (FML)

Fujitsu Microelectronics Limited designs and manufactures semiconductors, providing highly reliable, optimal solutions and support to meet the varying needs of its customers. Products and services include ASICs/COT, ASSPs, power management ICs, and flash microcontrollers, with wide-ranging expertise focusing on imaging, wireless, automotive and security applications. Fujitsu Microelectronics also drives power efficiency and environmental initiatives. Headquartered in Tokyo, Fujitsu Microelectronics Limited was established as a subsidiary of Fujitsu Limited on March 21, 2008. Through its global sales and development network, with sites in Japan and throughout Asia, Europe, and the Americas, Fujitsu Microelectronics offers semiconductor solutions to the global marketplace. For more information: http://jp.fujitsu.com/group/fml/en/

Key Specifications of the Multi-decoder, MB86H01

Internal CPU		ARC Tangent-A4 (202.5 MHz) ARM7TDMI-S™ (67.5 MHz): for H.264 video decoding
Video	Profile	H.264 Main Profile / Level3.0 decoder, MPEG-2 Video Main Profile /Main Level decoder
	Video Encoder	Supports PAL/NTSC/SECAM, 5 channel Video DAC embedded, supports Teletext/WSS/PDC/CC/VBID
	Interface	ITU-R BT.656 input, digital RGB888 output, YCrCb analog SD output
Audio	Formats	MPEG-1/2 Layer I/II
	Channels	2 channel
	Interface	L/R serial, I2S、S/P-DIF
TS processing	Format	MPEG-2 TS
	Interface	3 input streams, built-in DVB descrambler
	Encryption processing	3DES encryption/decryption
DDR Memory Interface		16 bit DDR-SDRAM 135MHz, 128 Mbit ~ 512 Mbit SDRAM
Flash Memory Interface		Supports Serial Flash, NOR Flash, NAND Flash
Display		6 planes: BG(Back Ground), Video, OSDx4
USB		USB 2.0 High Speed OTG Controller (UPLI interface)
ATA		Multiword DMA ATA interface
UPI		NAND/NOR FLASH, Common Interface
Peripheral I/O		UART, Smart Cardx2, I^2C, GPIO, PWM, IR Rx/Tx
Input Clock Frequency		27 MHz
Operating Frequency		Internal Bus Clock: 135 MHz DDR Memory interface: 135 MHz
Package		PBGA 256 pin, 27 mm x 27 mm (ball pitch 1.27mm) FBGA 240 pin, 10mmx10mm (ball pitch 0.5mm)
Operating Voltage		Core: 1.2V, I/O: 3.3V DDR memory interface: 2.5V