Fujitsu Launches Digital HDTV SoC for Superior Picture Quality Digital HDTV

- TV engine integrated with multi-decoder reduces total cost -

Tokyo, September 11, 2008 - Fujitsu Microelectronics Limited announced today that it has developed a digital HDTV system-on-chip (SoC) that integrates a video processing engine for superior picture quality, and a full high-definition (full HD, 1920 dots x 1080 lines) multi-decoder that decodes both MPEG-2(1) and H.264(2) video compression formats. The new chip, the MB86H70, is aimed for digital TVs receiving high-definition broadcasts that are ramping up in Europe. The chip is an application specific standard product (ASSP)(3), that features a proprietary video processing engine based on an algorithm by Fujitsu Laboratories Limited. By also including a proprietary picture quality adjustment tool that enables easy optimization of parameters by using a mouse, the

Figure 1: Digital HDTV SoC,
the MB**86H7**0

new LSI enables TV set makers to dramatically improve their design efficiencies with regard to picture quality settings. Furthermore, SoC integration of the video processing engine and multi-decoder allows the usage of common memory, thus enabling use of the chip by simply adding two 16-bit external memories, thereby reducing TV set makers' costs and development periods for both design and manufacturing. Sample shipment of this new SoC will start from mid-October 2008.
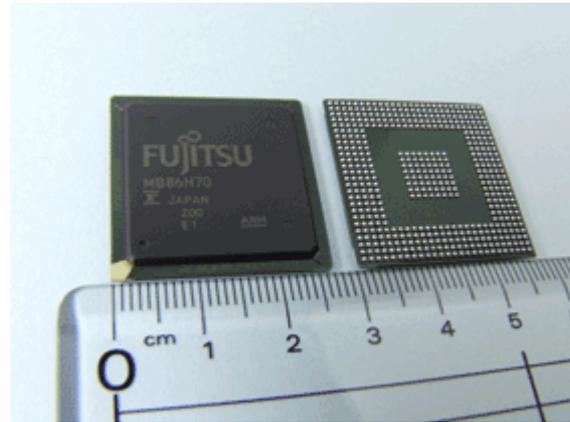
The MB86H70 will be exhibited at Fujitsu's booth (Stand 4.B75) at the International Broadcasting Conference 2008 (IBC 2008), the largest broadcasting and media trade exhibition that is held in Europe, to be held from September 12-16 in Amsterdam.

Background

Currently, in various regions such as Europe, digital TV broadcasting is offered in standard definition (SD) using the MPEG-2 video compression format. Next-generation broadcasts will be in HD, and it has been decided that H.264 will be the main format to be used. For example in France, HD digital TVs that are scheduled to be released to the market from the end of 2008 are required to be equipped with H.264 decoders. Thus, demand from the European TV market for high picture quality video processing engine chips with integrated H.264 decoders is expected to grow significantly.

Fujitsu Microelectronics already offers a full HD multi-decoder chip, the MB86H60, supporting MPEG-2 and H.264. In view of the ramp-up towards digital TVs for HD broadcasts in Europe, Fujitsu Microelectronics will offer this new ASSP that integrates as a SoC Fujitsu's proprietary superior picture quality video processing engine - based on an algorithm by Fujitsu Laboratories - with Fujitsu Microelectronics' already available full HD multi-decoder.

With digital TV, differing from analog TV, picture quality can be improved depending on the video processing engine. Up until now, Fujitsu Microelectronics has been providing to TV set makers its

expertise through custom ASIC(5) chip products. With this new digital HDTV SoC, Fujitsu Microelectronics' offerings for TV set makers expand to ASSPs, to improve the cost competitiveness of its customers.

Leveraging Fujitsu's highly regarded expertise in image processing-related technologies and products, Fujitsu Microelectronics has positioned its image processing ASSPs as a pillar for strategic growth for its ASSP business, providing world-class ASSPs for imaging, such as "Milbeaut™" LSIs for digital still cameras, as well as transcoder LSIs that convert MPEG-2 to H.264. Along with expanding its line-up of ASSPs for imaging through the new MB86H70, building on its video processing engine business, Fujitsu Microelectronics will continue to strengthen its product offerings for the TV market.

Sample Availability

Product Name	Sample Price	Sample Availability
MB86H70	5000 JPY	From mid-October, 2008

Sales Target
100,000 units per month

Key Features
1. Video processing engine for digital TV that realizes vivid colors and sharpness that are essential for HD broadcasts

    ·"Hybrid filter" automatically adjusts filter strength by separate areas in the picture.

    Distinguishes between contours of each object and other areas in the picture and distinctly enhances the contour to produce greater sharpness, while removing any noticeable noise from other areas. Such optimized filtering by area in the picture realizes a much smoother rendering of the picture.

    ·"Active tone curve control" automatically adjusts tone reproduction property in each scene

    Automatically selects optimized tone curve for various video scenes such as scenes where fine differences in brightness are required, or when there are large differences in brightness within a scene, thereby enabling a wide variety of images to be optimally displayed.

    ·Proprietary "Real 3-D color control" enables free selection of color range and control of desired level of color correction

    With standard color control methods, if a particular color is adjusted, it can change the color of the other colors of the entire picture. However, with Fujitsu's proprietary method that utilizes a 3-D color space, very precise color adjustment is possible without influencing other colors.

    ·Proprietary picture quality adjustment tool allows adjustment parameters to be easily set by using a mouse

    Each TV set maker has different picture quality requirements, which can be met simply and flexibly with Fujitsu's proprietary picture quality adjustment tool that is provided together with the new LSI. Using a graphical user interface (GUI), picture quality adjustment parameters can be easily set with a mouse while viewing the actual changes in picture quality. This allows TV set makers to dramatically improve their design efficiencies for picture quality settings.

In addition, other functions that are necessary to display HD video on a TV screen are included, such as motion adaptive de-interlacing(4) that reduces jagged edges that can be caused by diagonal lines, as well as a scalar that enlarges and reduces HD images.

2. Includes full HD MPEG-2 and H.264 decoders, supporting current and next-generation European broadcasting standards

This chip includes full HD MPEG-2 and H.264 decoders and thus can be used for current SD MPEG-2 broadcasts used widely in Europe and other regions, and for next-generation HD broadcasts using H.264. Includes audio decoders necessary for HD broadcasts in Europe such as Dolby® Digital, Dolby® Digital Plus(6), HE-AAC.

3. Integrates as a system-on-chip (SoC) key functions necessary for a TV

The CPU core in the chip is the ARM1176JZF-S™, which is supported by widely and easily available software in the market. Fujitsu also provides various software stacks for DVB(7), such as for teletext(8), subtitles, and JPEG decoding(9), which make it possible for TV set makers to more easily design and construct their systems with the necessary functions to view HD broadcasts.

4. Complete functionality by adding two 16-bit wide DDR2-SDRAMs

By simply connecting two 16-bit wide DDR2 SDRAM667 external memory chips as working memory to this digital HDTV SoC, the chip becomes fully functional, including CPU-based system control and digital-video decoding. This allows TV set makers to reduce the overall cost of their systems

Glossary and Notes

1 **MPEG-2:**
A video compression format (codec) that is part of the MPEG standard for video compression. MPEG-2 is widely used in DVDs and other video products.

2 **H.264:**
Refers to MPEG4 AVC/H.264, a video-encoding format (codec) noted for offering more compression than MPEG-2 and other earlier formats. Jointly defined by the International Telecommunication Union, Telecommunication Standardization Sector (ITU-T) and International Organization for Standardization/International Electrotechnical Commission (ISO/IEC), it is the most recent international standard for video compression.

3 **ASSP:**
Application specific standard product. LSIs for specific applications, such as image processing and network-related processing, which are sold to a wide range of customers.

4 **Motion adaptive de-interlacing:**
Conversion of an interlaced signal, containing every second (2nd) scanning line of a frame, to a progressive signal, by introducing line data to give a full frame while taking into account motion between frames.

5 **ASIC:**
Application specific IC. Customized ICs for specific applications (customers).

6 **Dolby® Digital Plus:**
Fujitsu Microelectronics plans to support this audio format from around November, 2008.

7 **DVB:**
Digital Video Broadcasting. A set of internationally approved open standards for digital television broadcasts. DVB is used in many countries, especially in Europe.

8 **Teletext:**
A TV broadcasting standard in which data such as text (e.g. subtitles, closed caption) or diagrams are transmitted within the TV broadcast signal.

9 **JPEG decoding:**
Refers to decoding that enables JPEG photographic data to be viewed on devices such as TVs

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Fujitsu Microelectronics Ltd. - Video Processing LSIs

About Fujitsu Microelectronics (FML)

Fujitsu Microelectronics Limited designs and manufactures semiconductors, providing highly reliable, optimal solutions and support to meet the varying needs of its customers. Products and services include ASICs/COT, ASSPs, power management ICs, and flash microcontrollers, with wide-ranging expertise focusing on imaging, wireless, automotive and security applications. Fujitsu Microelectronics also drives power efficiency and environmental initiatives. Headquartered in Tokyo, Fujitsu Microelectronics Limited was established as a subsidiary of Fujitsu Limited on March 21, 2008. Through its global sales and development network, with sites in Japan and throughout Asia, Europe, and the Americas, Fujitsu Microelectronics offers semiconductor solutions to the global marketplace. For more information: http://jp.fujitsu.com/group/fml/en/

Key Specifications of the MB86H70

Video	Profile	H. 264 high profile / Level 4.0 decoder MPEG-2 Video main profile / High Level decoder
	Resolution	Input: 480i, 480p, 576i, 576p, 720p, 1080i, 1080p Output: 1920 x 1080, 1366 x 768, 640 x 480
	Video Processing	Motion adaptive de-interlacing 3:2 / 2:2 Pull down Frame rate conversion Noise reduction Scalar: Enlarge /shrink Edge emphasis 3D-LUT color control
	Interface	10bit digital RGB input ITU-R BT. 656 video input Dual link 10bit LVDS video output
Audio	Format	MPEG-1/2 Layer I/II/III, MPEG-2/4 AAC LC, Dolby® Digital/Dolby® Digital Plus $^{(*)}$, HE-AAC
	Channels	5.1 Channels
	Interface	L/R serial, S/P DIF
	Others	Additional delay for lip synch
OSD	Layers	Video x 1, OSD x 3, Background x 1
	Size	OSD1/2 : 1920 x 1080, OSD3 : 480 x 1080
	Format	32bpp / 16bpp / 8bit CLUT
TS processing	Format	MPEG-2 TS
	Interface	2 input stream Built-in DVB descrambler
Internal CPU		ARM1176JZF-S^{TM} CPU @ 324MHz
DDR2 Memory Interface		2 x 16 bit width DDR2-SDRAM 667, Supports 256Mbit to 1Gbit SDRAM
Peripheral I/O		UPI, USB OTG Link, GPIO, Smart Card, I2C, UART, IR, PWM, 54MHz ADC, Interrupt, SPI
Input Clock Frequency		27MHz
Operating Frequency		Internal: 324MHz / DDR2 memory interface: 324MHz
Operating Voltage		1.4W (typ.)
Package		484 pin PBGA, 27mm^2(1.0-mm pitch)

* Dolby® Digital Plus: Fujitsu Microelectronics plans to support this audio format from November, 2008.