Press Release

[プレス リリース]

2013 年 12 月 10 日
富士通セミコンダクター株式会社

DDC™テクノロジとフラッシュメモリの混載に成功

～三重工場の低消費電力デバイス製造プロセスの適用範囲をさらに拡大～

富士通セミコンダクター株式会社 (注 1) は、当社三重工場の 55nm プロセスで DDC™テクノロジを適用したロジック回路とフラッシュメモリセルとを混載して製造する技術を世界で初めて開発しました。従来の CMOS 構造で超低消費電力を実現する DDC と不揮発性メモリであるフラッシュメモリとを同一チップに搭載したデバイスが可能になることで、IoT を初めとした様々な用途の製品への適用が期待されます。当社は本開発の成果について、12 月 9 日より 11 日まで米国ワシントン DC で開催中の IEEE International Electronic Device Meeting (IEDM) 2013 にて発表します。

各種の機器がインターネットにつながる「IoT (Internet of Things)」の発展に伴い、例えばワイヤレスセンサーネットワークに利用されるセンサー内蔵 LSI といったデバイスの需要が高まることが予想されています。このような用途においては、低電圧動作、低消費電力の重要性に加えて、センシングしたデータを保持するのに電力を必要としない不揮発性メモリの搭載が望まれています。

当社は、米国 SuVolta, Inc.からライセンスを受け共同開発した低消費電力化技術 DDC (Deeply Depleted Channel) テクノロジを世界で初めて実用化し、当社三重工場での生産をすでに開始しています。今回、この DDC トランジスタ搭載回路と、FLOTOX (FLOating gate Tunnel OXide) 構造のフラッシュメモリとを同一チップに搭載することが可能な製造技術を開発しました。

FLOTOX 構造のフラッシュメモリセル (図 1) では、浮遊ゲートに電子を注入する (書き込み) 、また浮遊ゲートから電子を抜き出す (消去) ことで、データの「0」と「1」を表現します。したがって、注入された電子が浮遊ゲートから漏れ出すと正しいデータが保持できなくなります。特に、書き込みと消去のサイクルを多数繰り返した後に漏れが発生する「シングルビット・チャージロス (SBCL) 」は本構造の信頼性にとって最大の課題でした。このような不良を防ぐためには、FLOTOX 構造を形成する「STI コーナーラウンディング」や「トンネル酸化膜形成」と呼ばれる工程において高温 (～1000℃程度) での処理が必須だと考えられてきました。

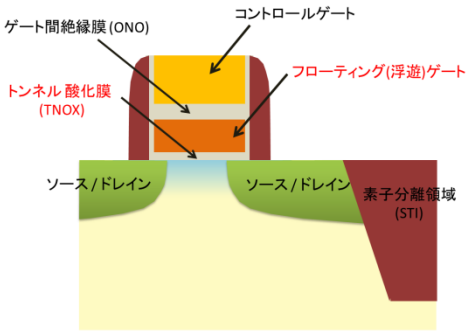

図 1. FLOTOX 構造の概要

一方、DDC トランジスタ (図 2) は、ゲート電極の下に「Depleted Layer」という、不純物を極低濃度に保った層を形成することがその特徴であり、このような層を形成し保持するためには、前述したような高温プロセスを使用することができない、という制約がありました。

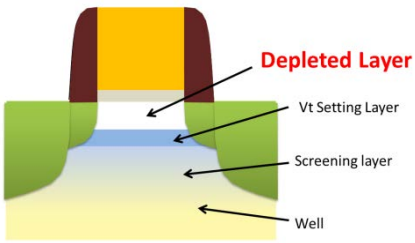

図 2. DDC の概要

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そこで、当社開発チームは低温プロセスのみで FLOTOX を形成することを目指しました。工程の一つ一つについて注意深く見直しを行い、チャネル領域およびソース・ドレイン電極部分の不純物濃度分布が最適となるよう調整した結果、DDC トランジスタに要求される特性は維持したまま、FLOTOX 構造を形成できる処理条件を見出すことに成功しました。この新しい条件で試作した評価用チップにより、フラッシュメモリ動作の初期特性を確認するとともに、書き込み・消去サイクル後の SBCL 不良の発生がなく、信頼性についても問題がないことが確認できました。

また、この最適化の過程において、SBCL が発生するメカニズムが、従来信じられていたトンネル酸化膜への電流ストレスではなく、ドレイン近傍で発生するホットホール(注 2)によって支配されている、という新たな知見を得ることができ、今後、製造プロセスのさらなる最適化へ寄与することが期待されています。

当社は今後も、機能・性能・コストを最適なバランスで実現する製造技術の開発を継続し、顧客製品の価値向上に貢献していきます。

なお、本件技術の詳細については、12 月 9 日から 11 日まで米国ワシントン DC で開催中の IEEE International Electron Devices Meeting (IEDM) 2013 において発表します。

【商標について】

記載されている製品名などの固有名詞は、各社の商標または登録商標です。

【添付資料】

IEEE International Electron Device Meeting (IEDM) 2013

・論文（英文）

【注釈】

注 1: 富士通セミコンダクター株式会社：
本社 神奈川県横浜市、代表取締役社長 岡田 晴基。

注 2: ホットホール：
高いエネルギーを持った正孔(ホール)。

【関連リンク】

http://jp.fujitsu.com/group/fsl/（富士通セミコンダクター）

【本件に関する 技術的なお問い合わせ先】

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Embedded FLOTOX Flash on Ultra-Low Power 55nm Logic DDC Platform

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Abstract

We have successfully embedded flash memory on an ultra-low power (<0.9V) 55nm Deeply Depleted Channel™ (DDC) platform. In spite of reduced thermal budget of DDC process, single-bit charge loss (SBCL) of flash after cycling can be optimized and is comparable to that of baseline embedded flash. We have also verified that improved variability and resultant ultra-low power digital performance of the DDC process is maintained in an embedded flash flow.

Introduction

The DDC transistor has been shown to achieve ultra-low voltage SRAM operation [1] and to improve digital and analog performance [2] by aggressive reduction in random dopant fluctuation (RDF) and improvement in device electrostatic performance.

It is strongly desired to embed non-volatile memories on the DDC platform to enable a wide range of ultra-low power applications such as smartcards and a variety of energy harvesting and sensor MCUs for Internet of Things (IoT) applications.

We have successfully embedded and characterized 1T NOR FLOTOX flash macro on DDC platform. The FLOTOX flash cell itself can be applied to other architectures such as 2T NOR flash suitable for ultra-low power applications [3-4].

DDC Structure and 1T NOR Flash Macro

Cross sectional DDC structure is shown in Fig.1. DDC process utilizes reduced thermal budget in order to suppress impurity diffusion into the undoped epitaxial channel layer.

Memory cell layout of 1T NOR FLOTOX flash macro used in this work is shown in Fig.2. The macro contains 512 word lines (WL) and 1024 bit lines (BL) resulting 512k cells.

Process Flow and Challenges

Fig. 3 compares the process flow for embedded flash on DDC platform with that for standard DDC and embedded flash on baseline platform. Modified steps for embedded flash on DDC platform are highlighted by yellow. Epitaxial layer is thickened to compensate for Si loss during additional oxidation steps for flash tunnel oxide (TNOX) and high voltage gate oxide (HVGOX). Temperatures for flash related steps are aggressively lowered. Channel and drain engineering for flash and HV transistors are carefully modified.

Fig. 4 shows cross-sectional TEM of fabricated flash cells on both baseline and DDC platforms. The cells are very similar with the exception of smaller STI corner rounding of flash on DDC platform.

Leakage current through TNOX and ONO with aggressively reduced thermal budget is very concerned to degrade flash data retention characteristics. Moreover, past literature [5-7] suggests that low temperature TNOX and reduced STI corner rounding degrade flash reliability, especially single bit charge loss (SBCL) after program & erase (P/E) cycling.

DDC Characteristics

Fig. 5 shows Ion-Ioff plots comparing performance of DDC transistors with and without embedded flash. Though there found slightly worse NMOS but slightly better PMOS with embedded flash, the differences are small enough to adjust.

Fig. 6 shows Pelgrom AVT values as a function of V_T. Pelgrom AVT values on an embedded flash DDC flow are comparable to those on a standard DDC flow and significantly better than those on a baseline 55nm flow.

The results validate that the additional thermal budget for the flash related steps could be enough reduced to suppress impurity diffusion from screen layer to un-doped epitaxial channel layer of DDC transistors.

High Voltage (10V) Transistors for Flash Control

Fig. 7 shows source drain (SD) breakdown voltage (BV) of high voltage (HV) transistors as a function of V_T. Even with the aggressive reduction in thermal budget, both NMOS and PMOS transistors show BV in excess of 10V. If HV NMOS and PMOS are used symmetrically for flash control, the peripheral circuit can apply 20V to the FLOTOX flash cell, making it applicable not only for 1T NOR but also for other architectures of FLOTOX cell such as 2T NOR.

The results validate that the aggressively reduced thermal budget for flash related steps is well acceptable for HV transistors.

Fundamental Characteristics of Single Flash Cell

Table 1 summarizes the 4 different process conditions for flash cells on DDC platform – 2 levels of SD implant energy and 3 levels of V_T doses for lower SD implant energy.

Fig. 8 shows fundamental characteristics of single flash cell monitors, initial V_T (Vti), program V_T (Vtp), Vtp after accelerated drain disturb (DD), erase V_T (Vte) and Vte after accelerated gate disturb (GD). Flash cells on DDC platform show a clear Vtp shift by the accelerated DD.

Other characteristics are comparable to baseline though Vti of some DDC splits are different.

Fig. 9 shows bias conditions for the accelerated DD. There are 2 possible models for the Vtp shift by DD. One is electron F-N tunneling from floating gate (FG) to drain through TNOX and the other is hot hole injection from drain edge to FG. The hot hole is generated by impact ionization at drain edge.

Fig. 10 shows Vtp shift by DD as a function of Vti. Vtp shift increases with increasing V_T dose and decreases with increasing SD implant energy. It is clear that the Vtp shift is caused by hot hole injection and not by intrinsic TNOX tunneling, since impact ionization during DD is increased with increasing V_T dose and decreased with increasing SD implant energy but F-N tunneling is not so much affected by the splits.

Fig. 11 shows Vtp shift by DD as a function of disturb time with normal program bias. If disturb time is less than 2ms, Vtp shift is negligibly small. Since programming for each cell is completed by 1-2 of 1us pulses, DD time for the worst cell on a BL is about 1ms and less than 2ms. These suggest that the observed Vtp shift by DD does not degrade Vtp distribution within in a flash array. But past literature [6] suggests that the degraded DD may degrade SBCL after cycling.

Initial Characteristics of 512k Flash Macro

Based on the single cell results and the suggestion of past literature [6] especially about impact of DD on SBCL, we compared DDC-1 and DDC-2 with baseline. DDC-2 has higher flash SD implant energy and smaller DD compared to DDC-1.

Fig. 12 shows V_T distributions at initial, program and erase state of 70 macros for each condition. Though initial V_T (Vti) is a little different from each other, program and erase V_T (Vtp and Vte) are comparable to others because of verify operation implemented in the macro. Nice Vtp distributions for any of the conditions validate small enough impact of DD on array programming as expected from Fig. 11.

Fig. 13 shows Vtp distributions before and after 250C bake. No severe Vtp shift was seen for any of the conditions which validating leakage current through TNOX and ONO with the aggressively reduced thermal budget is not an issue.

These results validate that initial characteristics of the macro with the aggressively reduced thermal budget are well acceptable and healthy.

Characteristics of 512k Flash Macro after Cycling

Since flash reliability after cycling especially SBCL is a big concern, we cycled 20 dice for each condition up to 1k times. 10 dice for each were used for Vte shift and another 10 dice for Vtp shift after cycling and bake. We lowered the bake temperature down to 150C and elongated the bake time up to 1kH to detect SBCL definitely.

Fig. 14 shows minimum Vtp and maximum Vte in an 512k array as a function of cycling. We applied V_T verify operation for the normal cycling but did not apply it for program and erase operation just before Vtp and Vte measurement after predetermined cycling. Though flash cells on DDC platform showed a little faster window narrowing by charge trapping than flash cells on baseline, it is well acceptable.

Fig. 15 shows Vtp and Vte distributions after 1k cycling and 150C 0-1kH bake. We plotted all cells on 10 dice of 512k macro at once in a graph to make SBCL more clearly visible. No Vte shift was seen on any of the conditions. On the other hand, Vtp shift of SBCL was seen on DDC-1 but not seen on both DDC-2 and baseline. Since differences between DDC-1 & DDC-2 are flash Vt and SD implant conditions and resultant drain disturb (DD) amount, the results mean that (1) SBCL found on DDC-1 is dominated by hot hole injection during DD and can be optimized as DDC-2, (2) very low temperature TNOX and small STI rounding adopted for both DDC-1 and DDC-2 are not issues.

All of the results shown above validate healthy and well acceptable initial and post-cycling characteristics of DDC-2. Moreover, DDC-2 can be improved more because there is room to reduce V_T dose further and match DD to the baseline as seen in Figure 10.

Conclusions

Embedded flash memory has been successfully integrated on to an ultra-low power 55nm DDC platform. This should pave the way for a variety of low power MCU based applications.

This work on flash added new knowledge to the past literatures, (1) flash single bit charge loss (SBCL) is much dominated by hot hole injection during drain disturb (DD) rather than F-N stressing of TNOX and (2) very low temperature TNOX, ONO and STI schemes are not issues.

Acknowledgements

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[4] Sung-Rae Kim et al., 'High performance 65nm 2T-embedded Flash memory for high reliability SOC applications', *IEEE IMW 2010*

[5] G. Ghidini, 'Charge-related phenomena and reliability of non-volatile memories', *Microelectronics Reliability vol.52, 1876(2012)*

[6] A. Chimenton et al., 'Drain-accelerated degradation of tunnel oxides in Flash memories' , *IEDM 2002, pp167-170*

[7] Ming-Yi Lee et al., 'Anomalous Single Bit Retention Induced by Asymmetric STI-Corner-Thinning for Floating Gate Flash Memories', *IEEE IPFA 2012*

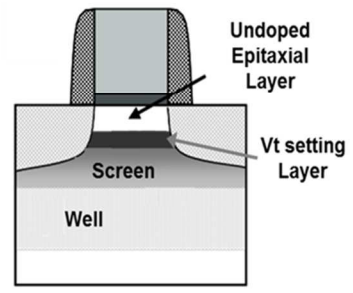

Fig.1 Structure of DDC transistor

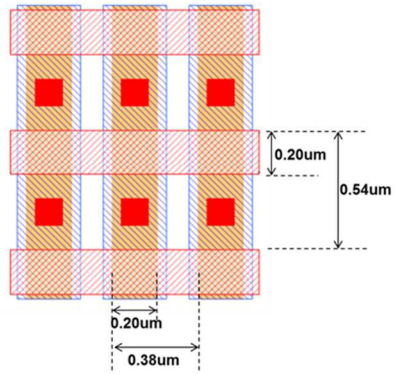

Fig.2 FLOTOX flash cell layout

	DDC	flash on BL	flash on DDC
DDC implant	POR	-	POR
Blanket epi	25nm	-	35nm
STI	LT	HT	LT
Flash TN-OX, FG & ONO	-	HT	LT
HV implant	-	POR	modify
MV implant	POR	POR	POR
HV-GOX	-	HT	LT
MV-GOX	LT	HT	LT
DDC-GOX	LT	HT	LT
Gate poly	POR	POR	POR
Flash CG	-	POR	POR
Flash SD	-	POR	modify
Flash SW-OX	-	HT	LT
HV/MV/DDC Gate	POR	POR	POR
HV LDD	-	POR	modify
MV LDD	POR	POR	POR
DDC LDD	POR	-	POR
SW	POR	POR	POR
SD	POR	POR	POR
Silicide	POR	POR	POR
BEOL	POR	POR	POR

** HV:10V for flash control, MV: 3.3V for I/O*

Fig.3 Process flow of DDC and embedded flash

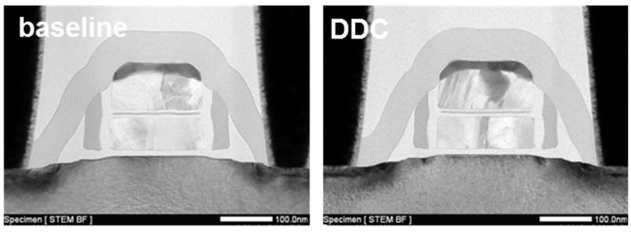

Fig.4: a) X-TEM of flash parallel to BL on baseline & DDC

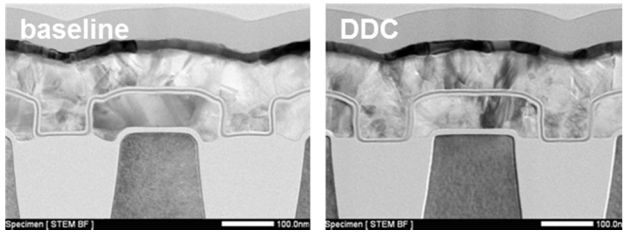

Fig.4: b) XTEM of flash parallel to WL on baseline & DDC

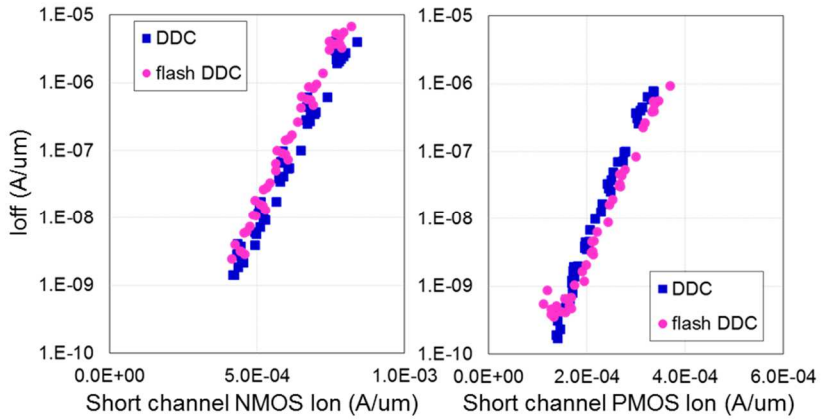

Fig.5: a) Ion/Ioff plot for short channel NMOS b) Ion/Ioff plot for short channel PMOS

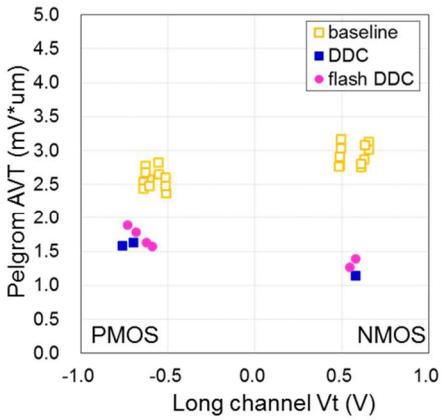

Fig.6: Pelgrom AVT as a function of long channel V_T

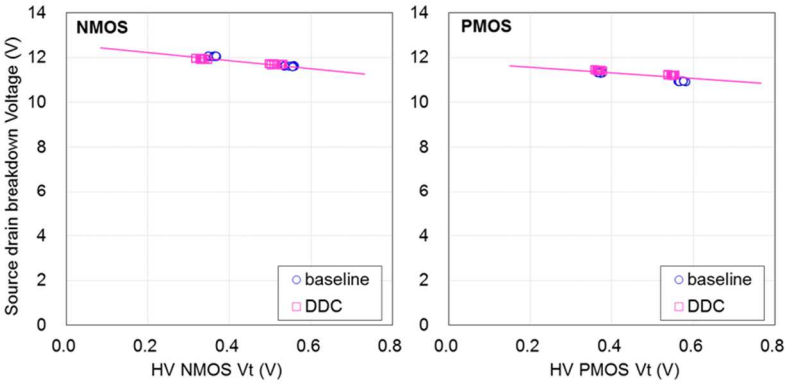

Fig.7: a) BV of HV NMOS b) BV of HV PMOS

Table 1: conditions for flash evaluation

	Vt implant	SD implant
baseline	POR	POR
DDC-1+	highest dose	POR
DDC-1	higher dose	POR
DDC-1-	lower dose	POR
DDC-2	lower energy	higher energy

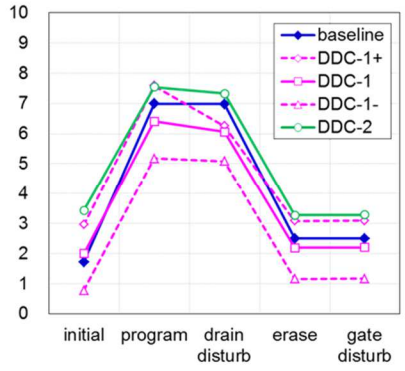

Fig.8: Fundamental flash characteristics

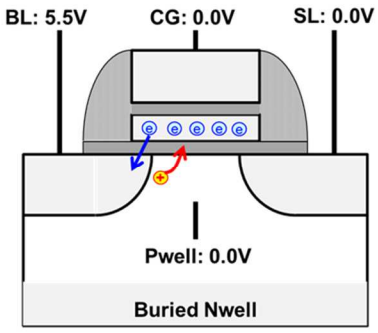

Fig.9: Bias condition of DD

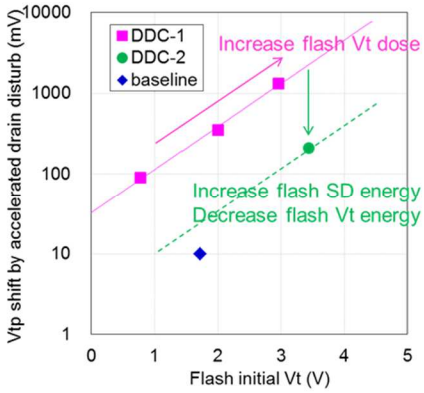

Fig10: dependence of Vtp shift by DD on Vti

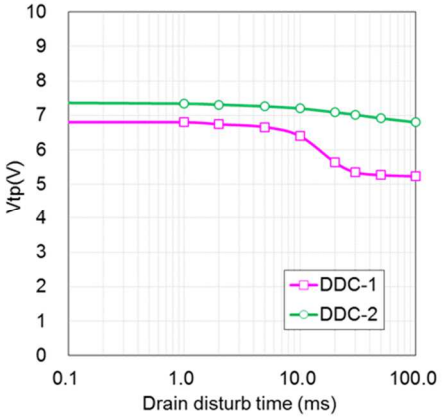

Fig.11: Dependence of Vtp shift on DD time

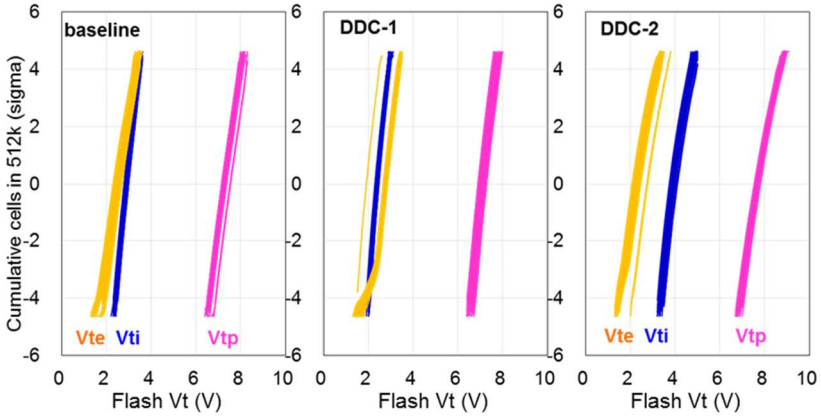

Fig.12: Distribution of UV, Vtp & Vte in 512k* 70 dice

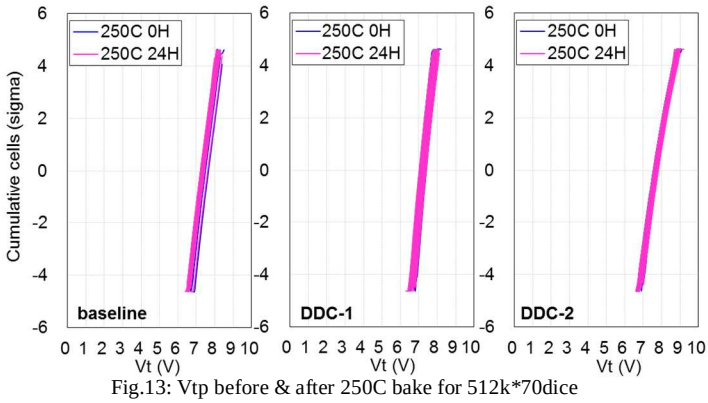

Fig.13: Vtp before & after 250C bake for 512k*70dice

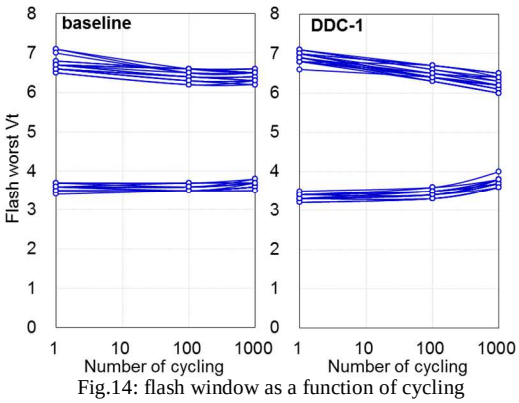

Fig.14: flash window as a function of cycling

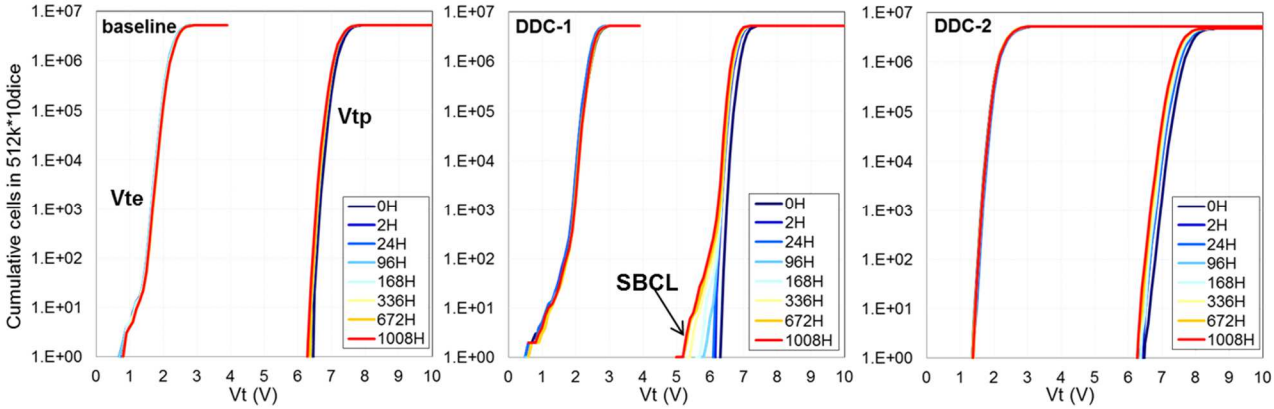

Fig.15: Vte & Vtp distribution after 1k cycling & 150C bake

Embedded FLOTOX Flash on Ultra-Low Power 55nm Logic DDC Platform

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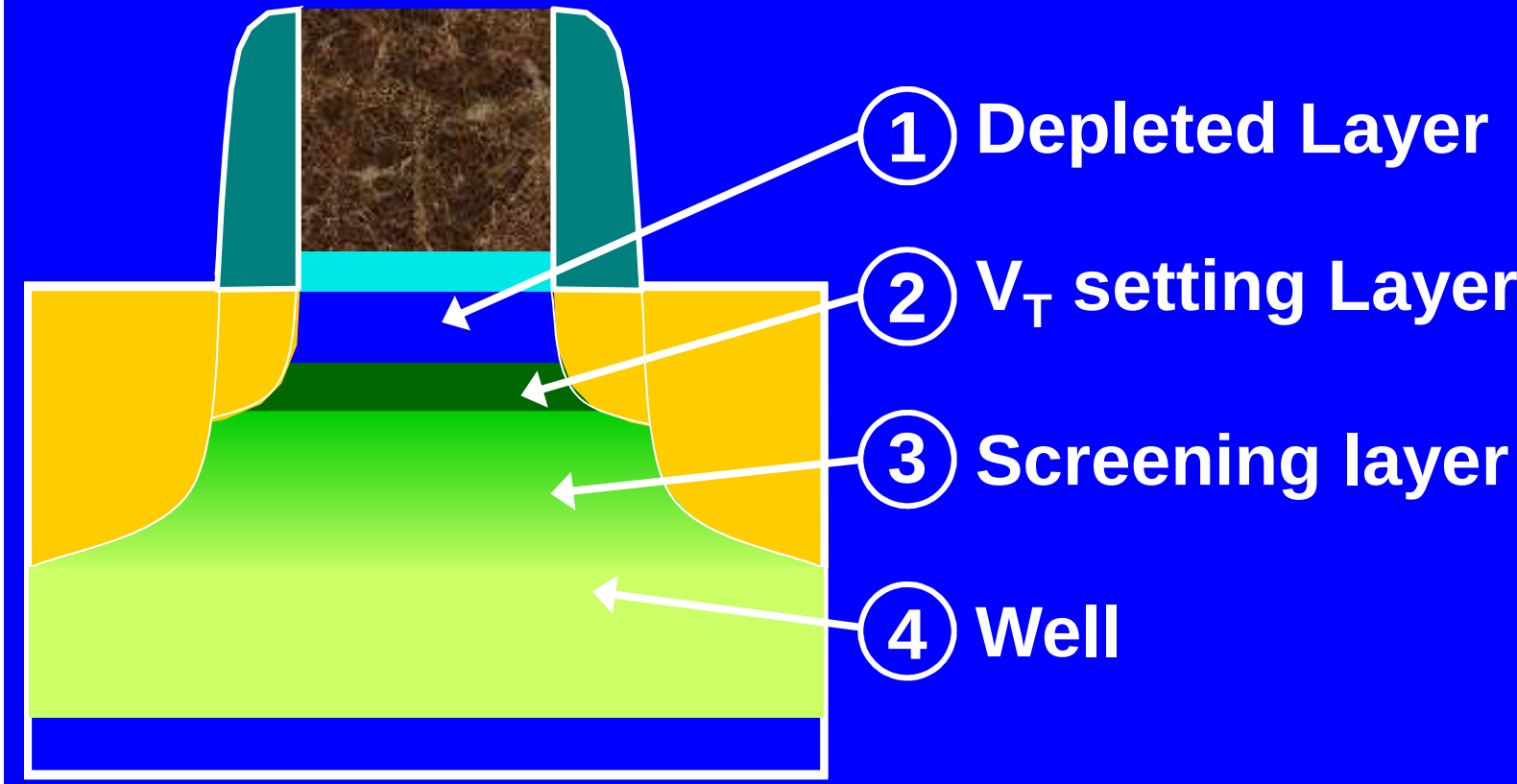
Outline

- Introduction
- Process Flow, Structures and Challenges
- Logic transistor characteristics
  - DDC transistors for logic circuits
  - HV transistors for flash control
- Results on Flash
  - Overall characteristics of single bit cell
  - Initial characteristics of 512k macro
  - Characteristics of macro after cycling
- Summary

Introduction

Deeply Depleted Channel ™ (DDC) Transistor



DDC is promising for ultra-low-power and ultra-low-voltage applications.

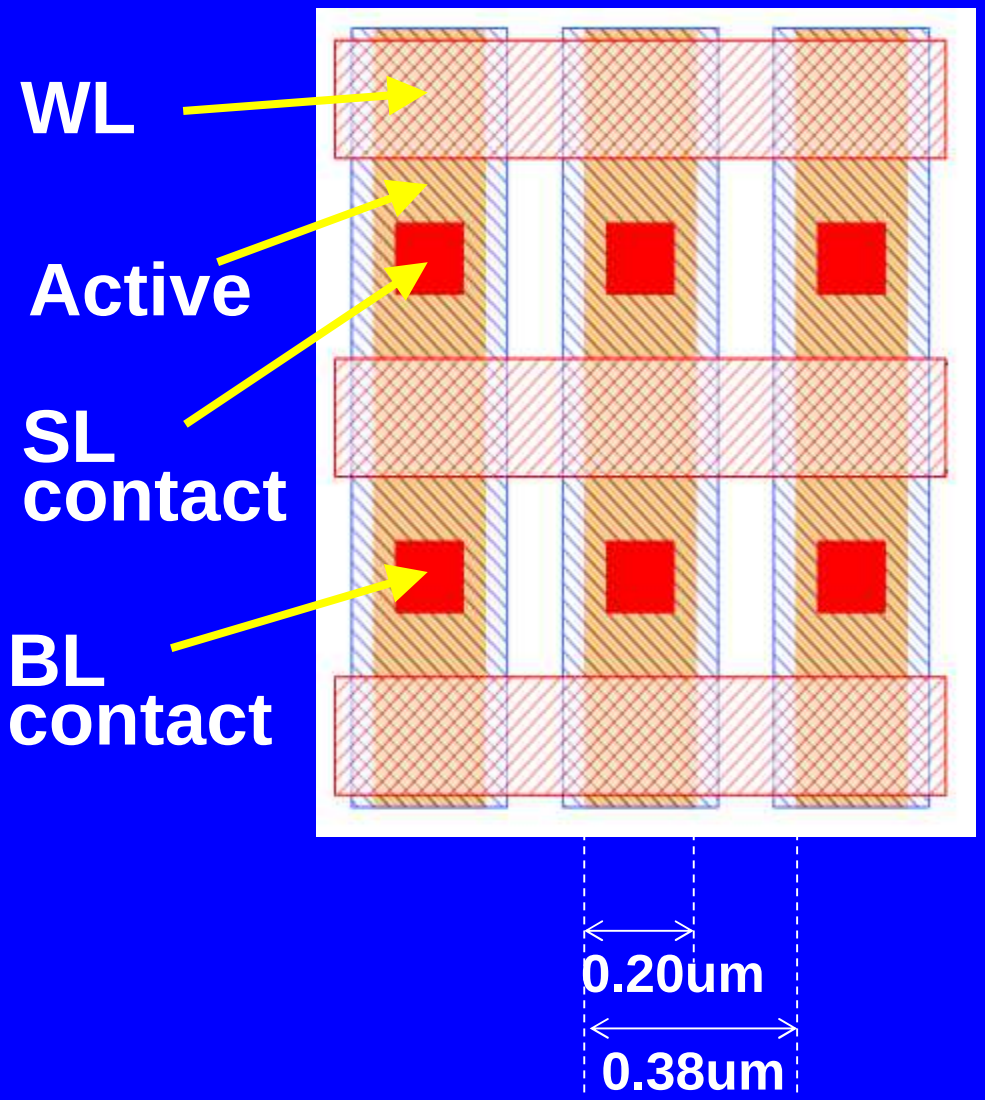
Introduction (Cont'd)

Low voltage and Low power sensor MCUs are strongly demanded for IoT.

[Source :http://jp.fujitsu.com/group/fsl/en/release/20130422.html]

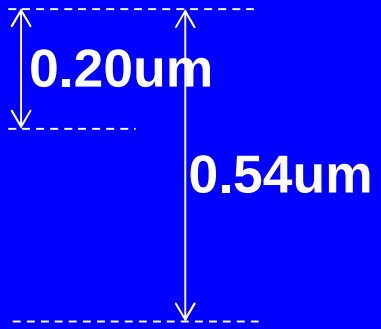
MCUs desires non-volatile memories on Ultra Low power Logic (= DDC transistor)

1T NOR FLOTOX flash cell layout



Cell size: 0.2052um^2

512k cells
(512WL*1024BL)

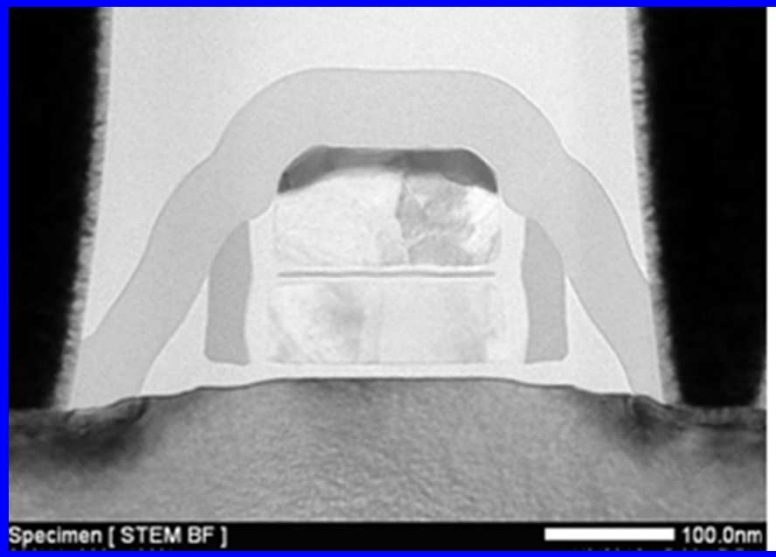


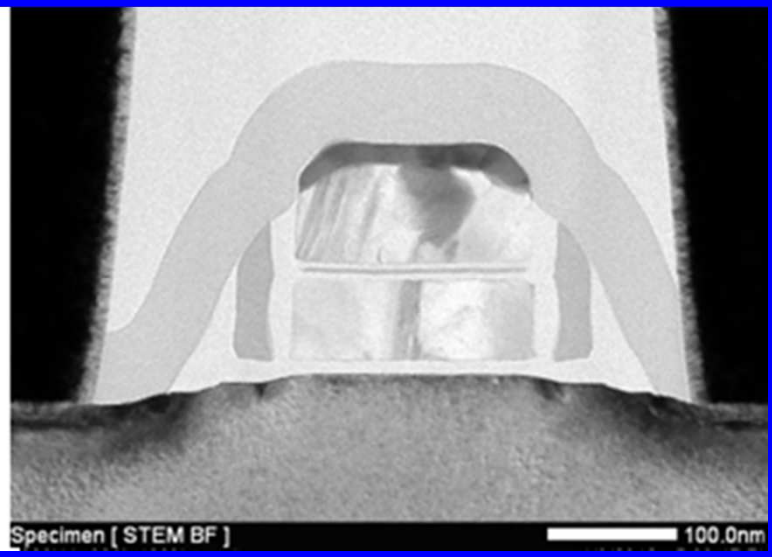
Process flow

Modules	Steps	BL	DDC	Flash on BL	Flash on DDC
DDC channel	DDC implant	-	POR	-	POR
	Blanket epi	-	25nm	-	35nm
STI	STI	HT	LT	HT	LT
Flash FG	Flash TN-OX, FG & ONO	-	-	HT	LT
Logic gate	HV implant	-	-	POR	modify
	MV implant	POR	POR	POR	POR
	HV-GOX	-	-	HT	LT
	MV-GOX	HT	LT	HT	LT
	DDC-GOX	HT	LT	HT	LT
	Gate poly	POR	POR	POR	POR
Flash Tr	Flash CG	-	-	POR	POR
	Flash SD	-	-	POR	modify
	Flash SW-OX	-	-	HT	LT
Logic Tr	HV/MV/DDC Gate	POR	POR	POR	POR
	HV LDD	-	-	POR	modify
	MV LDD	POR	POR	POR	POR
	LV LDD	POR	POR	POR	POR
	SW	POR	POR	POR	POR
	SD	POR	POR	POR	POR
	Silicide	POR	POR	POR	POR
BEOL	BEOL	POR	POR	POR	POR

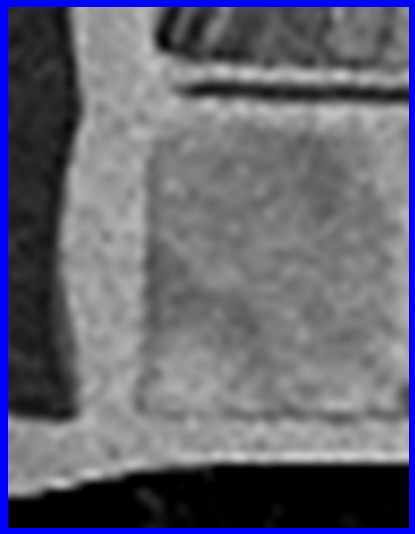
** HV:10V for flash control, MV: 3.3V for I/O*

TEM of flash cells Parallel to BL



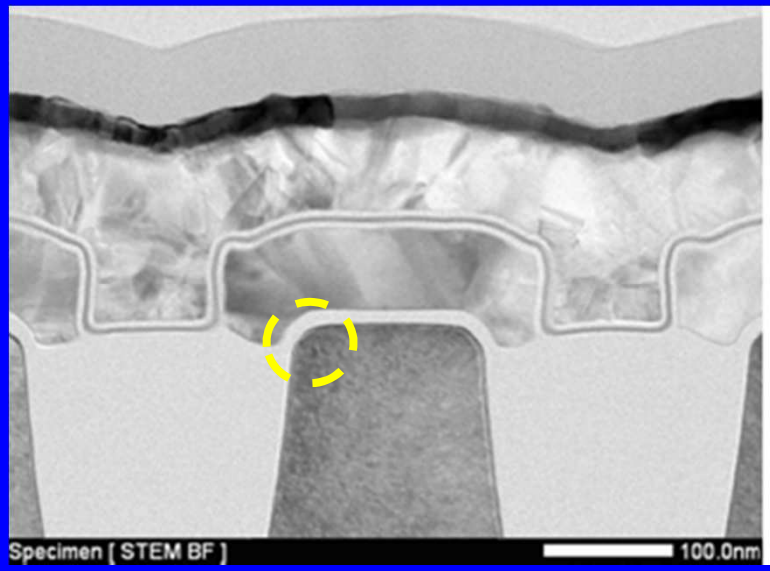


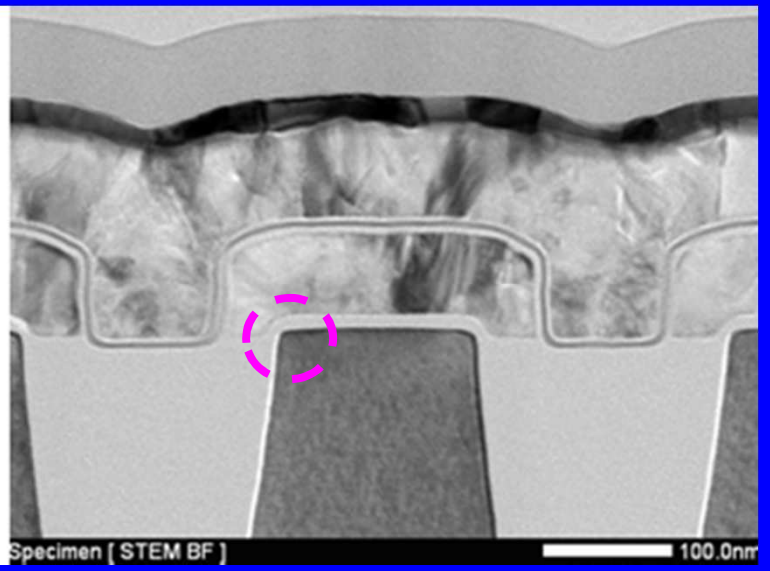
Flash on baseline

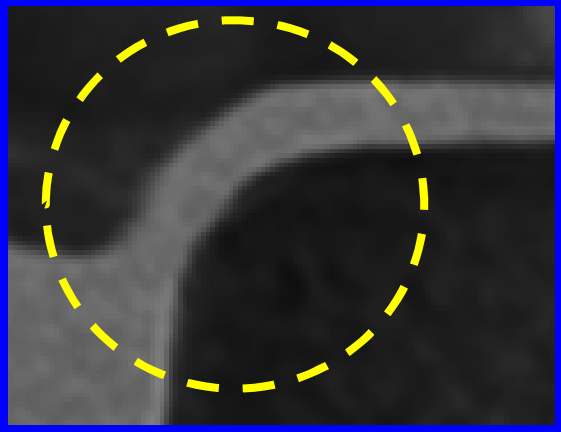


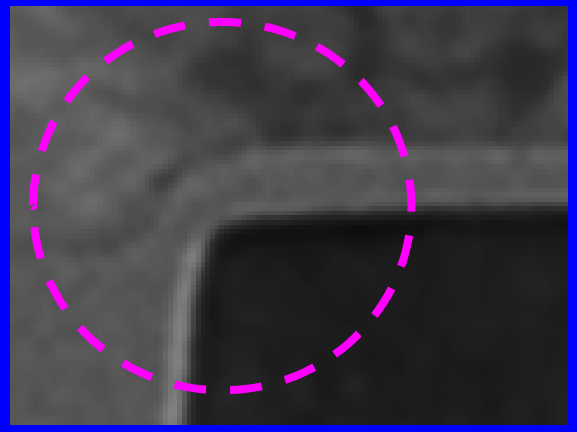
Flash on DDC

TEM of flash cells Parallel to WL







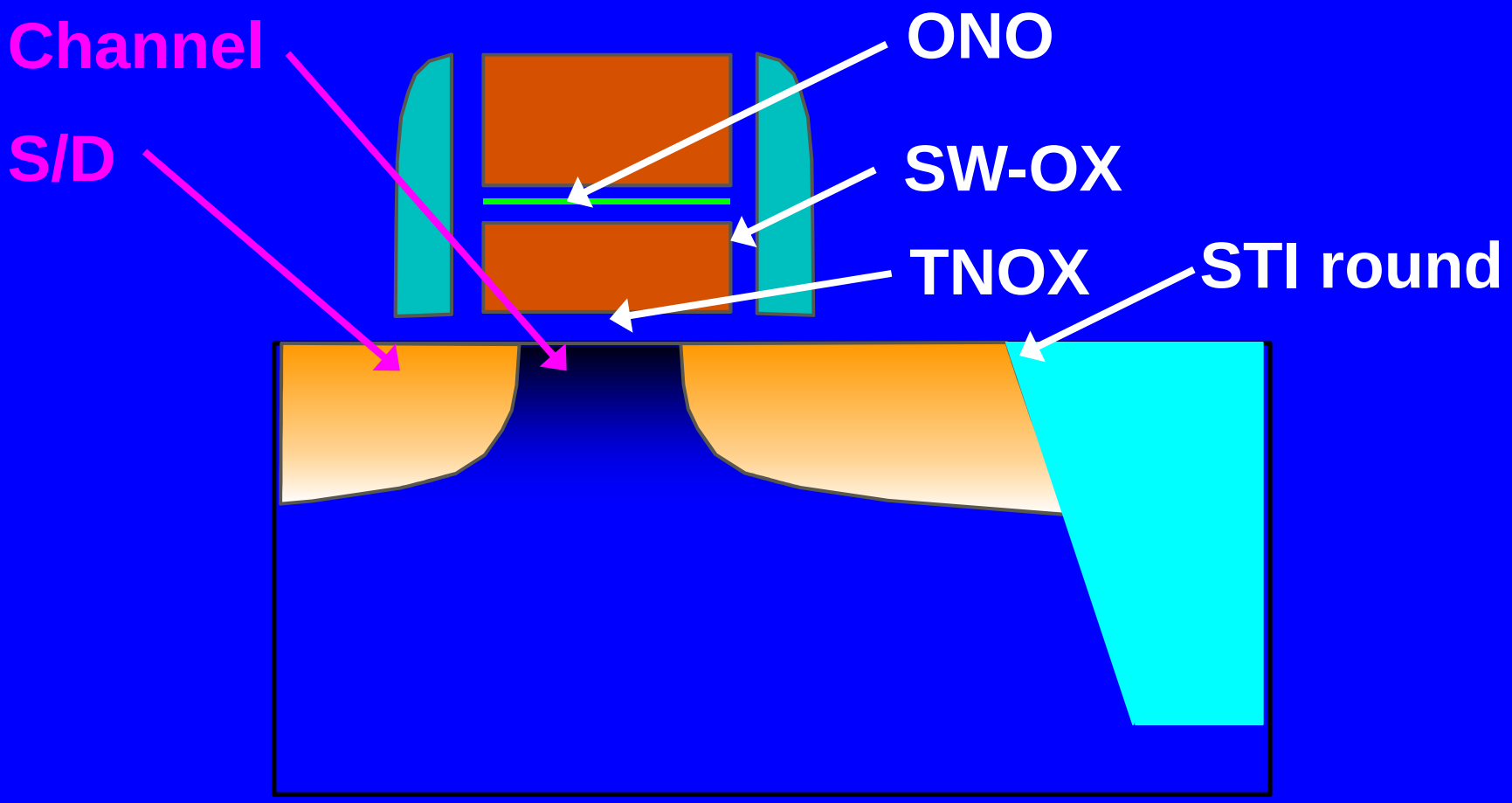


Flash on baseline

Flash on DDC

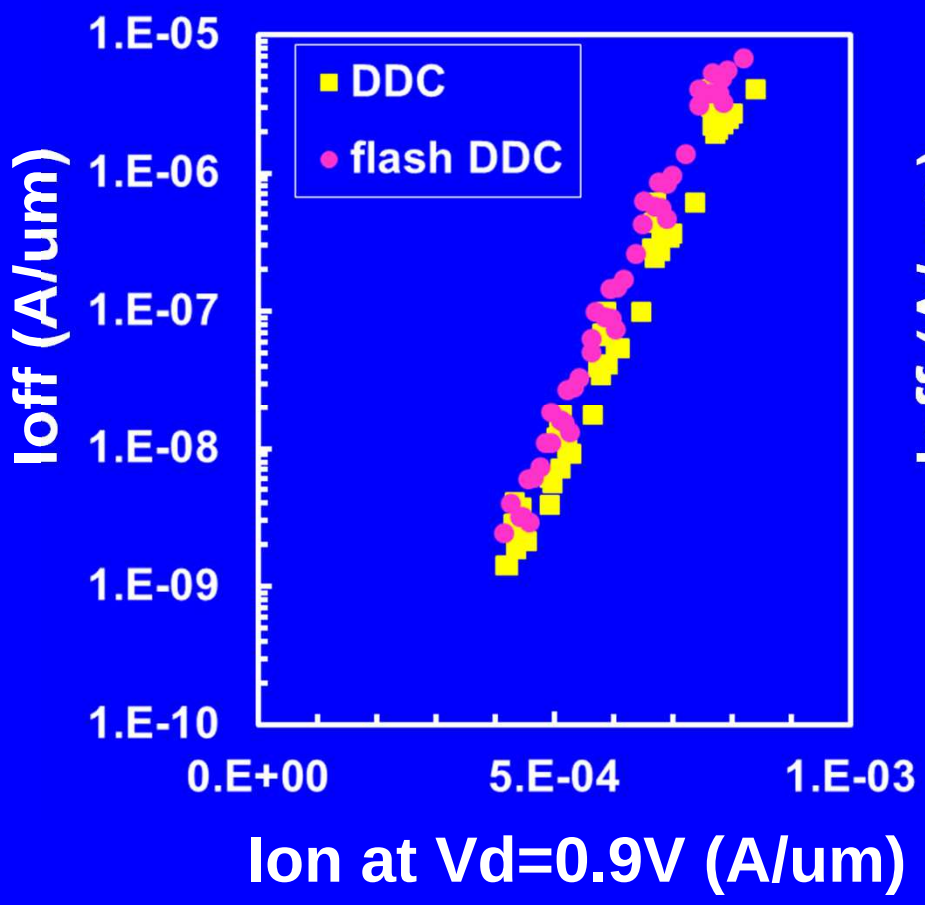
Challenges

- Low Temperature TNOX, ONO, STI, SW
- Channel and S/D engineering for flash and HV
- Impact of additional thermal budget on DDC

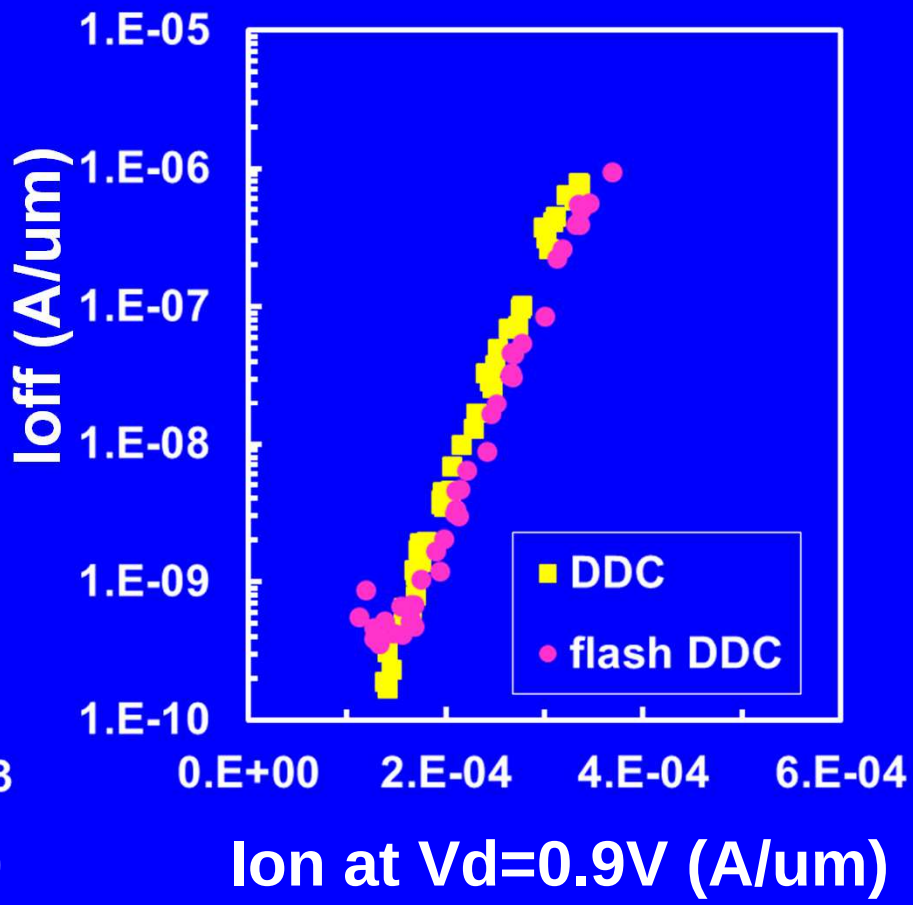


Performance of DDC transistors

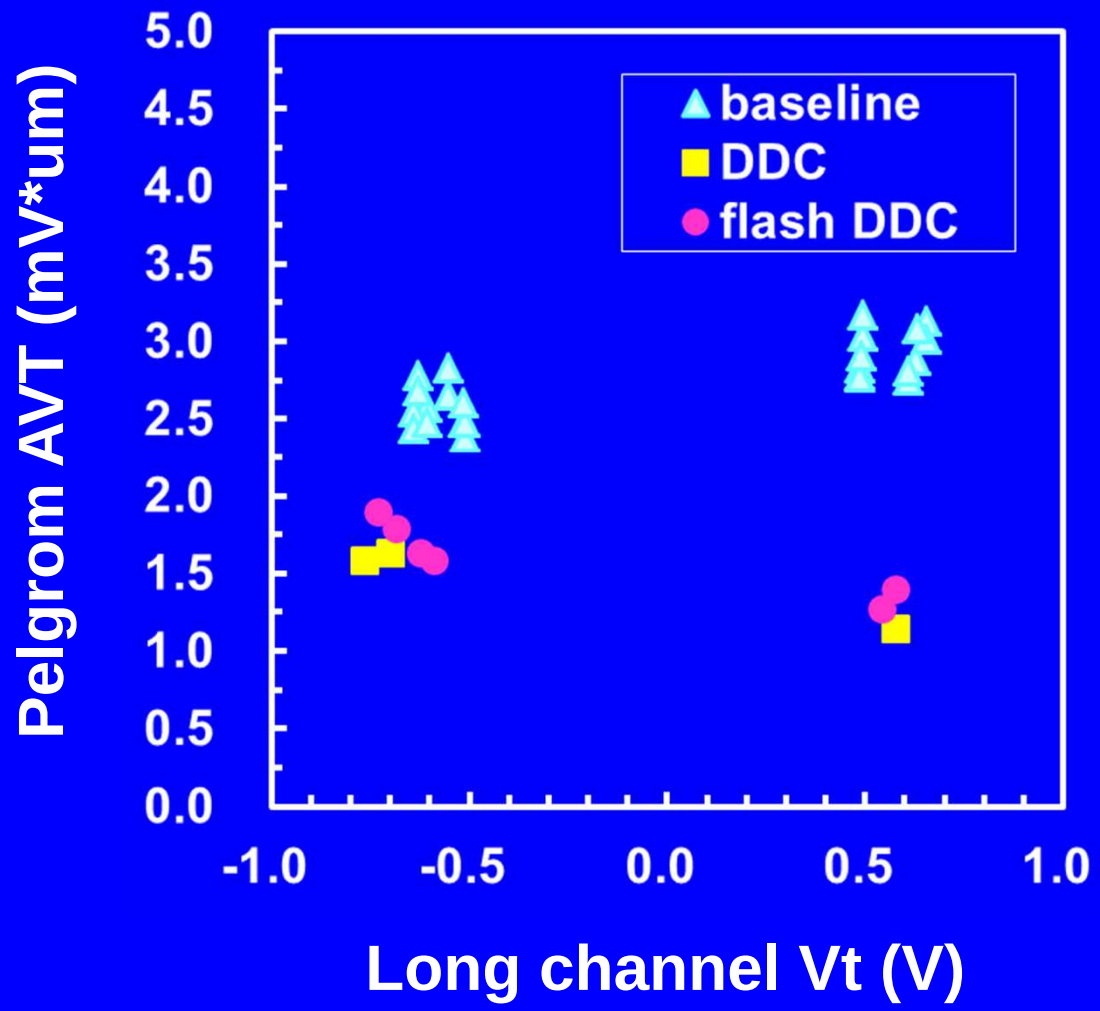
NMOS



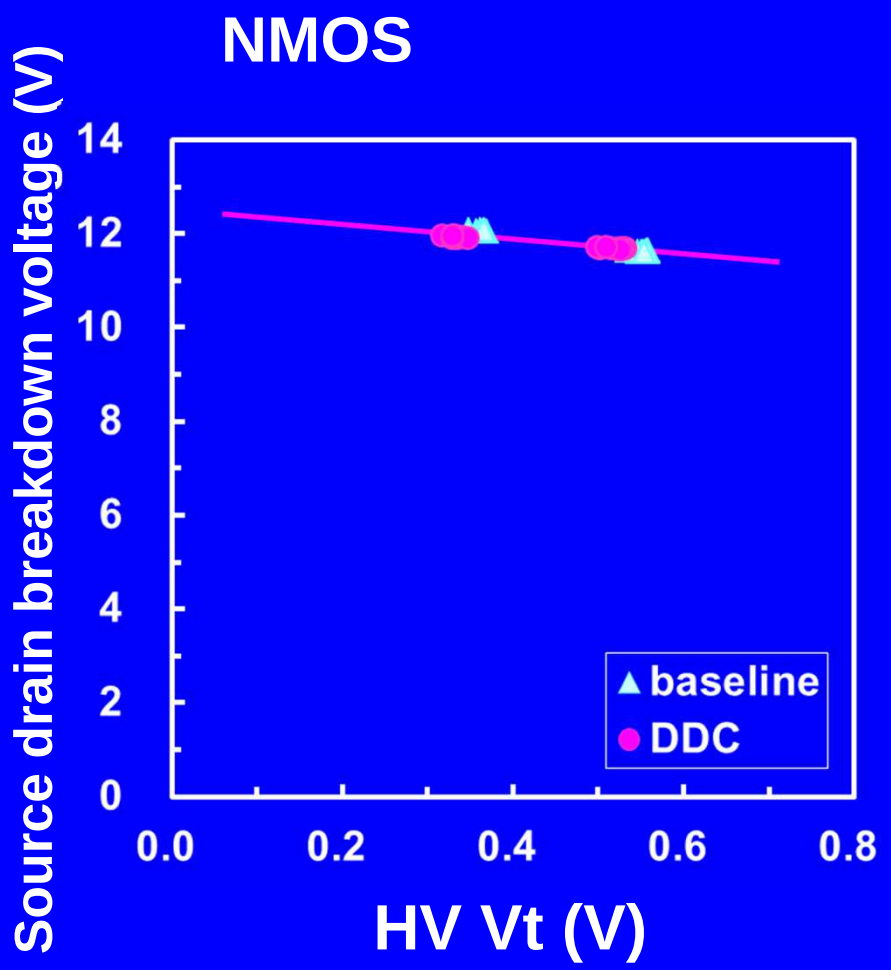
PMOS

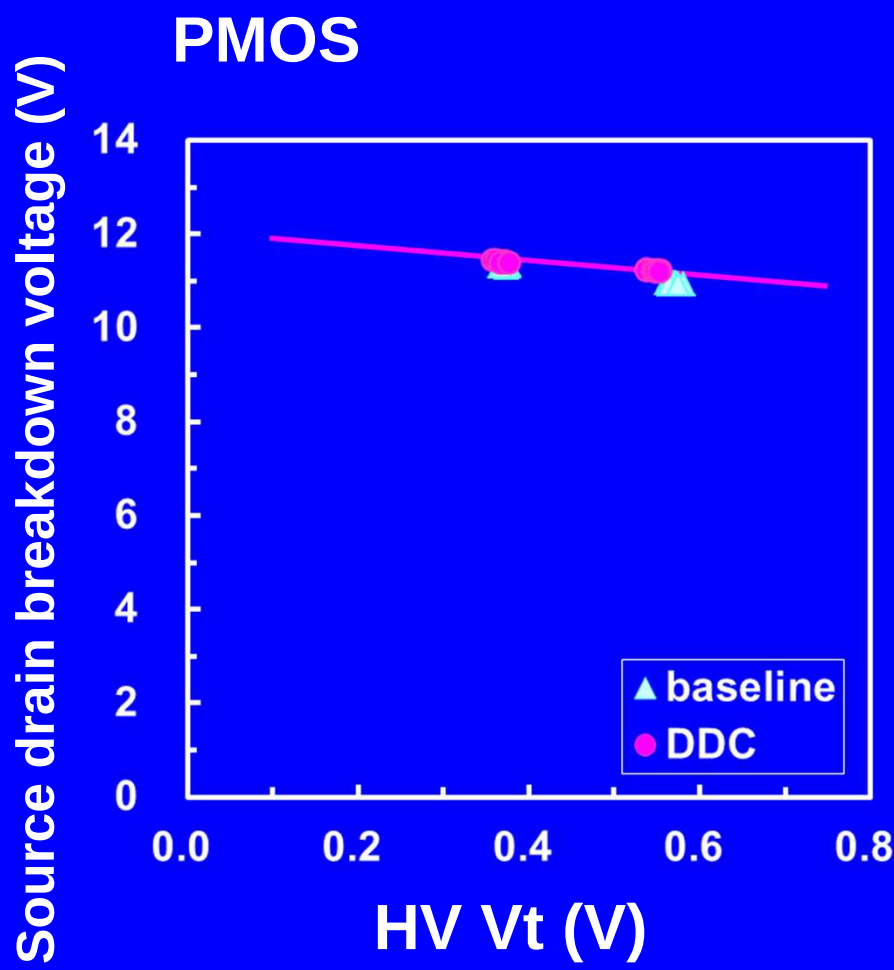


AVt values for DDC transistors



BV of high voltage transistors

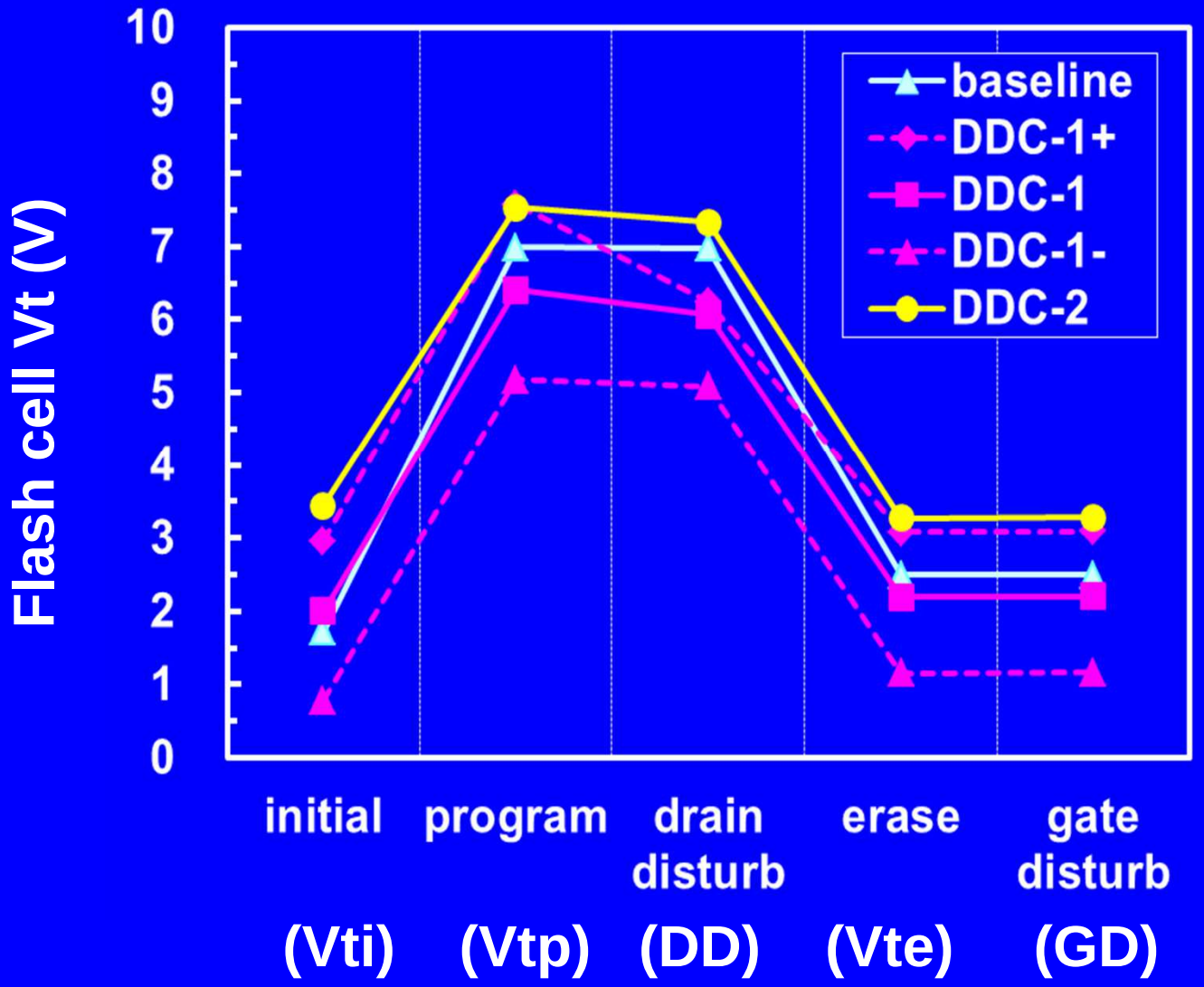




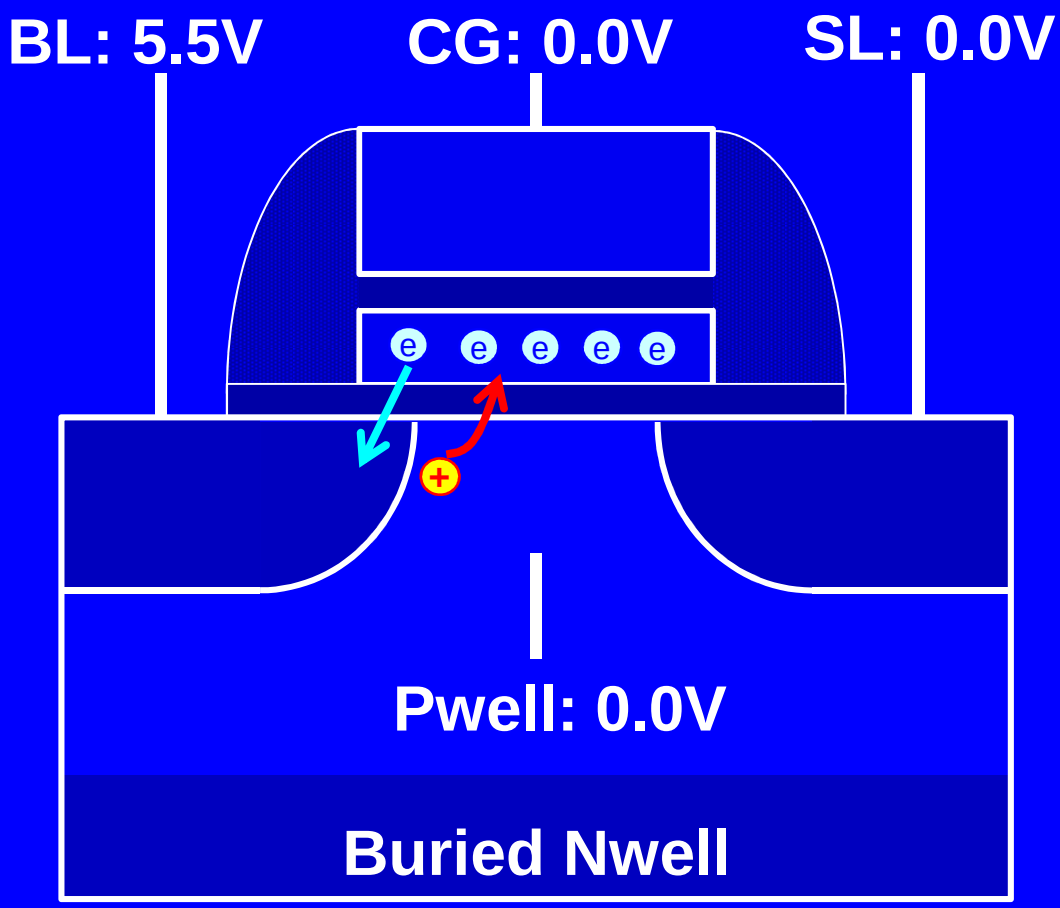
Splits for flash cells evaluation

	Vt implant	SD implant
▲ baseline	POR	POR
◆ DDC-1+	highest dose	POR
■ DDC-1	higher dose	POR
▲ DDC-1-	lower dose	POR
● DDC-2	lower energy	higher energy

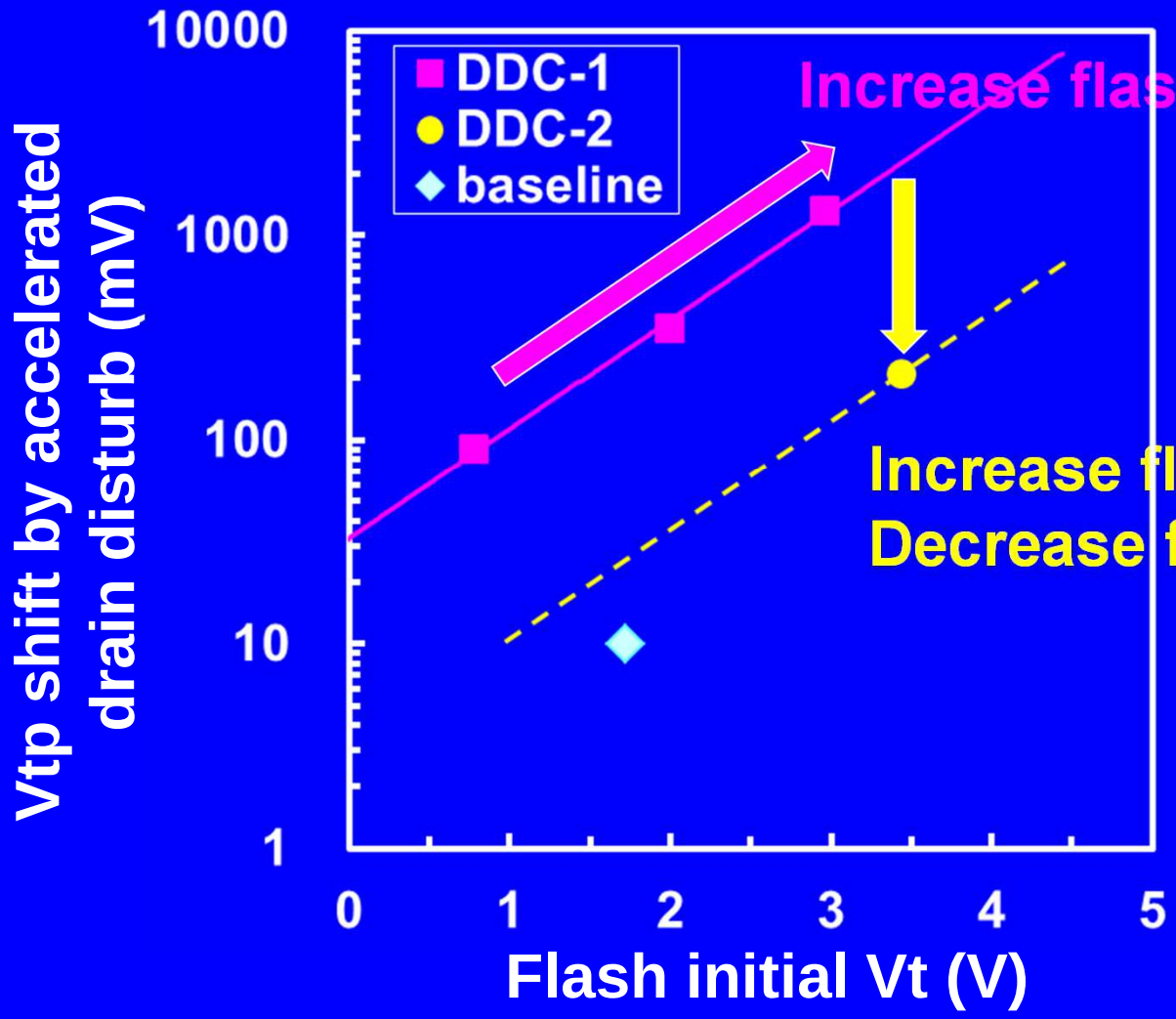
Characteristics of single flash cell



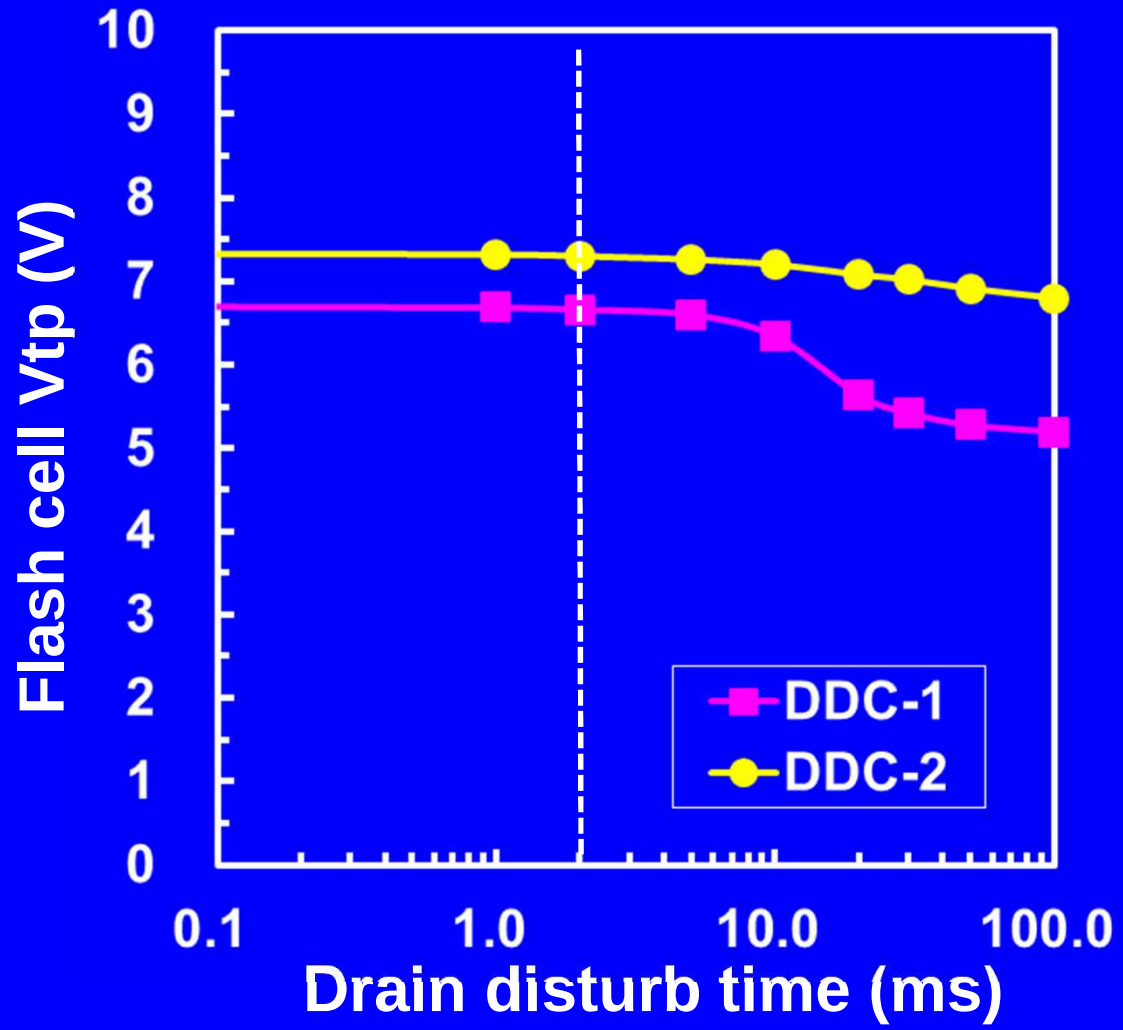
Possible causes of Vtp shift by DD



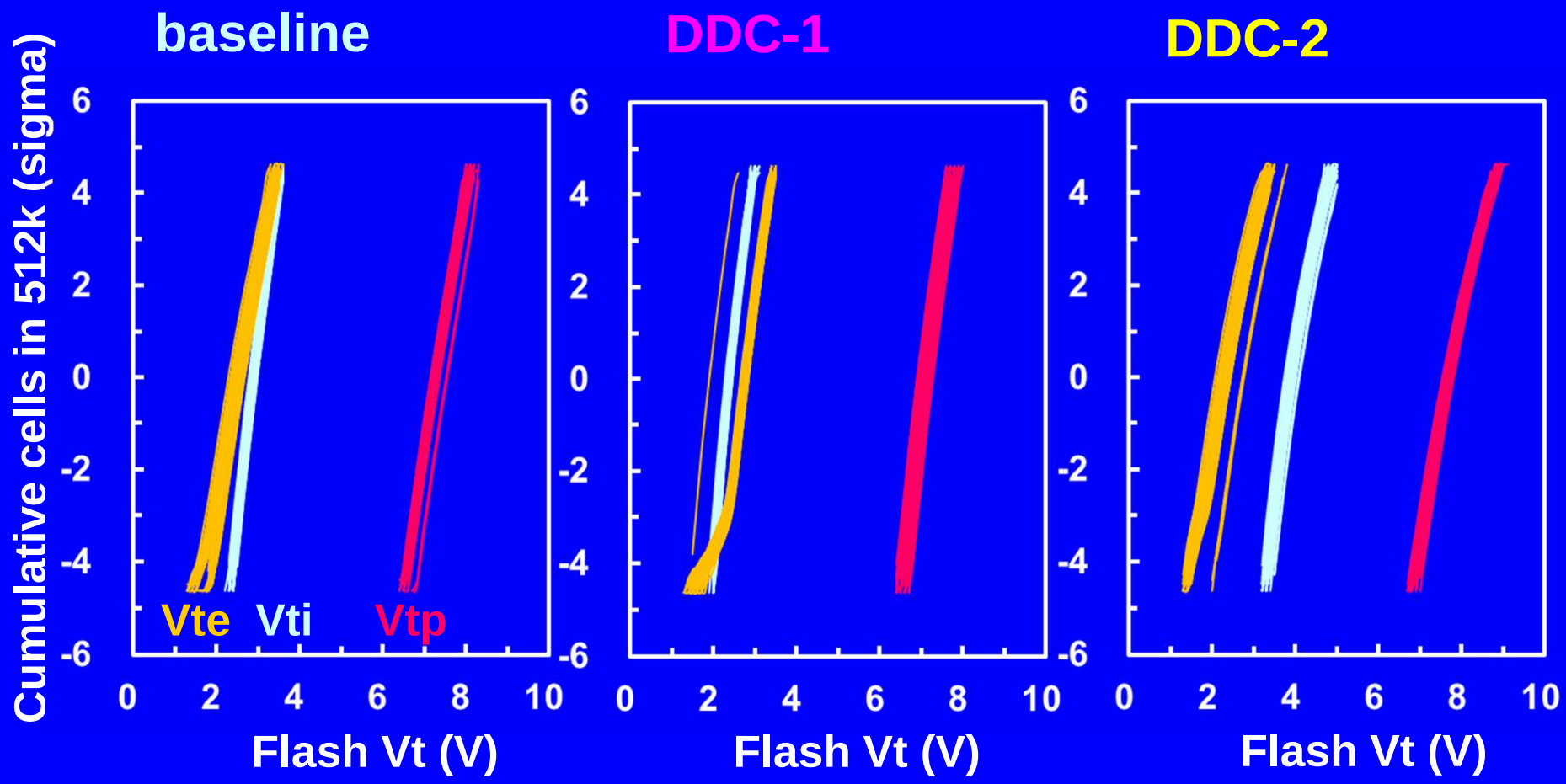
Vtp shift by DD as a function of Vti



Vtp shift as a function of DD time

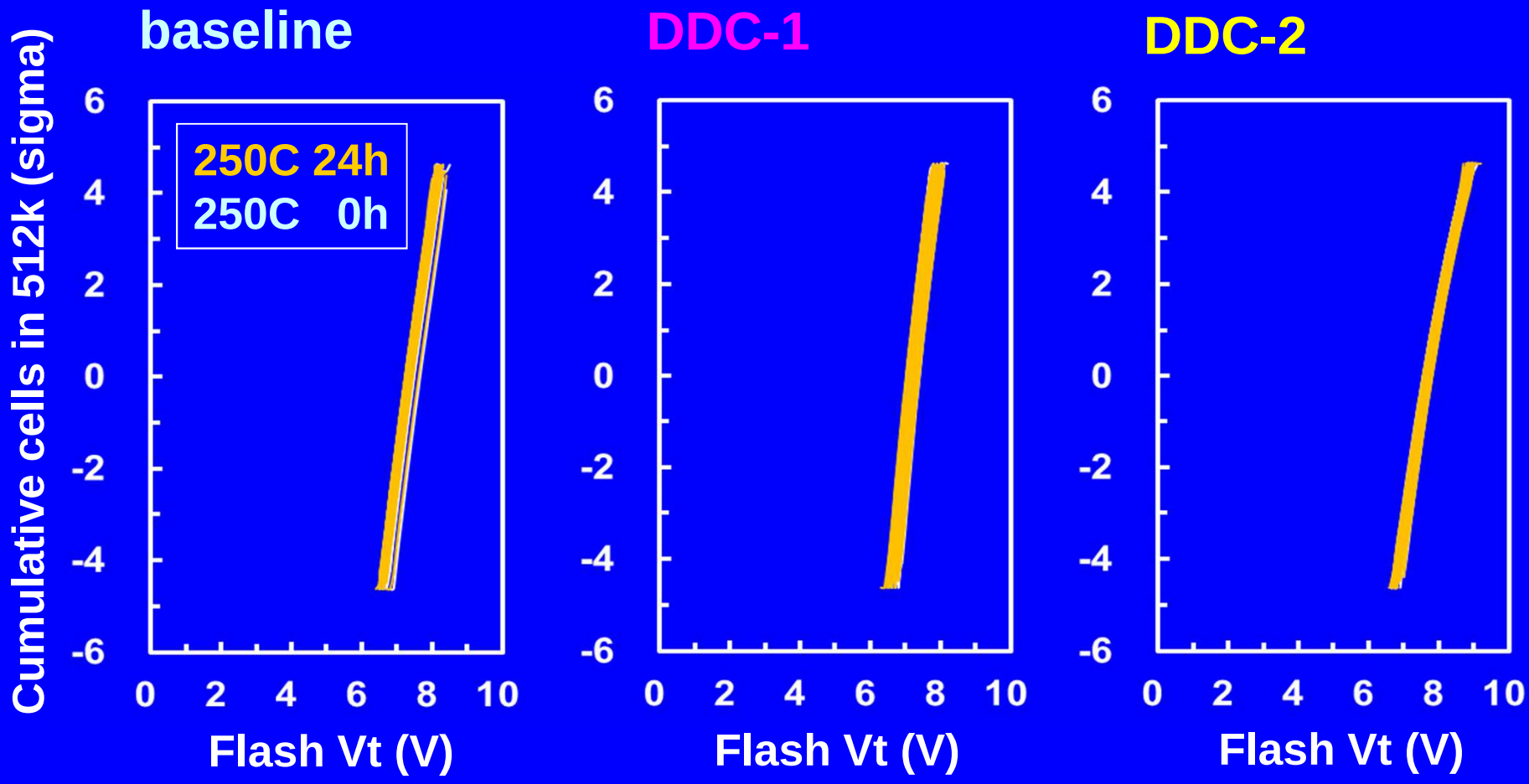


Vti, Vtp and Vte of 512k flash macro



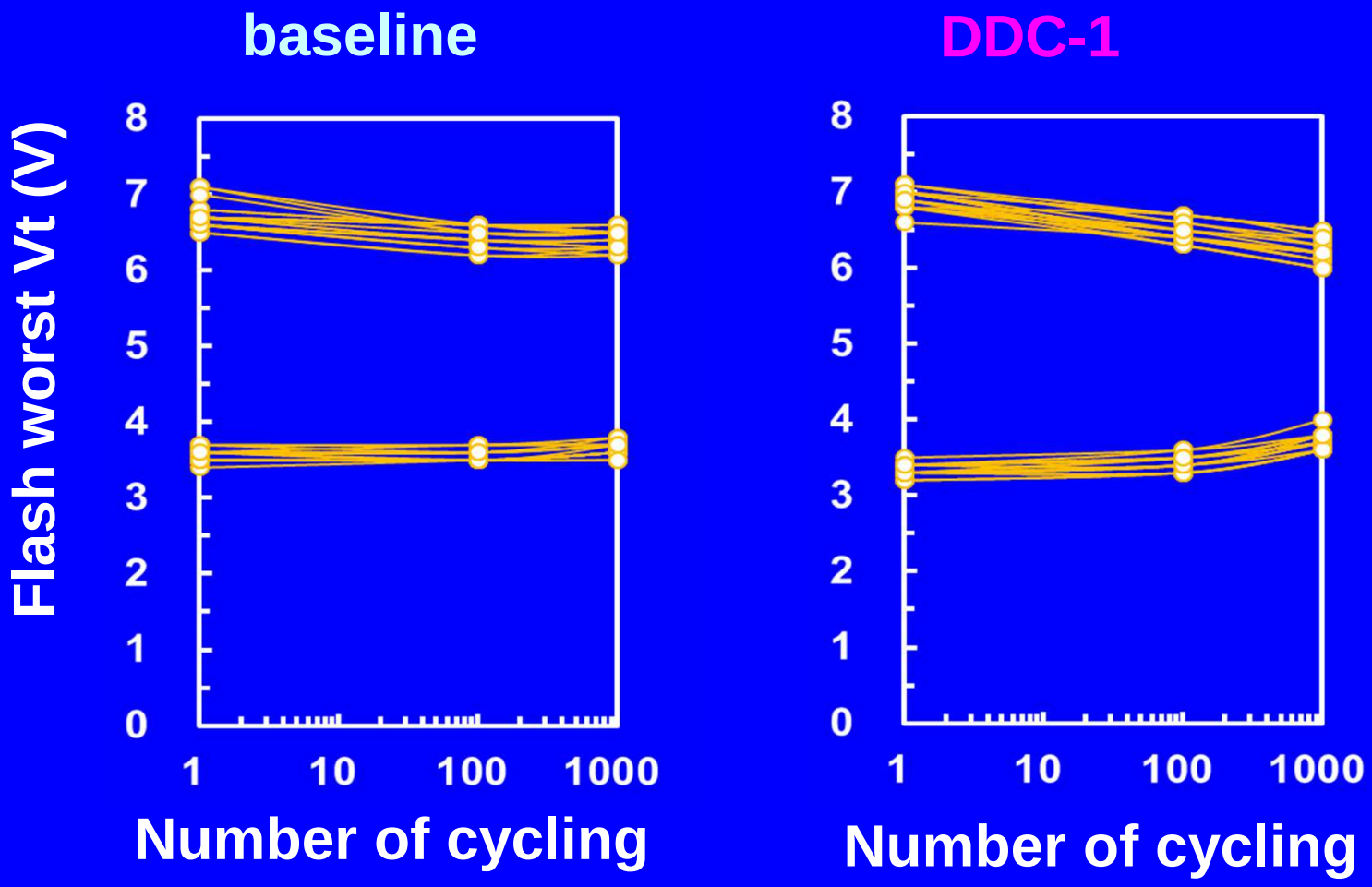
512k (512WL*1024BL) macro , 70 dice

Vtp before and after 250C bake



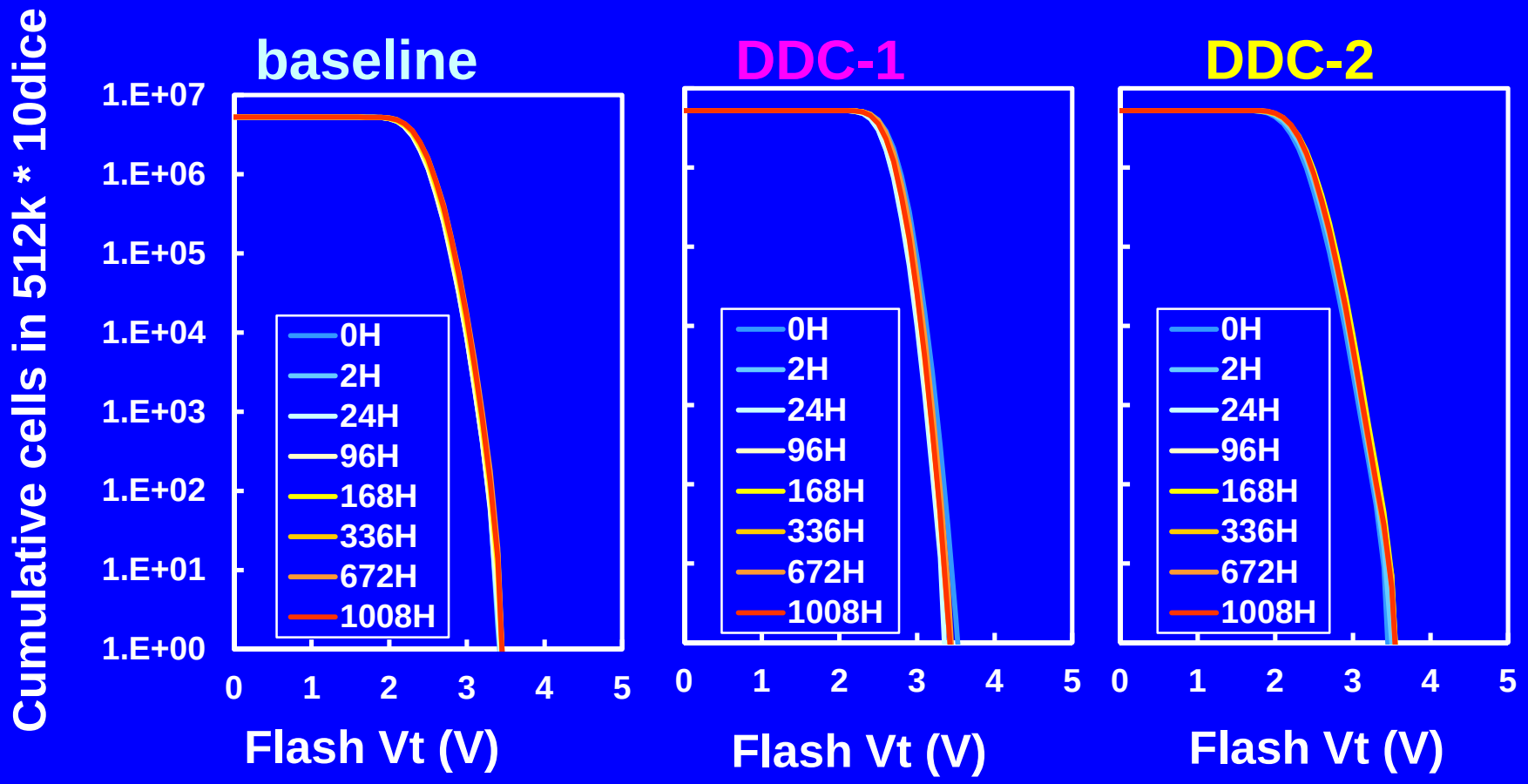
512k (512WL*1024BL) macro , 70 dice

Flash window after cycling



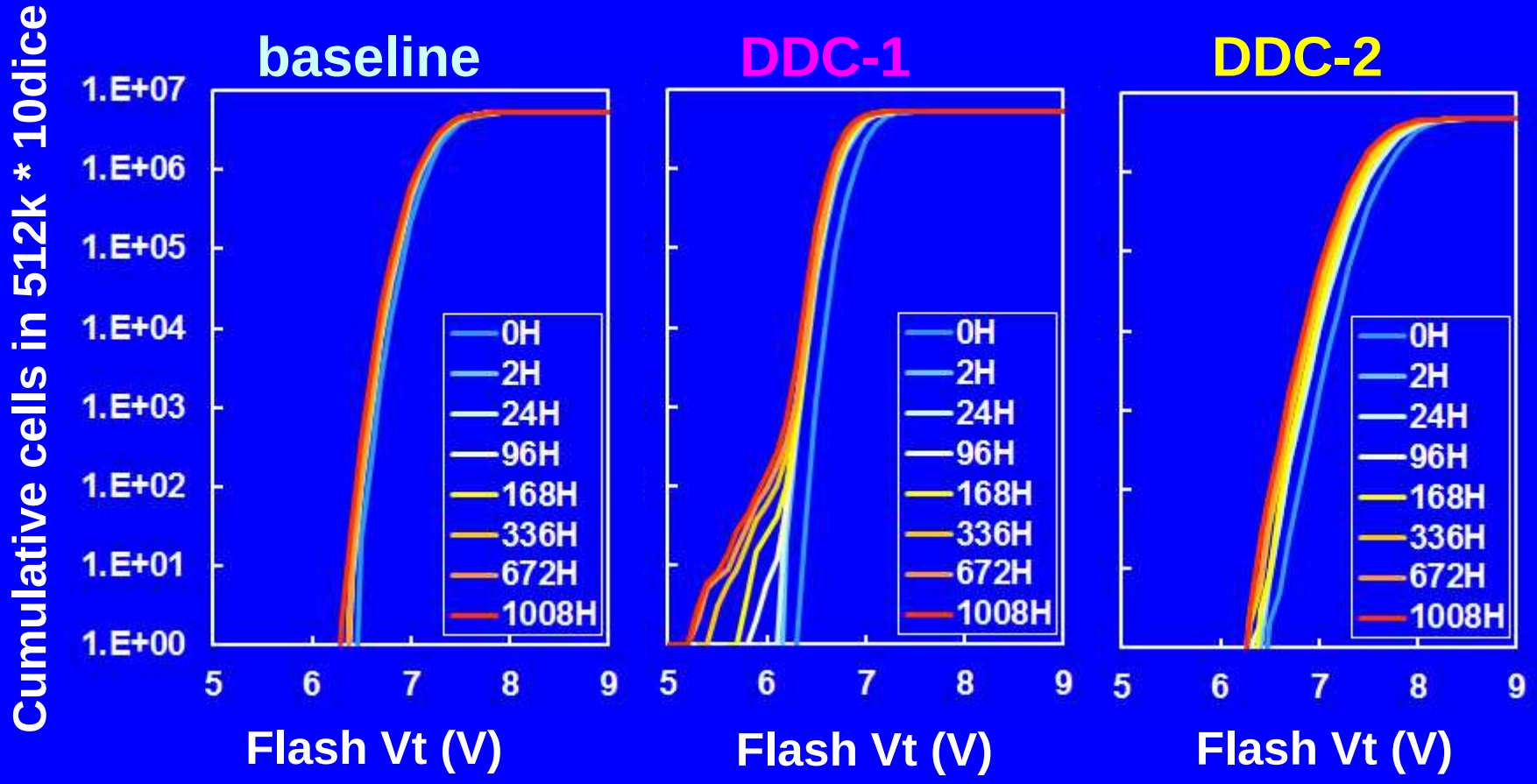
512k (512WL*1024BL) macro , 20 dice(10 for Vte, 10for Vtp) , 150C bake

Vte after 1k cycling and 150C bake



512k (512WL*1024BL) macro , 20 dice(10 for Vte, 10for Vtp) , 150C bake

Vtp after 1k cycling and 150C bake



512k (512WL*1024BL) macro , 20 dice(10 for Vte, 10for Vtp) , 150C bake

Differences between DDC-1 and -2

	Item	baseline	DDC-1	DDC-2
Process Condition	STI	POR rounding	LT small rounding	LT small rounding
	TNOX, ONO	POR	LT	LT
	Vt implant	POR	POR	lower energy
	SD implant	POR	POR	higher energy
Evaluation Results	HV-Tr BV	OK >10V	OK >10V	OK >10V
	Accelerated DD	OK	severe Vtp shift caused by hot hole injection	small Vtp shift
	Array Programming	OK	OK	OK
	Retention after 250C bake	OK	OK	OK
	Flash window after cycling	OK	faster narrowing	-
	1K cycling and 150c 1kh	OK	Vtp shift of SBCL	OK

Summary

- Embedded flash memory has been successfully integrated onto an ultra-low power 55nm DDC platform.
- This work added new knowledge,
  1) SBCL is more dominated by hot hole injection during DD rather than F-N stressing of TNOX.
  2) Very low temperature TNOX,ONO and STI schemes are not issues.