News Release

2011 年 12 月 7 日
富士通セミコンダクター株式会社
SuVolta, Inc.

富士通セミコンダクターと SuVolta、SRAM 動作を約 0.4V の超低電圧で実現

富士通セミコンダクター株式会社(本社：神奈川県横浜市、代表取締役社長：岡田 晴基、以下、富士通セミコンダクター)と SuVolta Inc.(本社：米国カリフォルニア州、CEO 兼社長：Bruce McWilliams、以下、SuVolta)は、SuVolta の“パワーシュリンク技術(注 1)”と富士通セミコンダクターの“低消費電力プロセステクノロジー”により、電源電圧が 0.425V という極めて低い電圧で SRAM を動作させることに成功しました。この両社の技術により、IC の消費電力を低減することができ、将来的には、超低消費電力製品(エコ製品)を提供することができます。詳細技術については、12 月 5 日から 7 日まで米国ワシントン DC で開催される「IEDM(International Electron Devices Meeting)2011」学会にて報告されます。

携帯機器からサーバー、ネットワーク関連機器にいたる幅広い機器において、消費電力を抑えることは重要課題の一つになっています。低消費電力化への最大の要因は電源電圧で、130nm テクノロジーまでは定常的に電源電圧の低減がなされてきました。それ以降、28nm テクノロジーにいたるまで、1V 近傍のまま低減されていません。電源電圧の低減を阻む最大の要因の一つは、組込み型 SRAM の動作電圧です。

SuVolta の“パワーシュリンク技術”の一つである DDC トランジスタ(注 2)と、富士通セミコンダクターの高度なプロセス技術を組み合わせることにより、両社はトランジスタのしきい値電圧の“ばらつき”を従来の約半分に低減し、576 キロビット(以下、Kb)の組込み SRAM で約 0.4V という極めて低い電源電圧での動作確認に成功しました。本技術は、システム LSI に用いられている既存の設計資産や既存装置などをそのまま活用することができます。

背景

微細化に沿って CMOS 回路の電源電圧は 1V 程度まで下げることができましたが、この電源電圧の低減の流れは 130nm テクノロジーまでで、それ以降の 28nm テクノロジーにいたるまでを 1V 以下に下げることができませんでした。動作時の消費電力は電源電圧の 2 乗に比例するため、消

費電力削減は CMOS 回路における重要な課題となっています。電源電圧の低減が 130nm テクノロジーで停滞したのは、RDF(Random Dopant Fluctuation)を含むいくつかのばらつき要因が存在するためです。RDF とは、不純物原子の位置と密度のランダムな揺らぎのことで、これによりトランジスタのしきい値電圧に“ばらつき”が大きく生じます。

極薄膜 SOI(Silicon on Insulator)トランジスタとフィン型トランジスタ構造により、RDF を劇的に改善できると報告されていますが、構造的に複雑であり、既存の設計資産や製造資産を利用することが困難と考えられました。

SuVolta の DDC トランジスタ構造

図 1.に、富士通セミコンダクターの低電力 CMOS 回路用プロセス技術を用いて製造した、SuVolta の DDC トランジスタ構造の断面 TEM(Transmission Electron Microscope)写真を示します。DDC トランジスタは、既存のトランジスタと同様にシリコン基板上に形成されます。

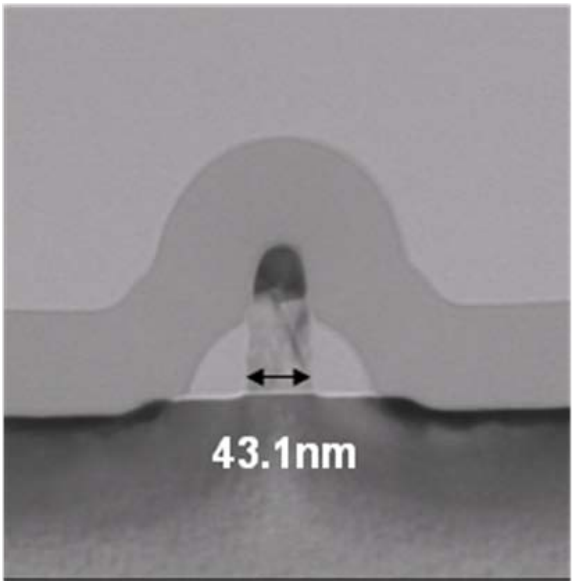

図 1. DDC トランジスタの断面 TEM 写真

組込み SRAM による電源電圧の低下と歩留まり

富士通セミコンダクターと SuVolta は、DDC トランジスタにより、組込み SRAM が 0.425V でも動作することを実証しました。図 2.に、その結果を示します。大半の製品における電源電圧の下限は、組込み SRAM の安定動作により決まるため、さまざまな CMOS 回路を搭載した製品でも 0.4V 近傍で動作することを実証したことになります。

図 2.は、576Kb の組込み SRAM の歩留まりを電源電圧の関数として示したものです。歩留まりは、576Kb すべてが動作した組込み SRAM 数から歩留まりを計算しています。

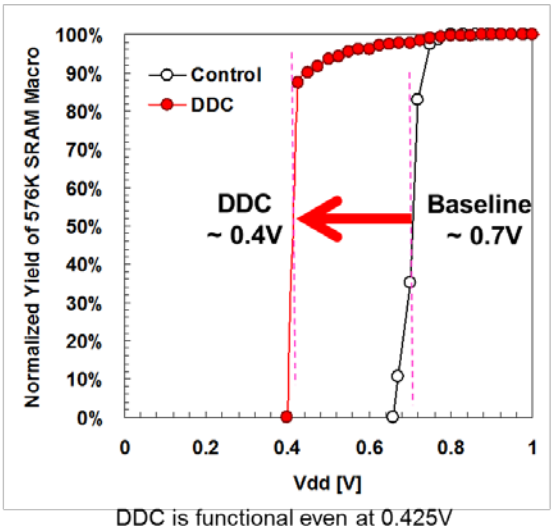

図 2. 576Kb 組込み SRAM の歩留まりの電源電圧依存推移

注釈

注１ パワーシュリンク技術:SuVolta の開発した消費電力低減技術全般の総称であり、後述する DDC トランジスタとこれを効果的に使用する回路などを含みます。

注２ DDC トランジスタ(Deeply Depleted Channel transistor):
シリコン基板上に複数の不純物層を含み構成することを特徴とします。

商標について

【本件に関する技術お問い合わせ先】

富士通セミコンダクター株式会社

お問い合わせ：http://edevice.fujitsu.com/jp-qform.html

SuVolta, Inc.
DDC トランジスタについて
www.suvolta.com/cmos-power/
SuVolta Inc.詳細： http://www.suvolta.com/sales-inquiry/
ツイッター：http://twitter.com/SuVoltaInc

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Advanced Channel Engineering Achieving Aggressive Reduction of V_T Variation for Ultra-Low-Power Applications

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Abstract

We have achieved aggressive reduction of V_T variation and $V_{DD\text{-}min}$ by a sophisticated planar bulk MOSFET named 'Deeply Depleted Channel™ (DDC)'. The DDC transistor has been successfully integrated into an existing 65nm CMOS platform by combining layered channel formation and low temperature processing. The 2x reduction of V_T variation in 65nm-node has been demonstrated by matching SRAM pair transistors, 2x improvement in SRAM static noise margin (SNM) and 300 mV $V_{DD\text{-}min}$ reduction of 576Kb SRAM macros to 0.425 V using conventional 6T cell layout.

Introduction

Power consumption of scaled CMOS is a big issue. Ultra-low-voltage operation is very effective to reduce both static and dynamic power. However, ultra-low-voltage operation is limited by V_T variation as widely discussed for SRAM [1].

V_T variation has two components, inter-die and intra-die variation. The former is caused by manufacturing fluctuation such as CD variation and can be compensated by design techniques such as adaptive Vbb control. On the other hand, the latter is caused by physical mechanisms such as random dopant fluctuation (RDF) [2], line edge roughness (LER) [3] and poly grain granularity (PGG) [4].

RDF is the dominant mechanism of intra die V_T variation. New structures such as ETSOI [5], Tri-gate FET [6] and delta-doped channel bulk MOSFET [7] were proposed to solve RDF. Among the structures, delta-doped channel bulk MOSFET is the most desirable solution because it very easily matches with adaptive Vbb control independently applicable to both NMOS and PMOS, simple planar manufacturing infrastructure and existing IP design layouts including multiple V_T and legacy transistors.

Epitaxial channel selectively grown after STI was proposed to realize the delta-doped channel bulk MOSFET [8, 9]. However the prior articles focused on capability to achieve higher performance and shorter channel rather than reduction of V_T variation. Moreover, selectively grown epitaxial Si has facet at the edge of active area which may generate parasitic leakage.

In this paper, we report 1) DDC structure achieving 2x reduction of V_T variation, 2) combination of layered channel formation and low temperature process flow realizing DDC transistor, 3) 65nm SRAM results demonstrating the aggressive reduction of V_T variation by DDC and its capability of ultra-low-voltage operation.

DDC Transistor Structure

Cross sectional TEM of fabricated DDC transistor is shown in Fig. 1(a) and sketch of it is shown in Fig. 1(b). Several layers are stacked in usual P or Nwell formed in bulk silicon substrate. Layer 4 serves to prevent sub-channel punch-through. Layer 3 is the screening layer, which terminates the depletion layer in the channel and also serves to smooth the depletion layer across the device, affording excellent σV_T and short channel effects. Layer 2 is V_T setting layer that allows multiple threshold voltage devices, which are highly desired for many SoC applications. Together, these three deep layers also produce a strong body coefficient that matches adaptive Vbb control and enables many circuit level power reduction techniques. Layer 1 is a very low doped channel that reduces RDF. A key benefit of the DDC architecture is that it is fully compatible with all known transistor performance enablers including PMOS embedded SiGe S/D. The devices reported here also utilized a tensile capping layer to enhance NMOS performance as seen in Fig. 1(a).

Features of Process Flow and Verification of Them

Process flow to fabricate DDC transistor is shown in Fig. 2. The process flow serves not only low voltage (LV) operating DDC transistors but also high voltage (HV) operating legacy transistors such as 3.3V I/O transistors. Layer 1 is formed by state of the art blanket undoped epitaxial deposition, giving excellent uniformity and allowing for near perfect thickness control across a wafer. This layer is grown after forming the layered channel stack by implantation and before STI. STI and gate oxidation (GOX) for both HV and LV transistors are done at very low temperature to prevent the impurity profiles in the channel stack from diffusing. No halo implant is done for DDC transistors. Steps for doping and activating gate, source/drain are set as same as baseline 65nm process not to cause gate depletion nor increased parasitic source drain resistance.

Since all process conditions except reduced thermal budget for STI & GOX were set as same as baseline 65nm technology, concerns of the process flow are focused on items related to low temperature STI & GOX.

Cross-sectional TEM picture of STI is shown in Fig. 3. Though increased STI recess and/or divot due to low temperature process were concerned, excellent STI shape has been achieved by optimizing other parameters for the STI process.

W dependence of V_T is shown in Fig. 4. No abnormality is seen. Sub-threshold characteristics of both NMOS and PMOS

DDC are shown in Fig. 5. No kink of sub-threshold characteristics is seen. These results demonstrate no parasitic leakage path along STI edge because of blanket epitaxial layer and optimized low temperature STI process.

Distribution of breakdown voltage for low temperature gate dielectric on DDC transistor is shown in Fig. 6. No concern is seen. HCI of NMOS and PMOS DDC results are shown in Fig. 7. Estimated lifetimes are long enough even for 1.2V applications. NBTI of PMOS DDC is shown in Fig. 8. Estimated lifetime is long enough even for 1.2V applications. These results demonstrate no concern about reliability due to the low temperature GOX process.

65nm SRAM Evaluation Results

Because SRAM is the severest circuit for ultra-low voltage operation, it is the best to demonstrate capability of DDC transistors to achieve aggressive reduction of V_T variation and ultra-low voltage operation. Data on DDC transistors are compared with the ones on existing baseline 65nm control wafer using a same SRAM macro. The SRAM macro, which is in production for our 65nm ASIC offering, was used for the control and DDC wafers with no layout or design changes.

Fig. 9(a-c) shows across-wafer V_T distributions of 3 types of 6T SRAM cell transistors. These data represents inter-die V_T variation. Much tighter V_T distribution of DDC than control has been demonstrated although NMOS V_T of DDC wafer in this experiment was deviated from control. Fig. 9(d) illustrates that inter-die V_T variation is reduced to half by DDC transistor. The result demonstrates not only excellent capability of DDC transistor itself but also excellent uniformity of process parameters across a wafer such as epitaxial layer and low temperature GOX thickness.

Fig. 10(a-c) shows distributions of V_T matching for 3 types of pair transistors forming 6T SRAM cell. These data represents intra-die V_T variation. Fig. 10(d) illustrates that intra-die V_T variation is reduced to half by DDC transistor. The result demonstrates not only excellent capability of DDC transistor itself but also the low temperature process flow successfully achieving ideal DDC channel profiles reducing RDF.

Fig. 11(a-b) shows superposition of 6T SRAM butterfly curves on DDC and control wafers. Much clearer butterfly curve of DDC than control at low V_{dd} region is seen. Smaller SNM of DDC than control at high V_{dd} region is caused by lower NMOS V_T of DDC in this experiment than control and is improved by adjusting NMOS V_T.

Fig. 12(a-b) shows distribution of SNM within each of DDC and control wafers. Both distributions are nice normal distributions and it is clear that the distribution of DDC is much tighter than control.

Fig. 13(a-b) shows the measured mean & sigma SNM as a function of V_{dd}, and demonstrates that SNM variation is aggressively reduced to half by DDC transistor. Fig. 13(c) shows mean/1σ of SNM as a function of V_{dd}. It is required to keep >5σ margin for 1Mb SRAM function. DDC transistor has sufficient margin even if V_{dd}=0.4 V.

Fig. 14 shows functional yield of 576Kb SRAM macros as a function of V_{dd}. The yield means no fail bit in 576Kb SRAM array. The DDC showed good yield down to V_{dd}=0.425 V, 300 mV lower than the control, as predicted by the measured SNM results shown in Fig. 13(c).

All these results consistently demonstrate both outstanding capability of DDC transistor for ultra-low-voltage applications and manufacturability of it.

Conclusions

A new planar transistor architecture (DDC) has been successfully fabricated for the first time by combination of layered channel formation and low temperature processing. The new process was shown to not affect critical performance parameters such as parasitic leakage along STI edge and gate insulator related reliability. The DDC transistor is promising for ultra-low power applications as shown by 2x improvement in inter-die and intra-die V_T variation and 2x improvement in 6T SRAM SNM. We have demonstrated 300mV $V_{DD\text{-}min}$ reduction and fully functional 576Kb SRAM down to 0.425V.

Acknowledgements

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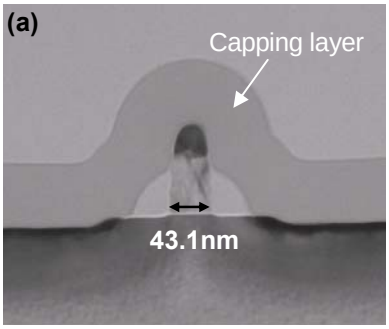

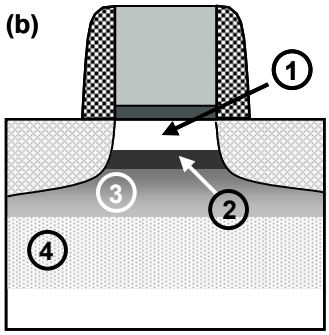

Fig.1 (a) Cross-sectional TEM picture of DDC transistor, (b) Cross sectional sketch of DDC transistor.

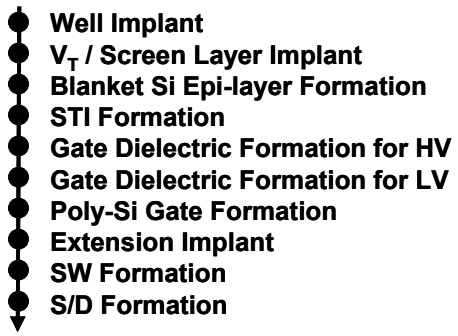

Fig.2 DDC process flow with low-temperature STI & GOX

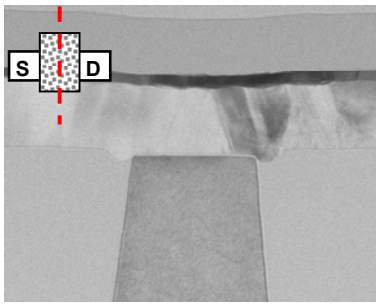

Fig.3 Cross-sectional TEM picture of STI formed by low-temperature process.

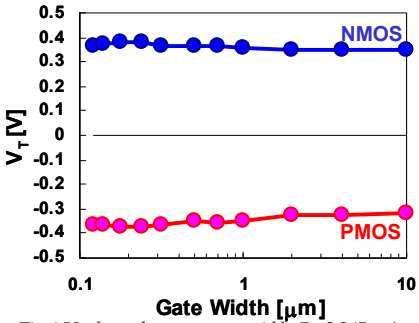

Fig.4 V_T dependence on gate width (L=0.045μm). V_T is defined as V_g at I_d=3E-6*W/L [A] for NMOS and -1E-6 for PMOS.

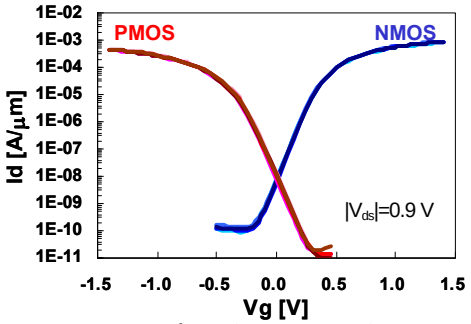

Fig.5 V_g-I_d curves of DDC (W/L=1/0.045 μm).

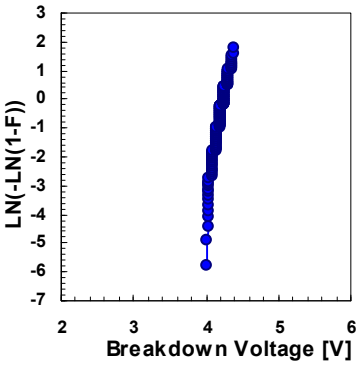

Fig.6 VRDB results of LV gate dielectric. W/L=5/0.045 μm. S_g=1E-7 cm^2.

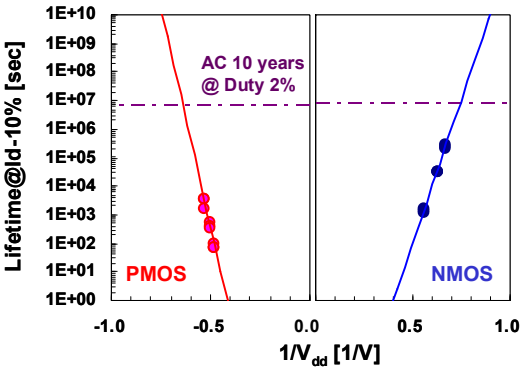

Fig.7 HCI results of NMOS and PMOS DDC at T=25C. W/L=10/0.045μm.

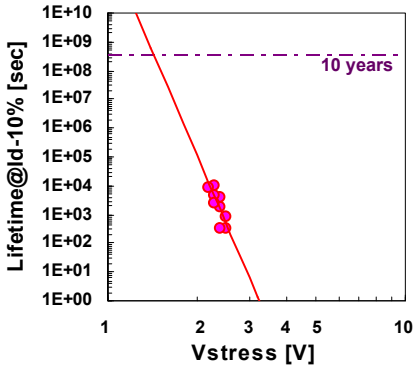

Fig.8 NBTI result of PMOS DDC at T=125C. W/L=10/0.045μm.

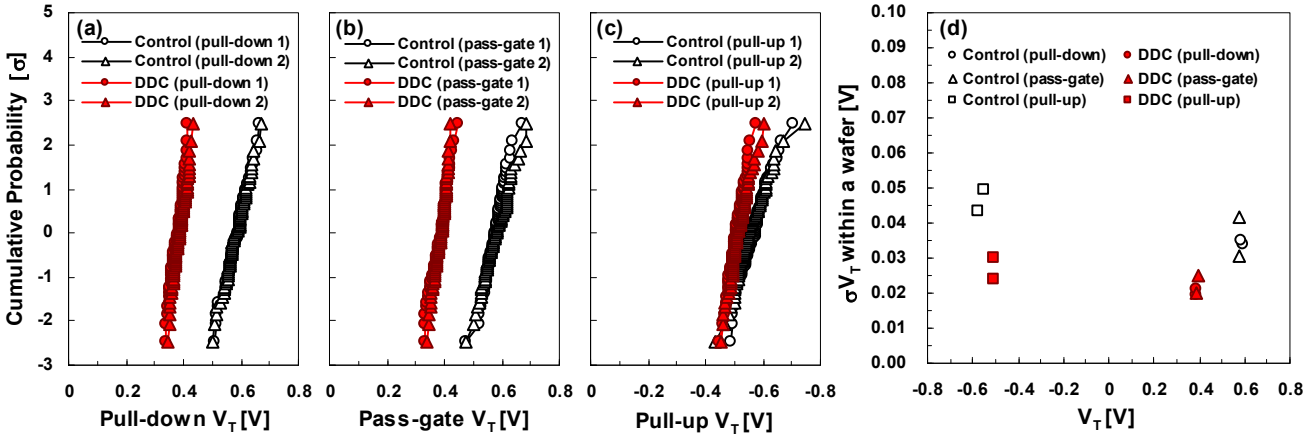

Fig.9 Across-wafer V_T distributions of (a) pull-down, (b) pass-gate and (c) pull-up. (d) Inter-die V_T variation as a function of V_T at V_{dd}=1.2V. V_T is defined as V_g at Ids=3E-6*W/L[A] for NMOS and 1E-6 for PMOS.

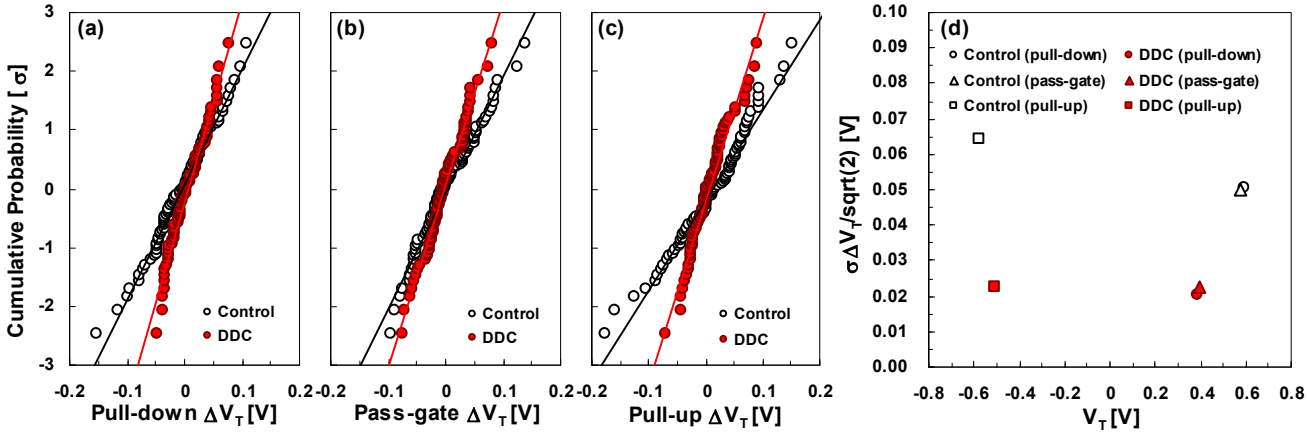

Fig.10 Distribution of V_T matching for (a) pull-down pairs, (b) pass-gate pairs and (c) pull-up pairs within a wafer. (d) Intra die V_T variation as a function of V_T at V_{dd}=1.2V. V_T is defined as V_g at Ids=3E-6*W/L [A] for NMOS and 1E-6 for PMOS.

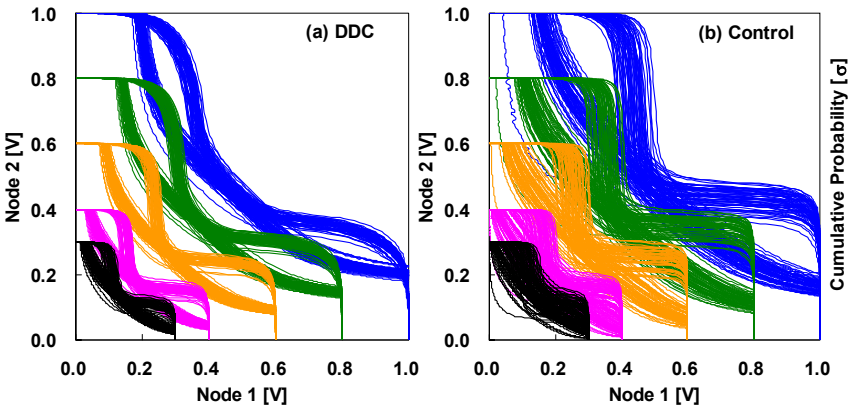

Fig.11 Superposed butterfly curves of 65nm-node SRAM cell (0.54 μm^2) on (a) DDC and (b) control.

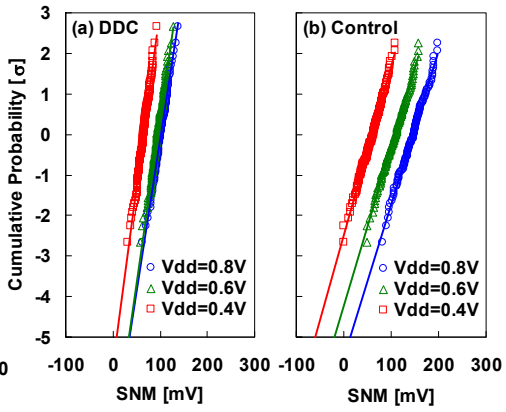

Fig.12 Distribution of SNM for (a) DDC and (b) control.

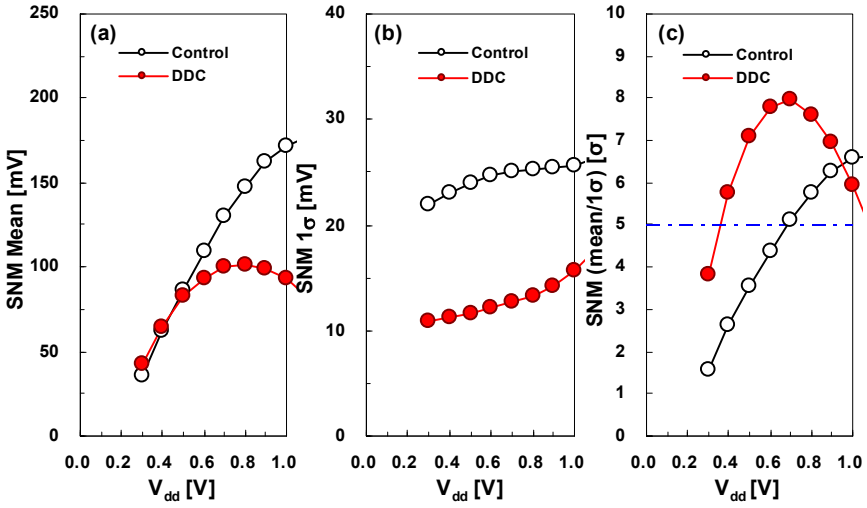

Fig.13 Measured (a) mean, (b) sigma, and (c) mean/1σ of SNM.as a function of V_{dd}.

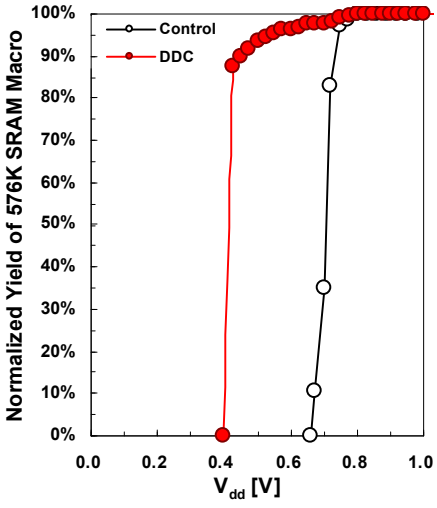

Fig.14 $V_{DD\text{-}min}$ of 576K bit SRAM array. Single bit fail is counted as array fail.

Advanced Channel Engineering Achieving Aggressive Reduction of V_T Variation for Ultra-Low-Power Applications

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**SuVolta Inc.*

FUJITSU

SUVOLTA™

Outline

- Introduction
- Transistor Structure
- Features of Process Flow and Verification
- 65nm 6T-SRAM Evaluation Results
- Summary

Introduction

V_{DD} lowering

V_T variation

RDF

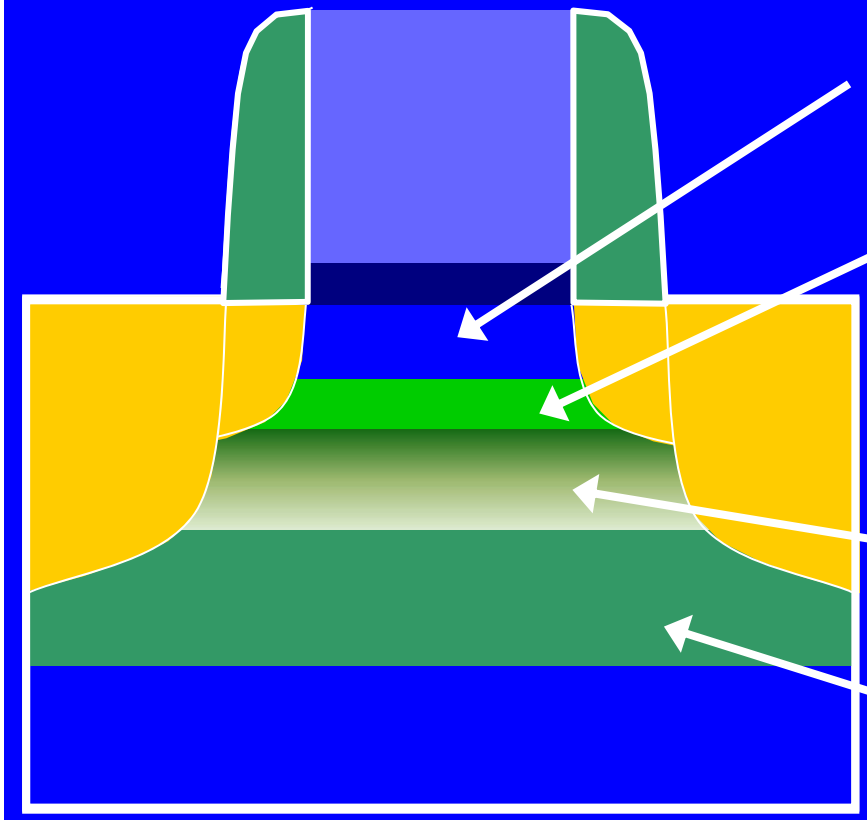
ETSOI, Tri-gate

Alternative solution

→ *complicated*

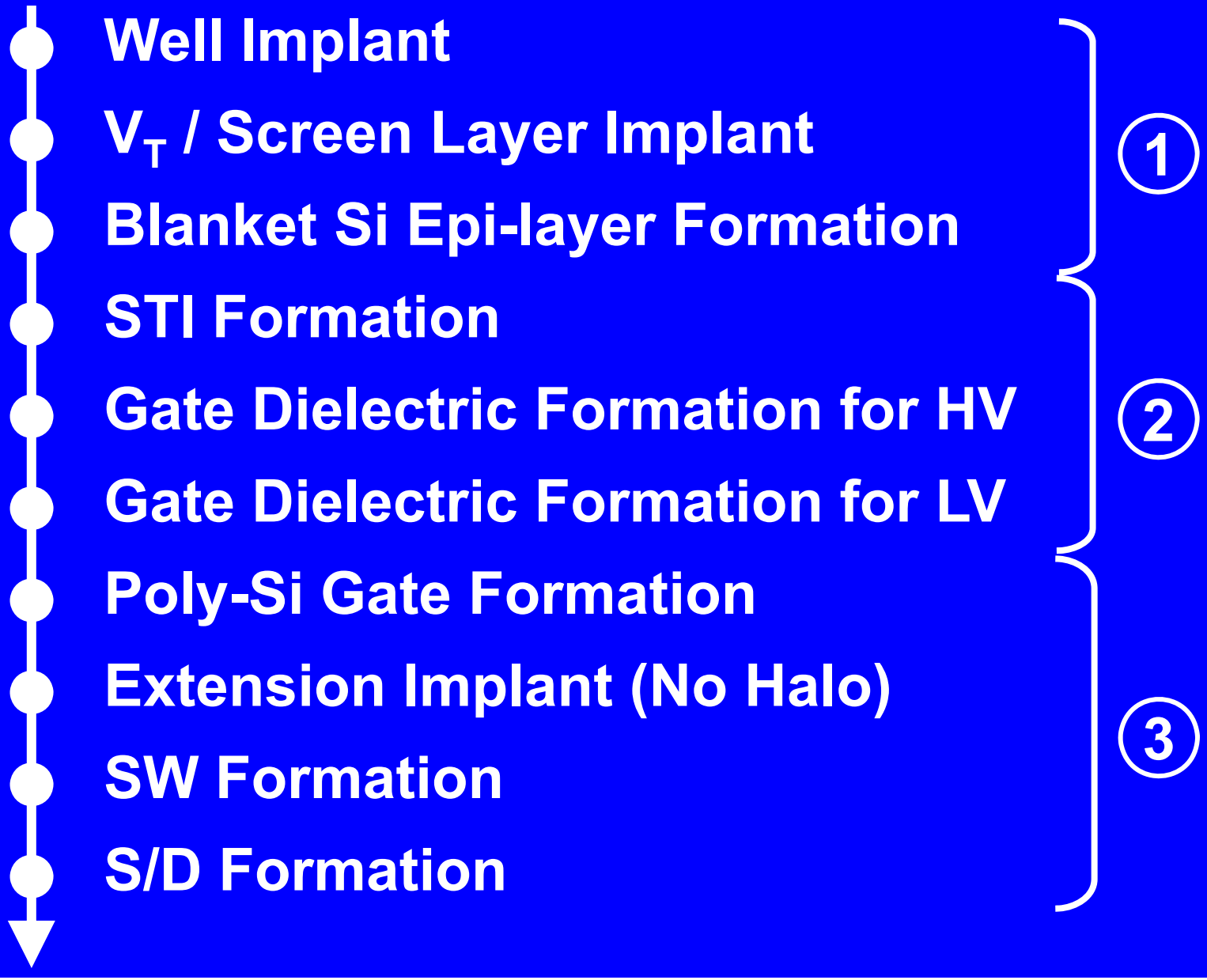
Transistor structure

Deeply Depleted Channel ™ (DDC) Transistor

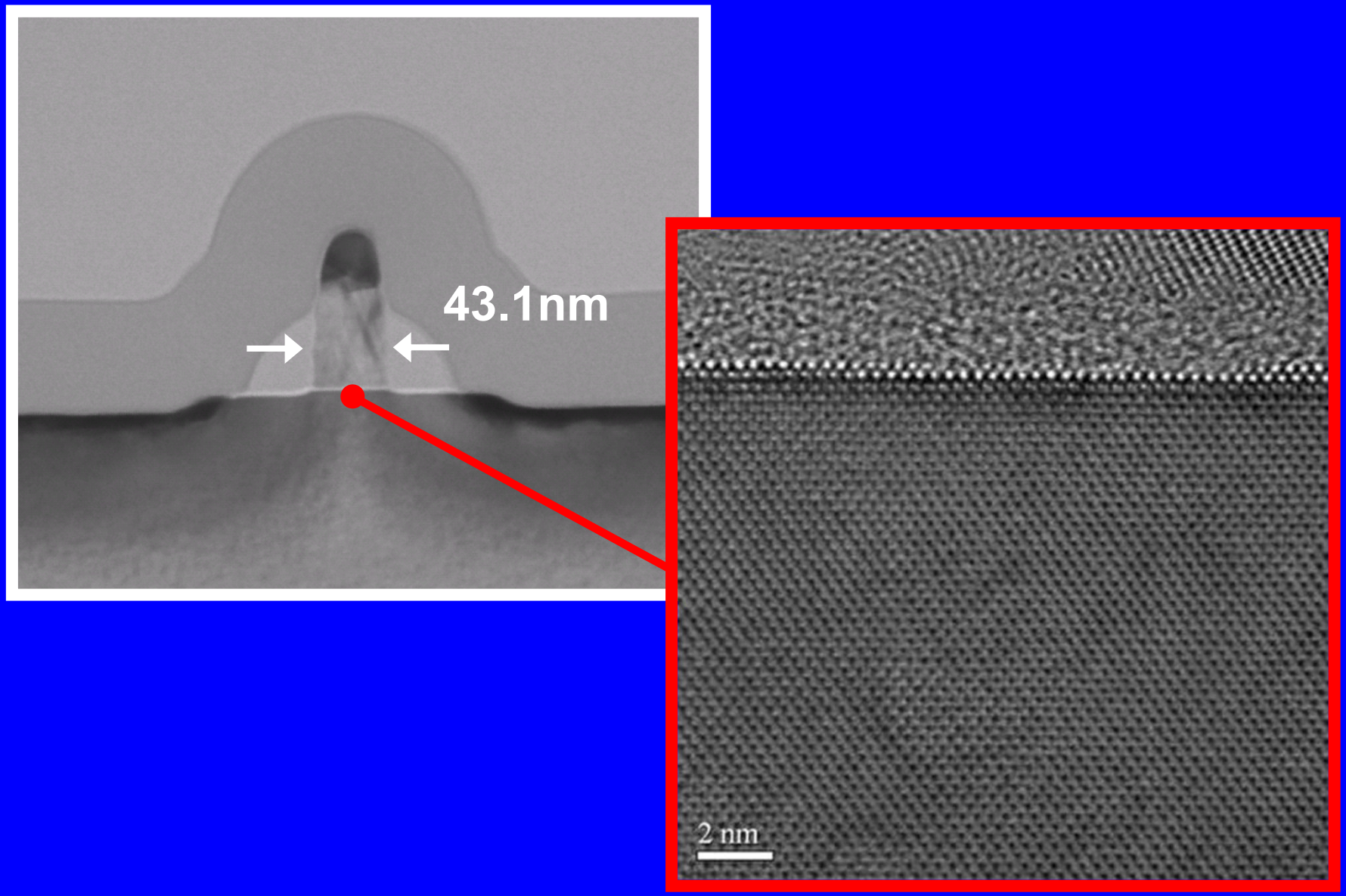


1. Depleted layer
2. V_T setting offset layer
3. Screening layer
4. Anti-punch-through layer

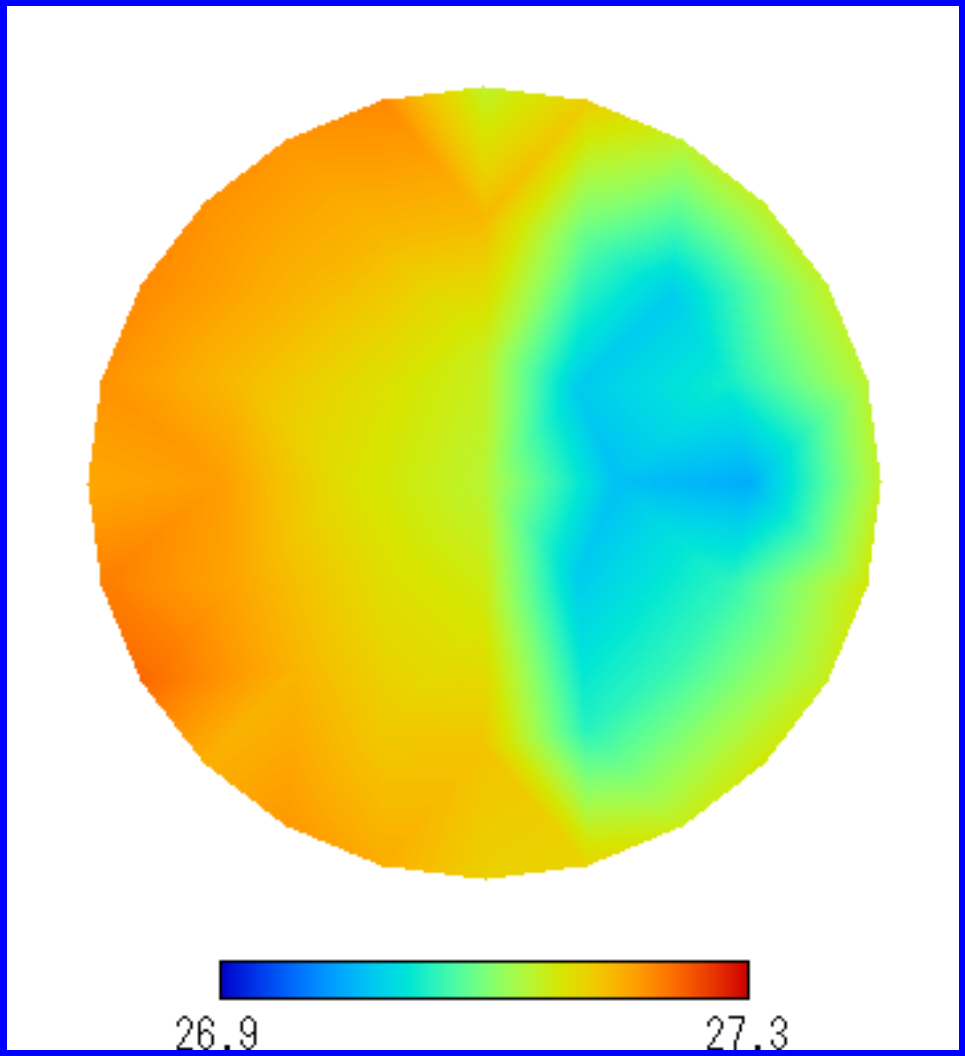
Process flow



TEM of DDC transistor

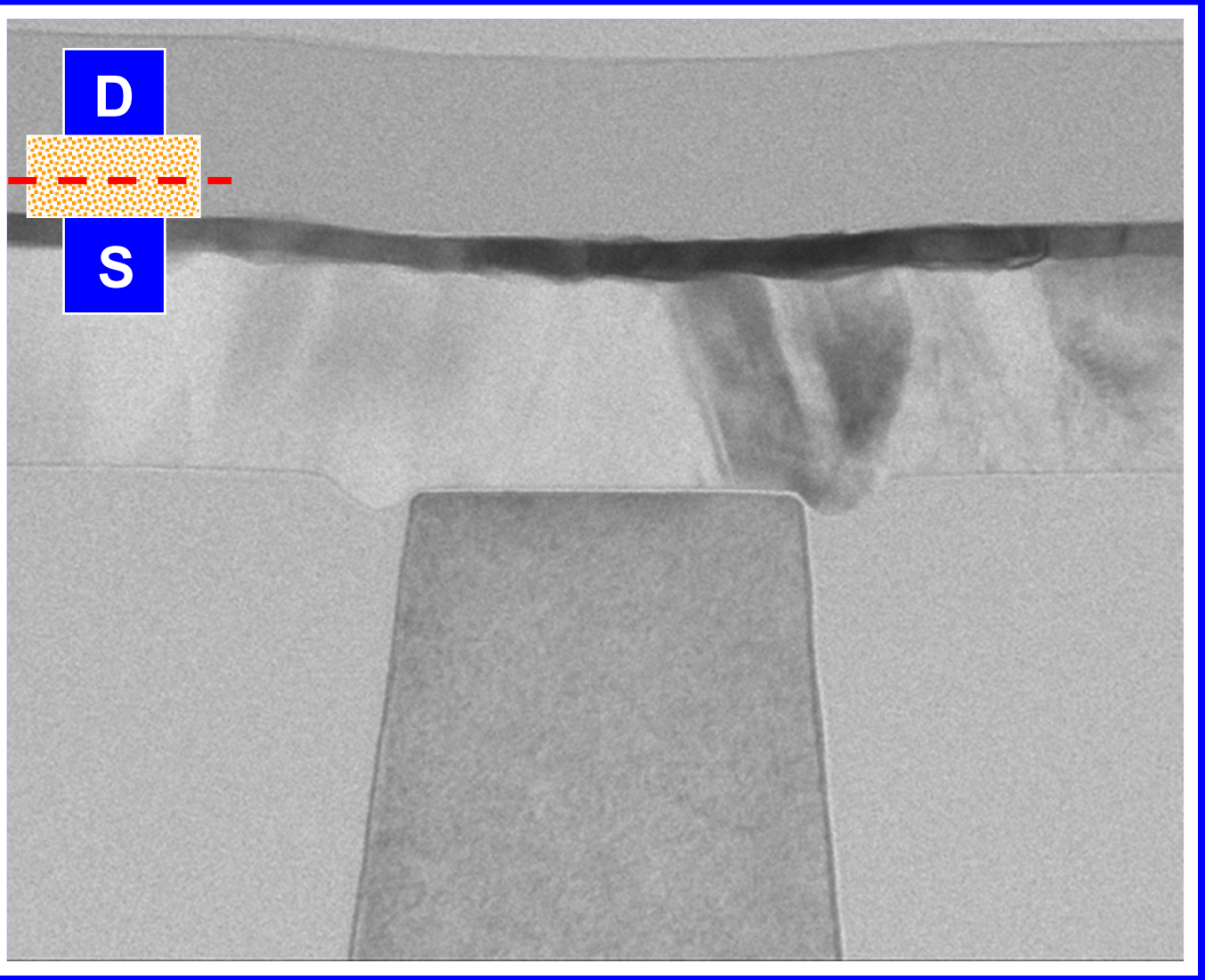


Uniformity of epitaxial silicon

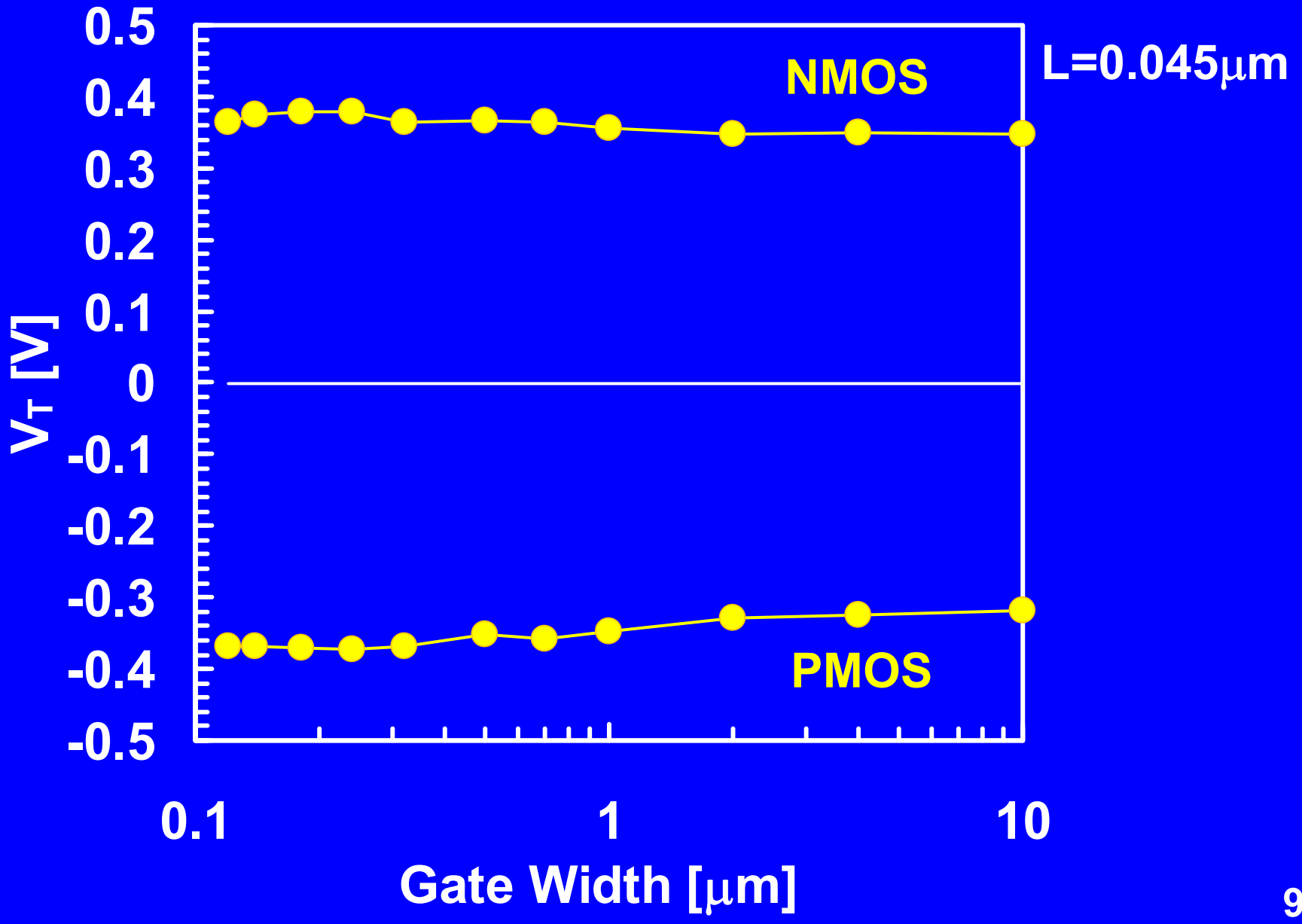


Avg. = 27.2nm, 1sigma = 0.25%

TEM of low-temperature STI

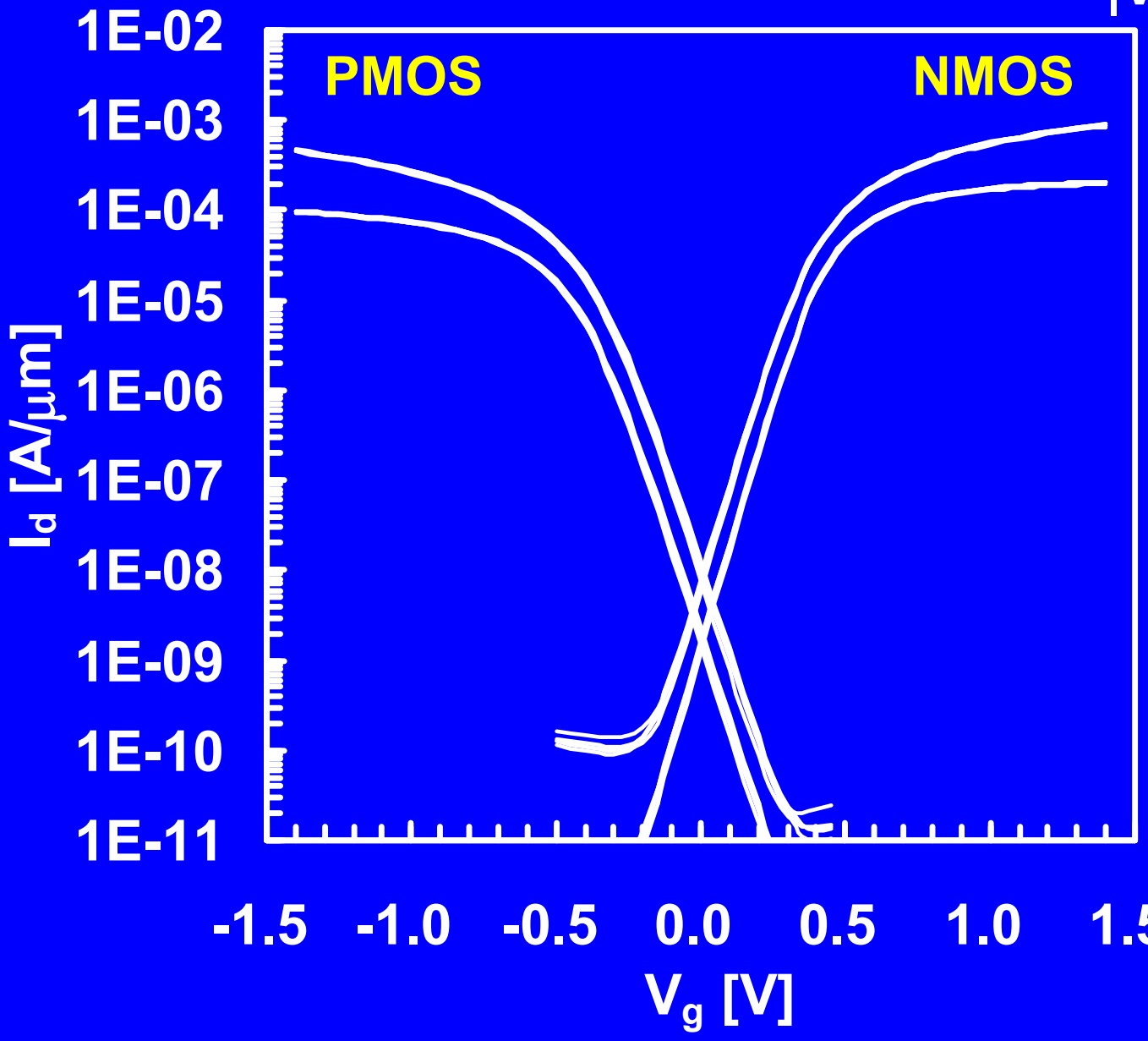


W-dependence of V_T



I-V characteristics

L=0.045μm
|Vdd|=0.9, 0.1V

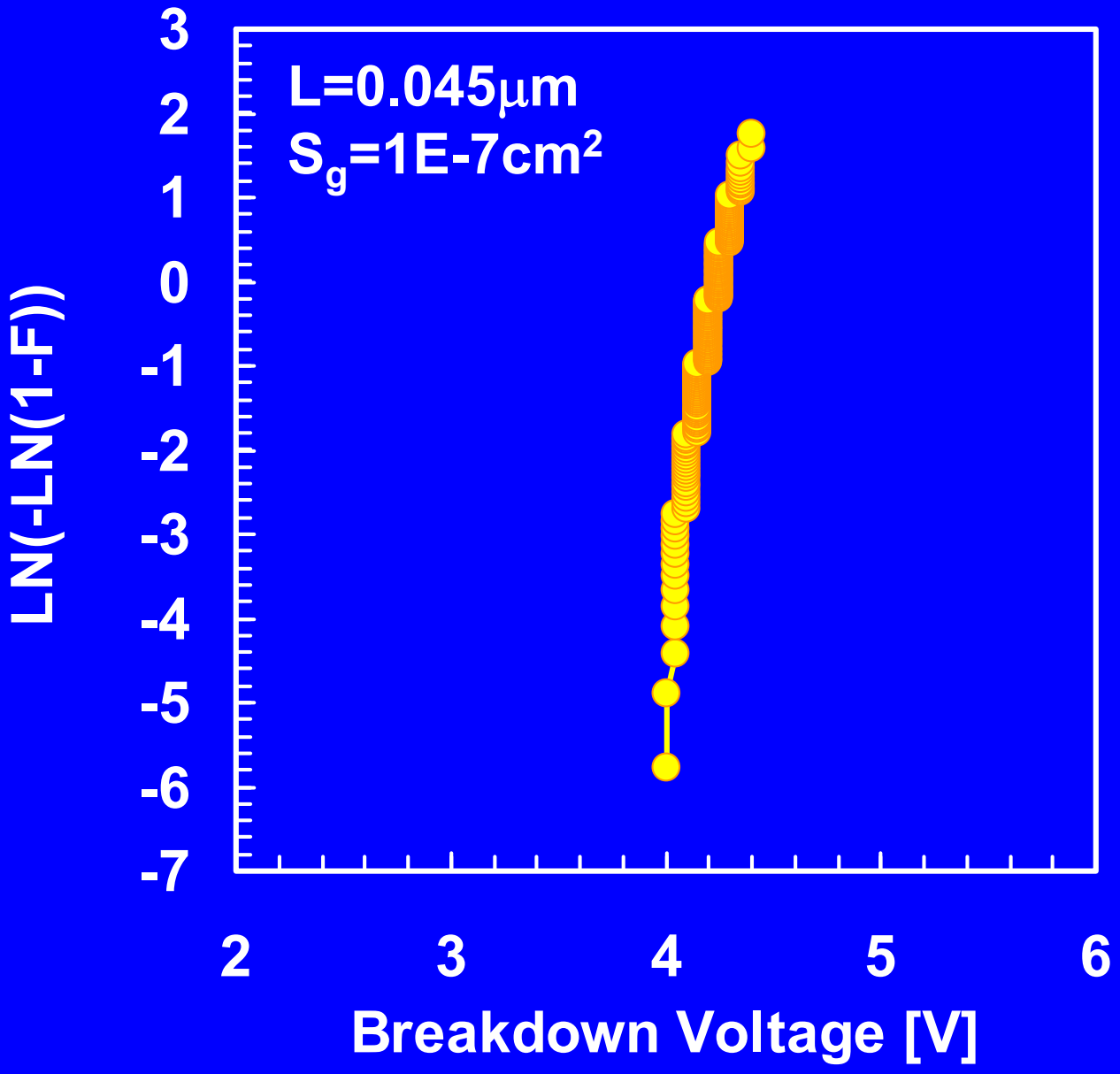


Summary of STI

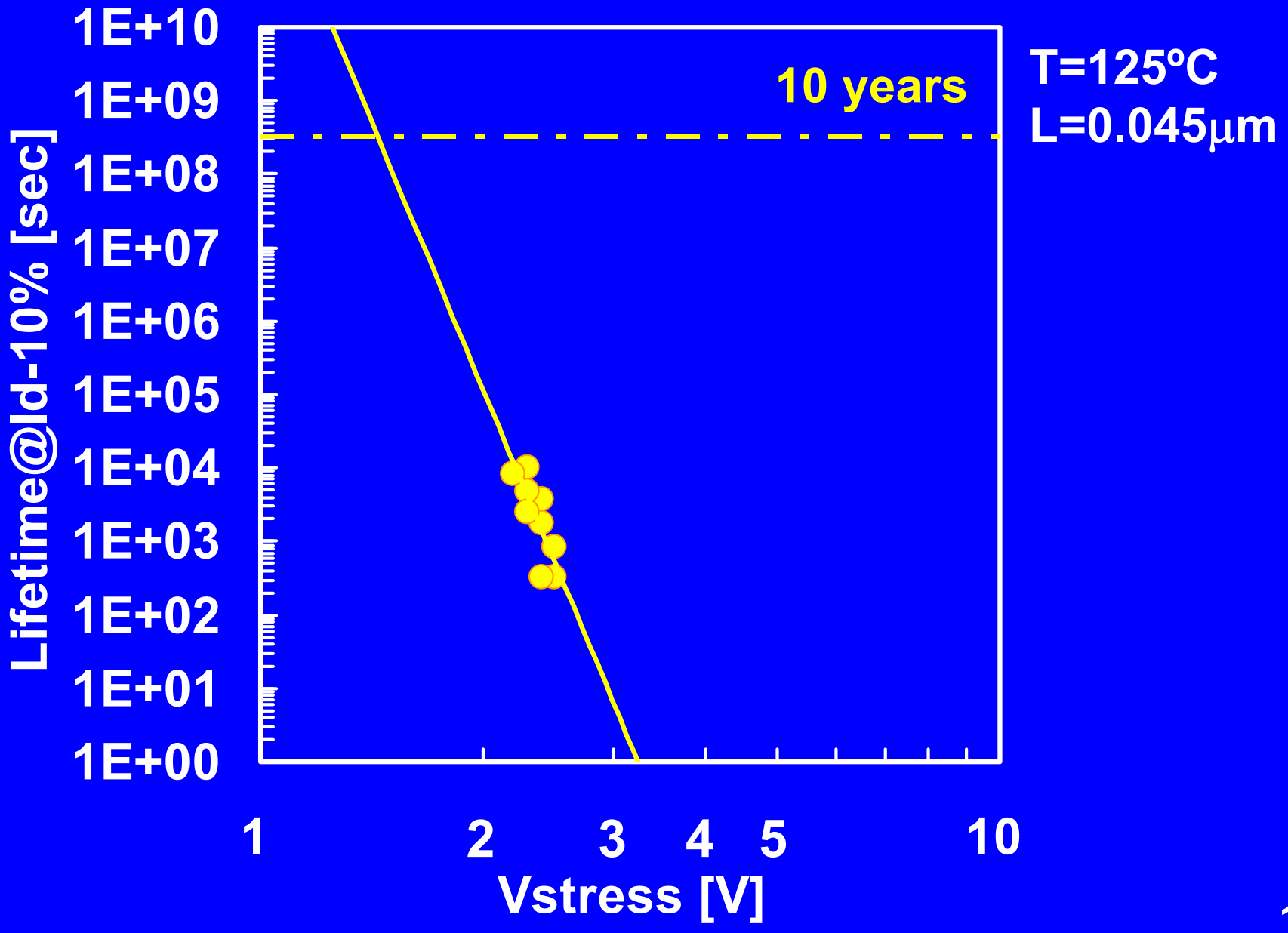
- Excellent STI profile
- No anomalous W dependence
- Nice sub-threshold characteristics

No concern about low temp. STI

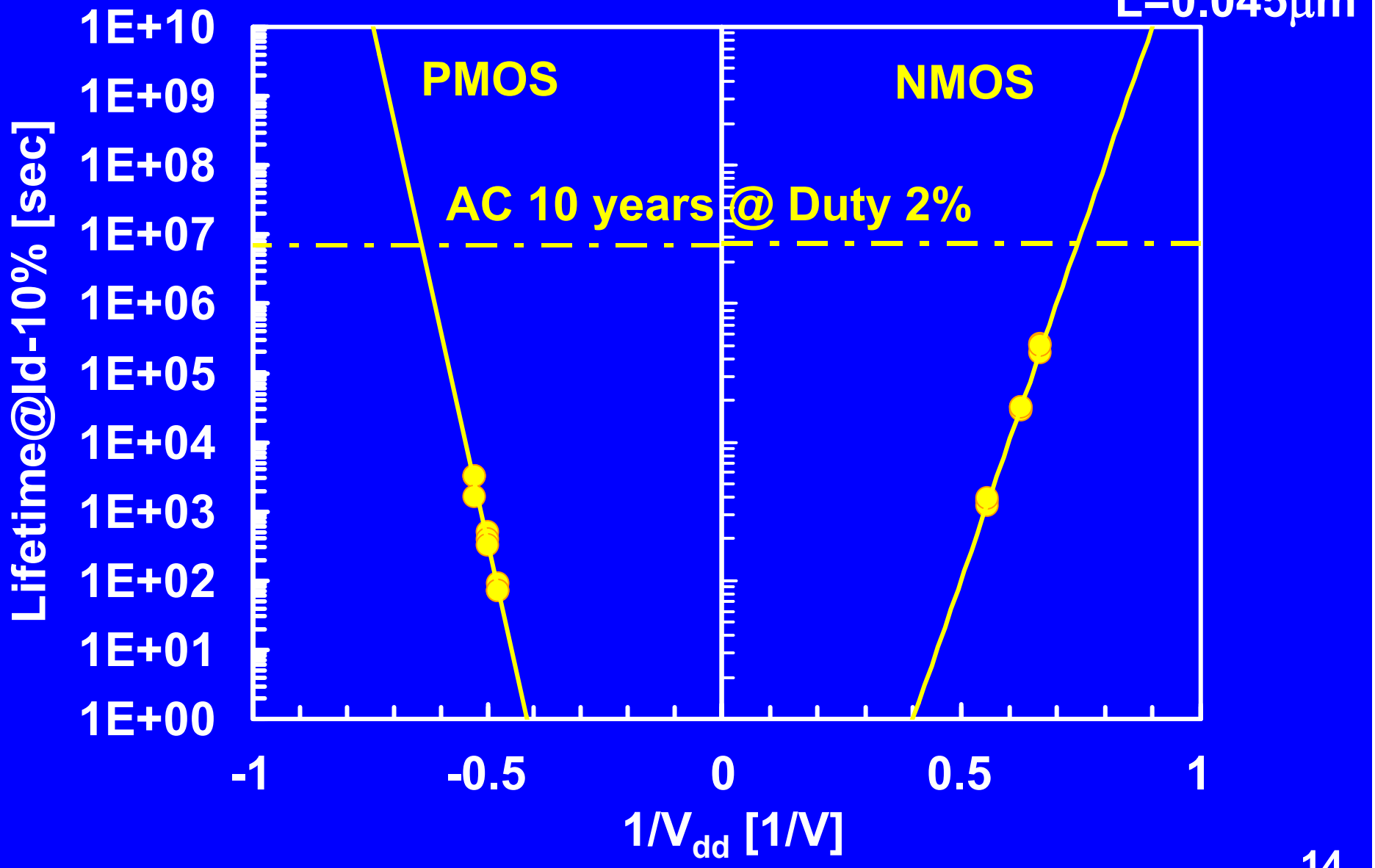
Breakdown of low-temperature GOX



NBTI of DDC PMOS



HCI of DDC

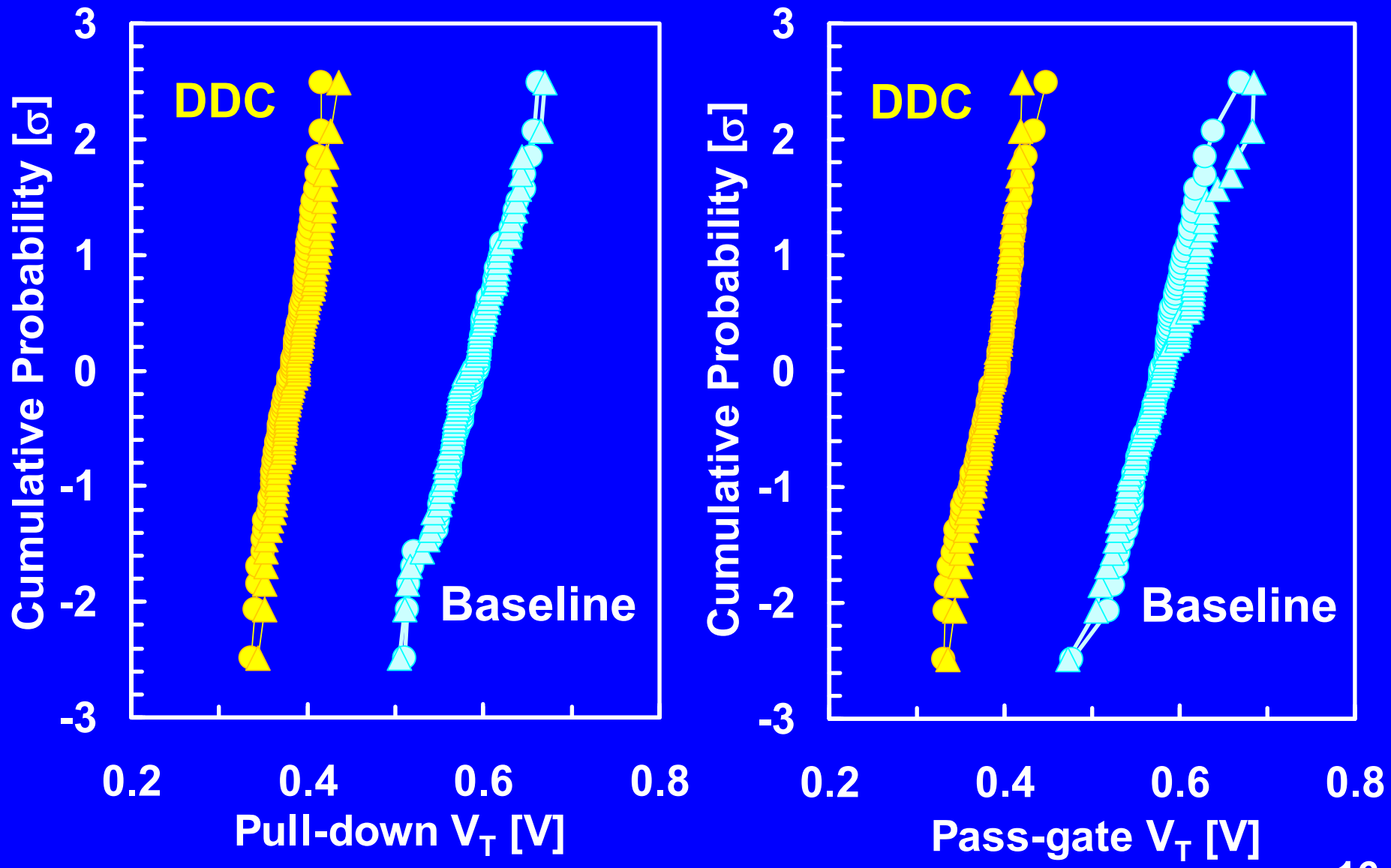

T=25ºC
L=0.045μm
PMOS
NMOS
AC 10 years @ Duty 2%
Lifetime@Id-10% [sec]
1E+10
1E+09
1E+08
1E+07
1E+06
1E+05
1E+04
1E+03
1E+02
1E+01
1E+00
-1
-0.5
0
0.5
1
1/V_dd [1/V]

Summary of GOX

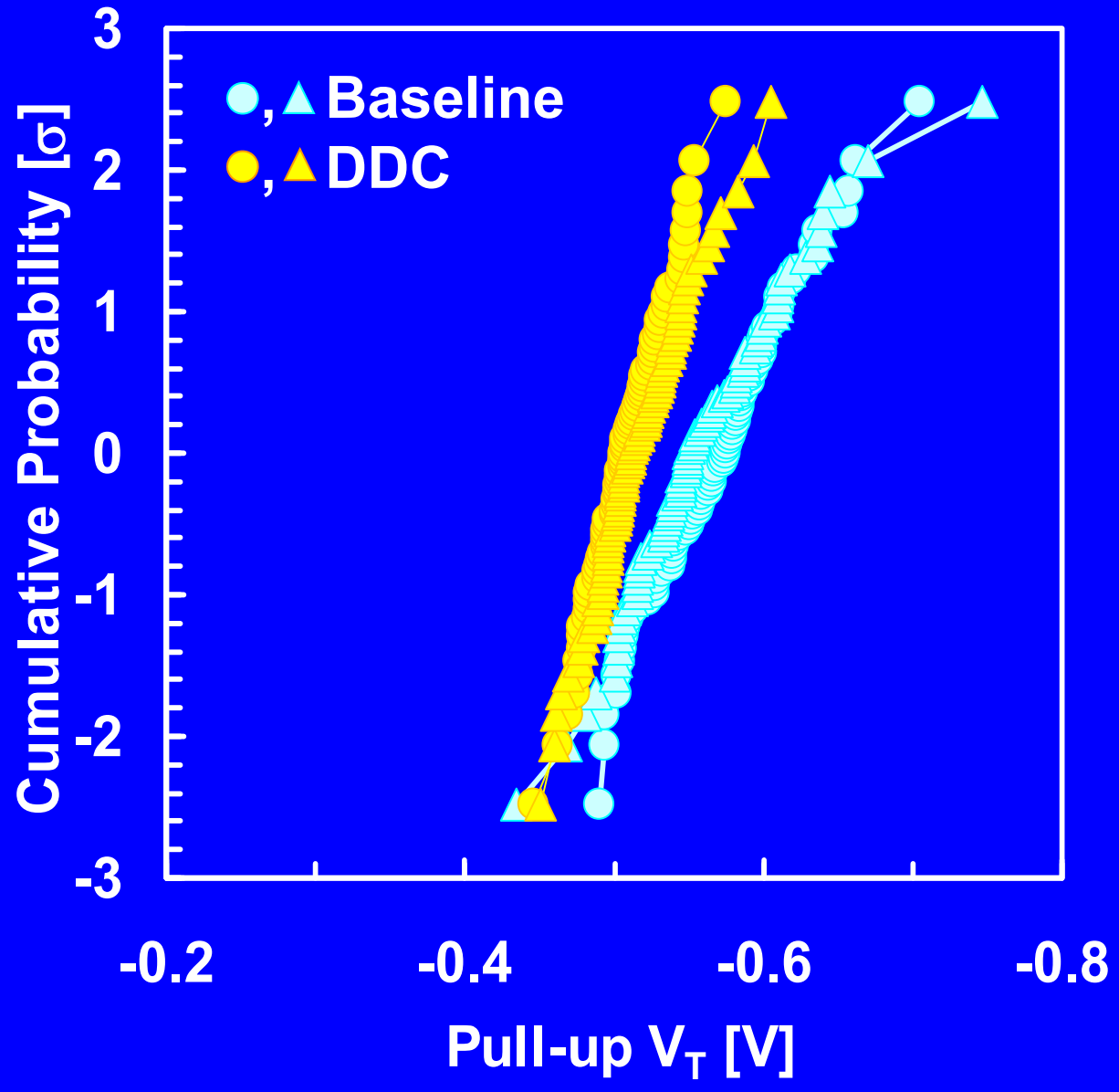
- Excellent distribution of breakdown
- Long enough life time for NBTI
- Long enough life time for HCI

No concern about low temp. GOX

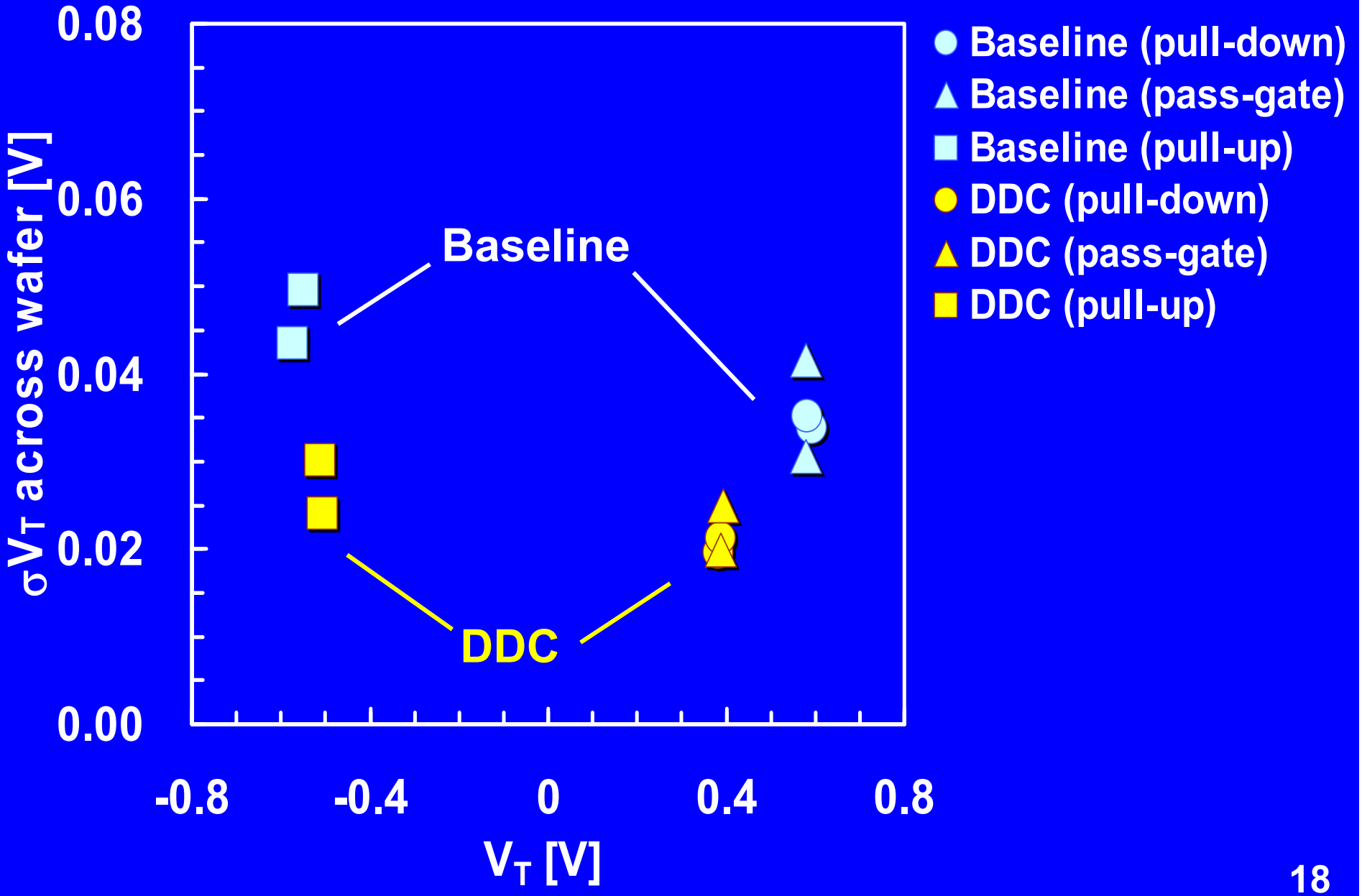
V_T distribution of NMOS



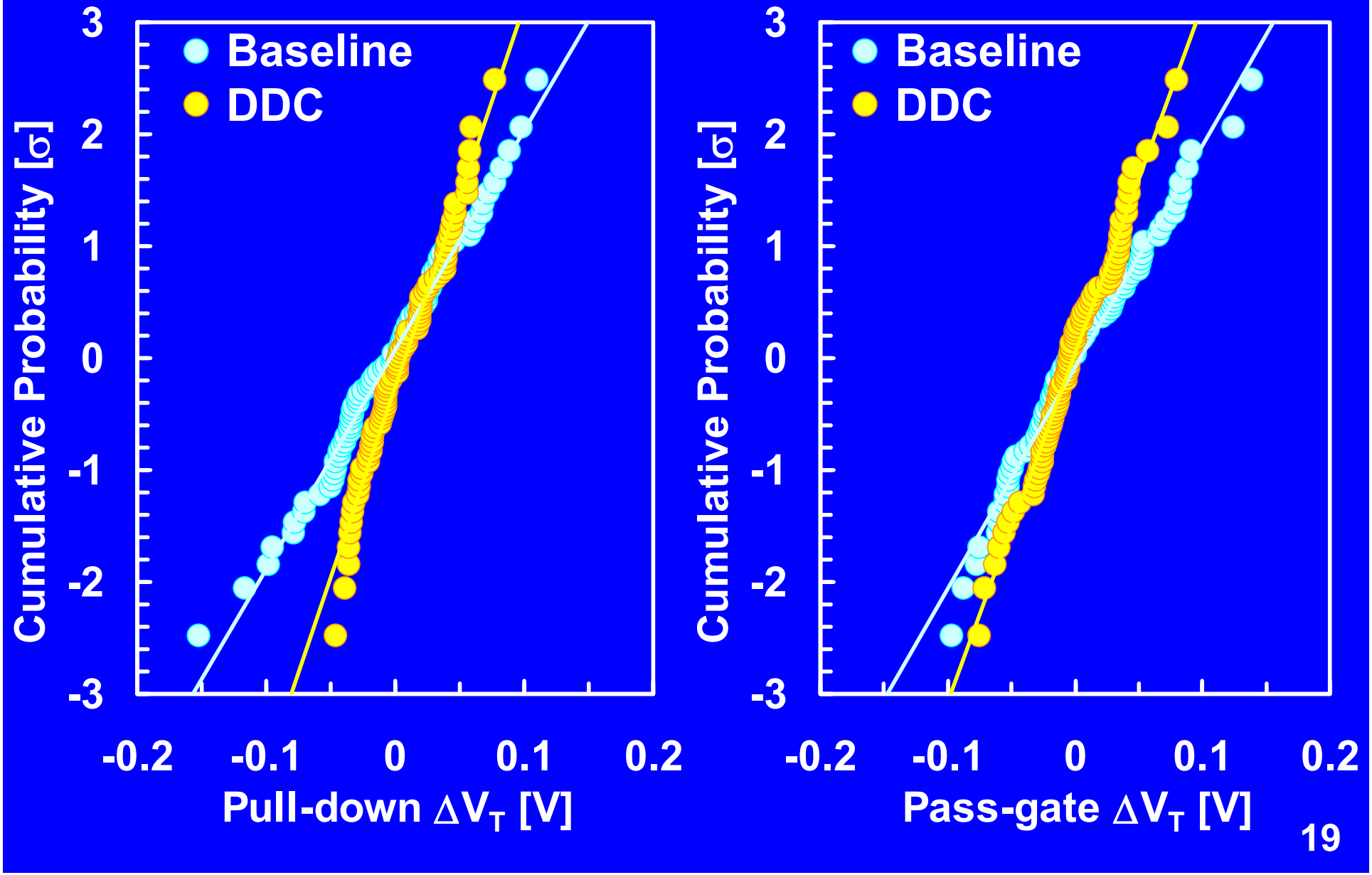
V_T distribution of PMOS



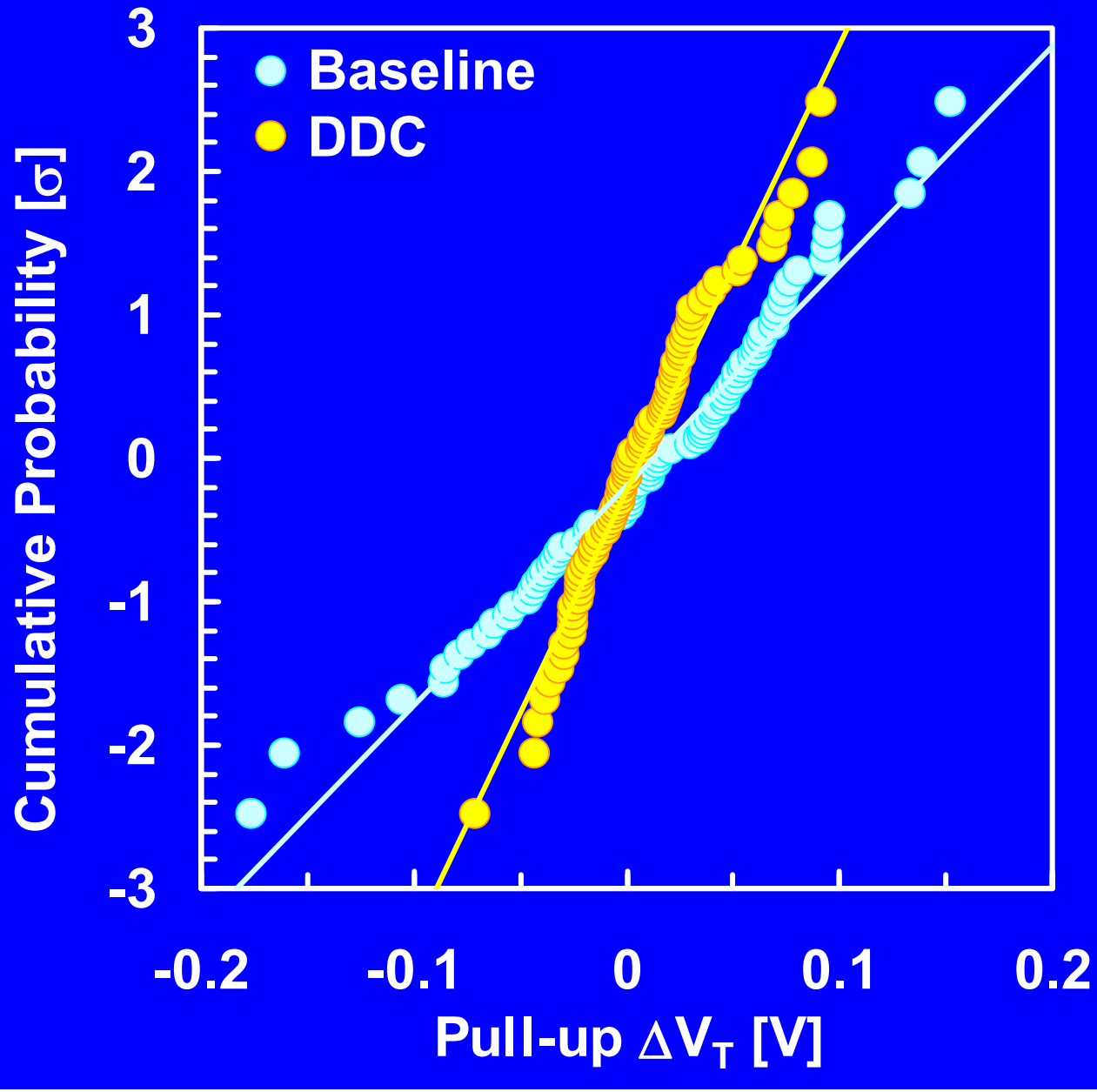
Summary of across-wafer variation



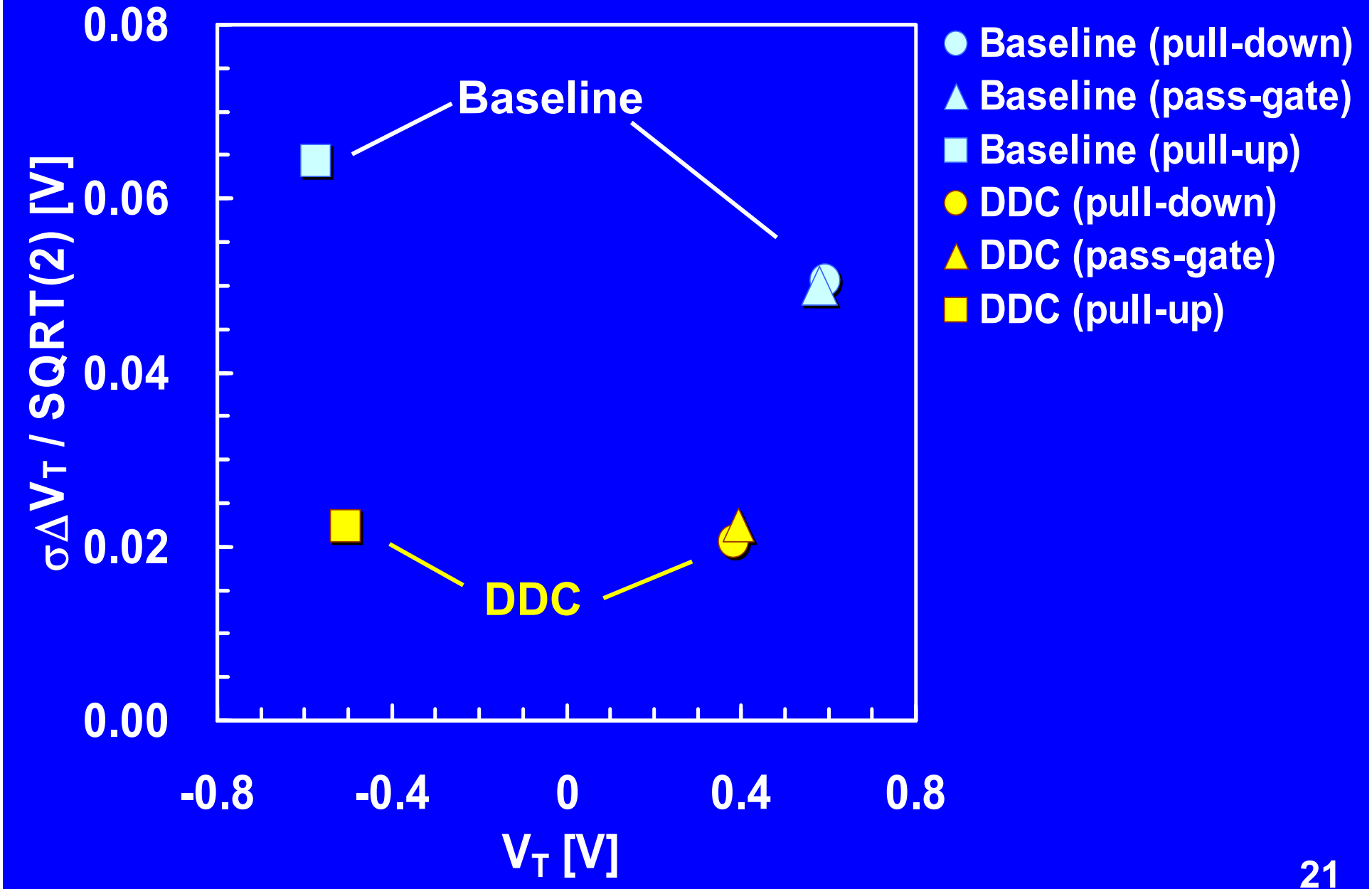
V_T matching of NMOS



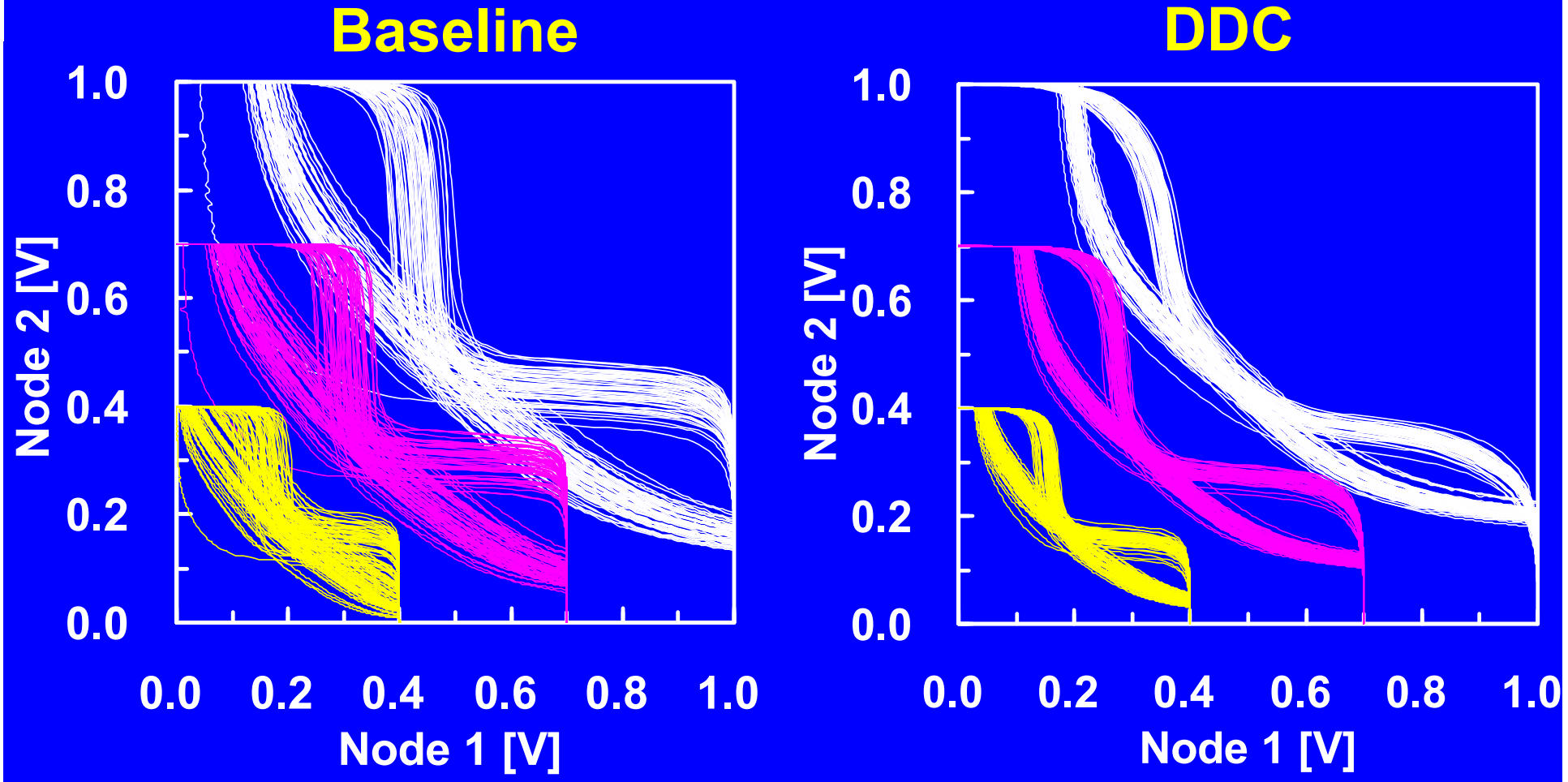
V_T matching of PMOS



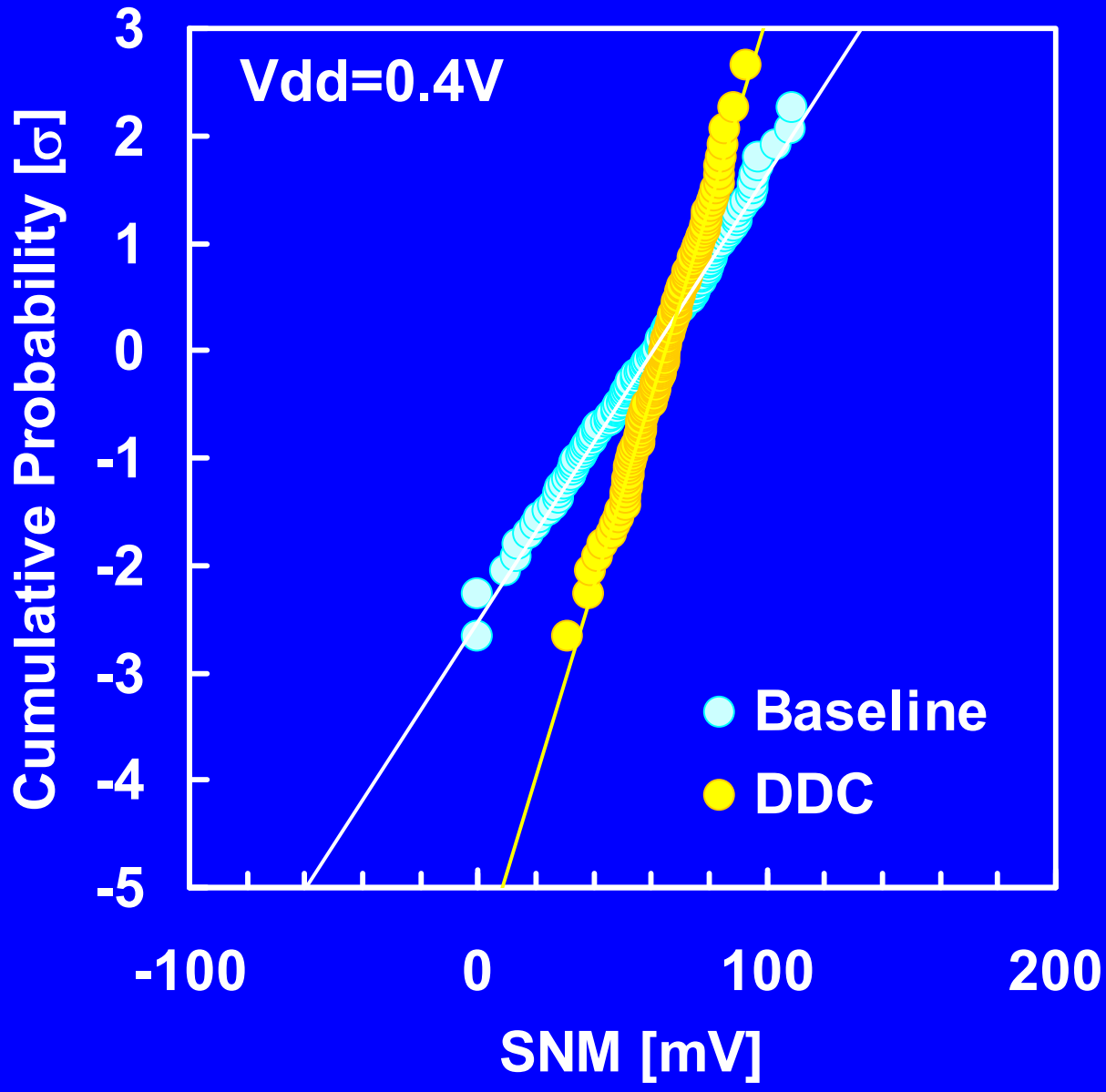
Summary of V_T matching



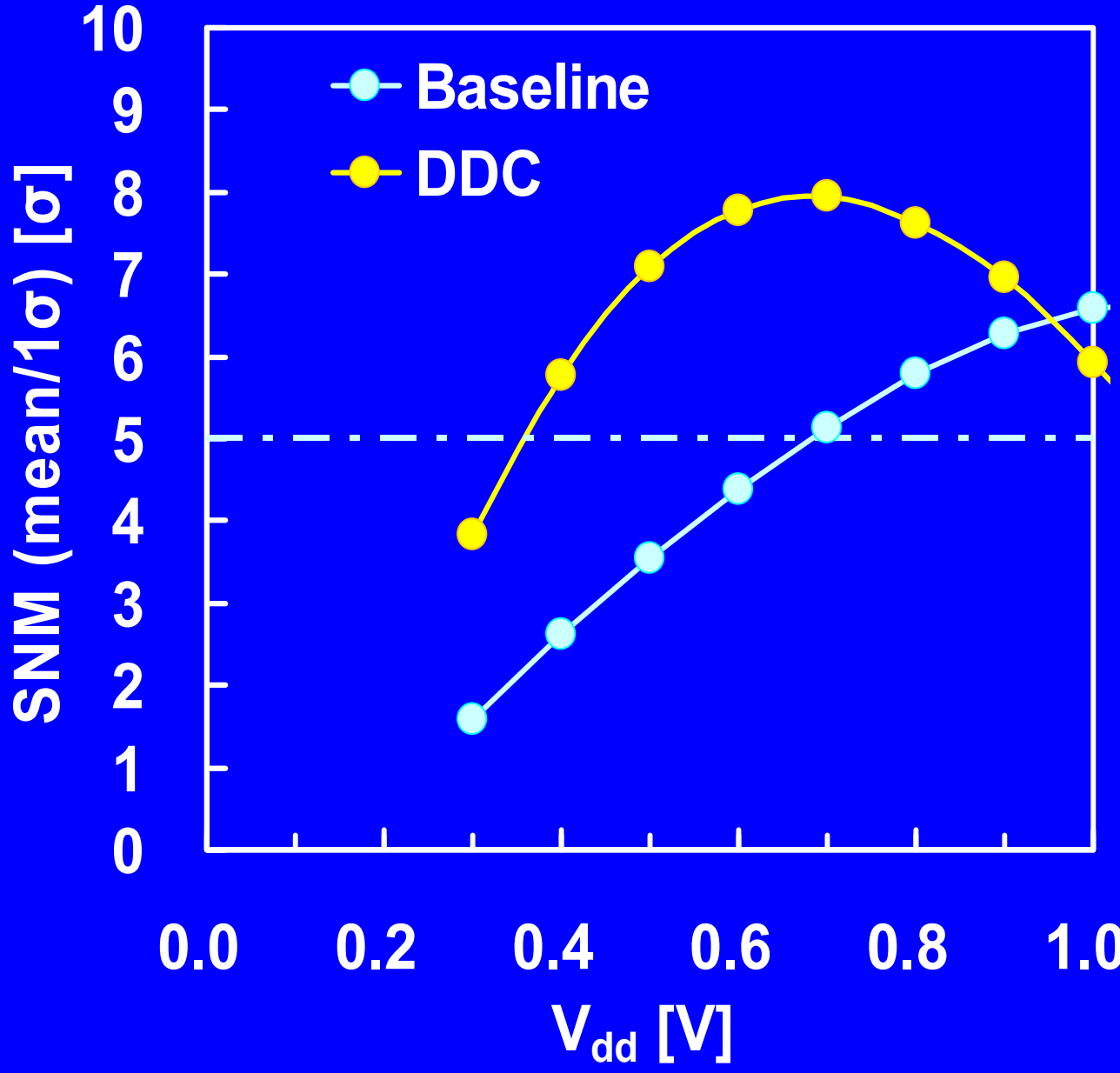
Butterfly curves of 6T-SRAM



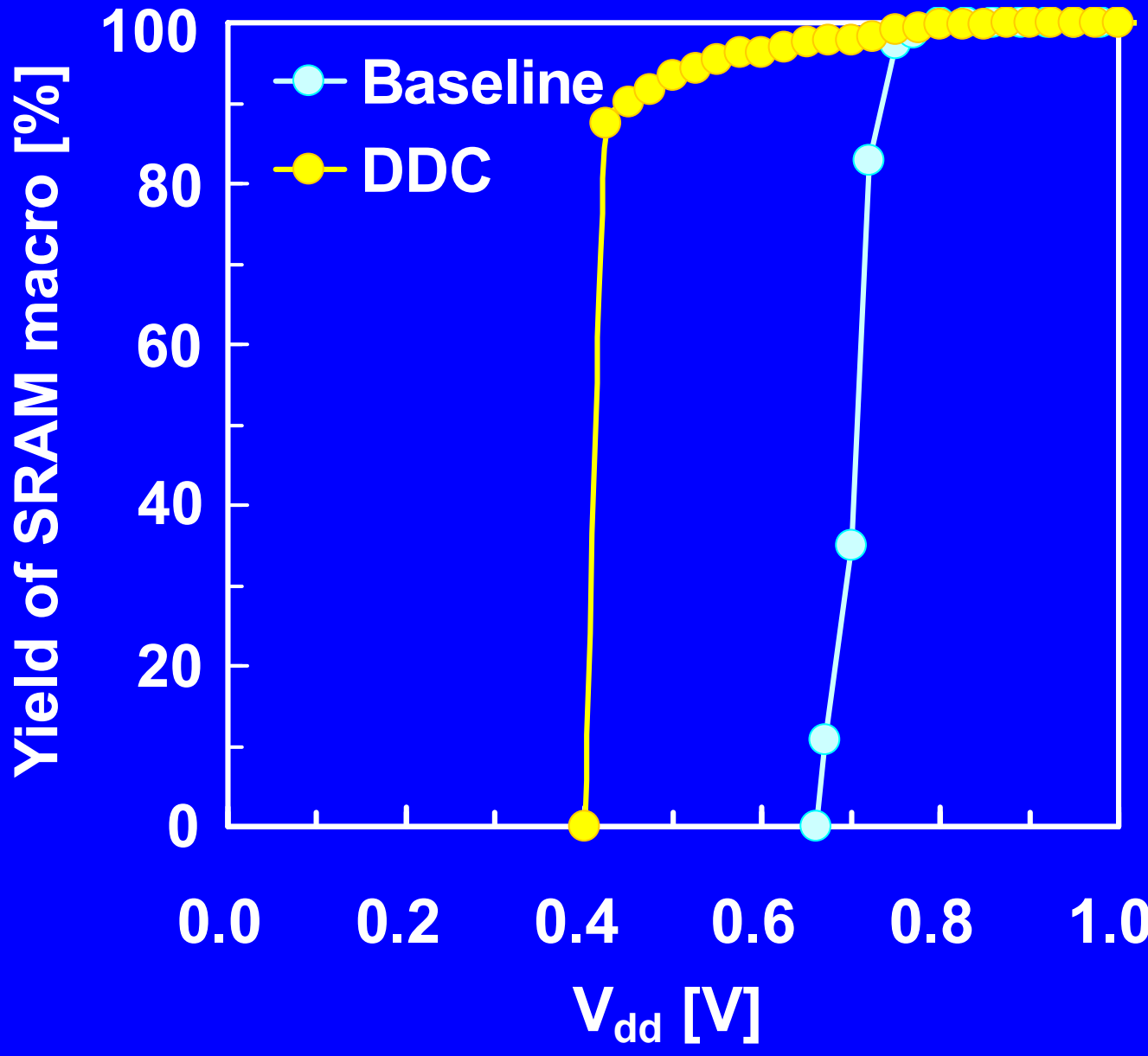
SNM distribution



V_{dd} dependence of SNM



V_{ddmin} of 576K bit SRAM array



Summary

- Deeply Depleted Channel (DDC) transistor has been introduced to reduce RDF.
- Process flow of DDC has been established.
- V_T matching of SRAM has been reduced to less than half by DDC.
- Near to 0.4V operation of SRAM has been achieved.