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Post-K Computer Development, Updates for SC'18

Fujitsu's High-end HPC Development

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- Fujitsu has been leading HPC technologies for over 40 years

K computer

Ranked Top500 No.1 in 2011
Competitive in various fields

AWARDS Gordon Bell Prize

Gordon Bell Prize Finalist (2016)

HPCG No.3(2018)

GRAPH 500 Graph500 No.1(2018)

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PRIMEHPC FX10

PRIMEHPC FX100

Post-K computer

Next Japanese flagship supercomputer under development

Japanese National Project

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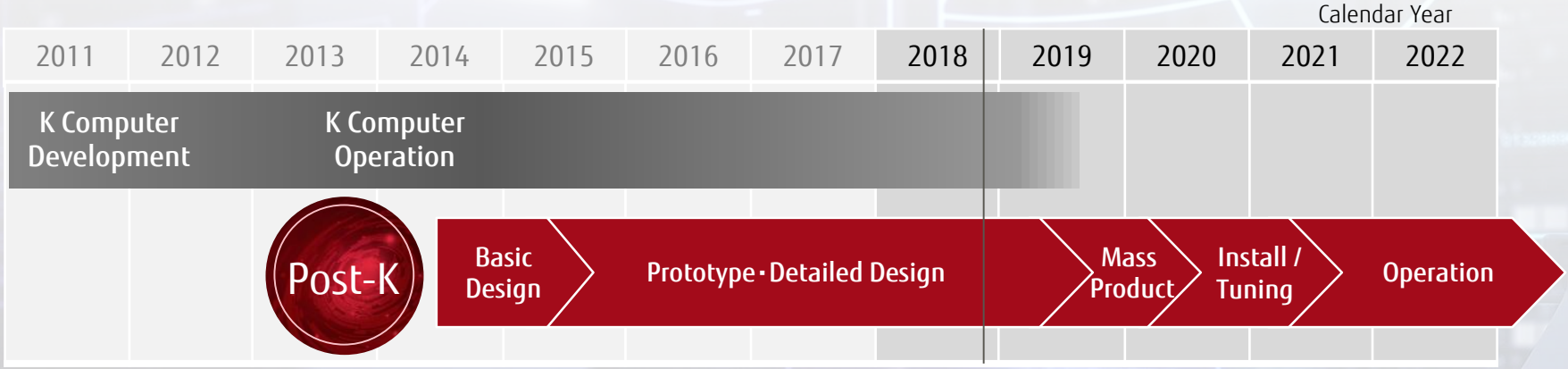
- RIKEN and Fujitsu are currently developing Post-K computer, the most advanced general-purpose supercomputer, in the world



- Post-K computer is optimized to achieve superior performance in real applications as next Japanese flagship system

Post-K Computer Goals and Approaches

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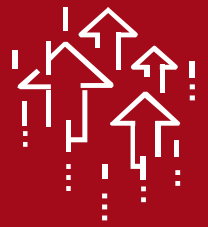

Application performance

Approach

1. A64FX CPU
2. Compiler and Runtime
3. LLIO (Lightweight Layered IO-Accelerator)

A64FX CPU

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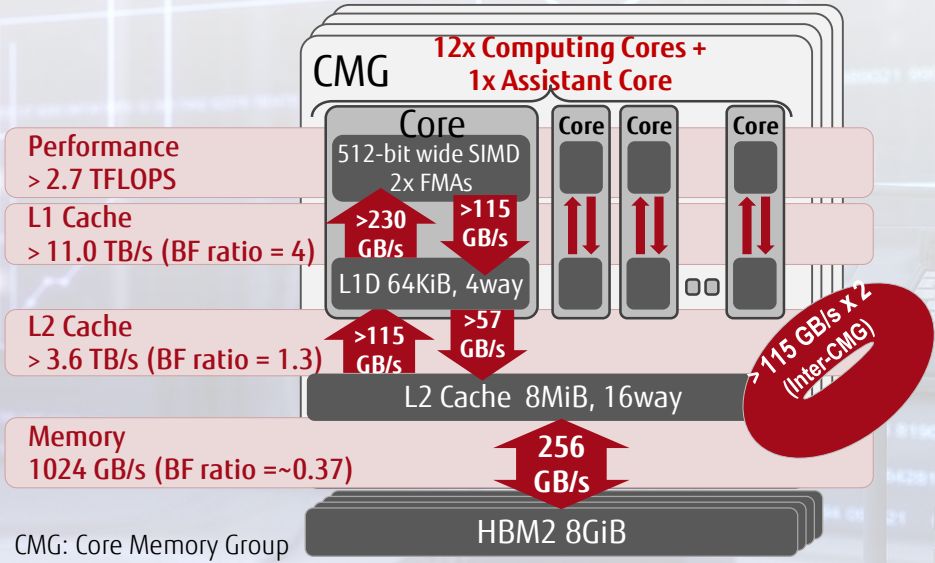
- Achieves high performance in HPC and AI applications
  - Arm Scalable vector extension (SVE), high-bandwidth caches and memory
  - (D|S|H)GEMM and INT (16b/8b) GEMM > 90%, STREAM Triad > 80%

	A64FX (Post-K computer)	SPARC64 VIIIfx (K computer)
ISA (Base + Extension)	Armv8.2-A + SVE	SPARC-V9 + HPC-ACE
Process Technology	7 nm	45 nm
Peak Performance	> 2.7 TFLOPS	128 GFLOPS
SIMD	512-bit	128-bit
# of Cores	48+4	8
Memory Peak B/W	1024 GB/s	64 GB/s



CMG: Core Memory Group

Compiler and Runtime

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- Fujitsu's compiler and runtime libraries exploit the hardware capabilities along three dimensions
  - Support Fortran, C/C++, Python software development environment

	Memory access performance	Computational performance	Thread-parallel performance
Compiler & Runtime	• Software prefetch • Loop-blocking	• Software pipelining with Loop fission • Auto-vectorization with SVE	• CMG & SVE optimized math library • OpenMP 5.0 API & fast barrier
Hardware capabilities	• Hardware prefetch • Stacked memory; HBM2	• Out-of-order • 512-bit SVE	• 48 cores in 4 CMG • Inter-core barrier

Preliminary Performance Evaluation Results

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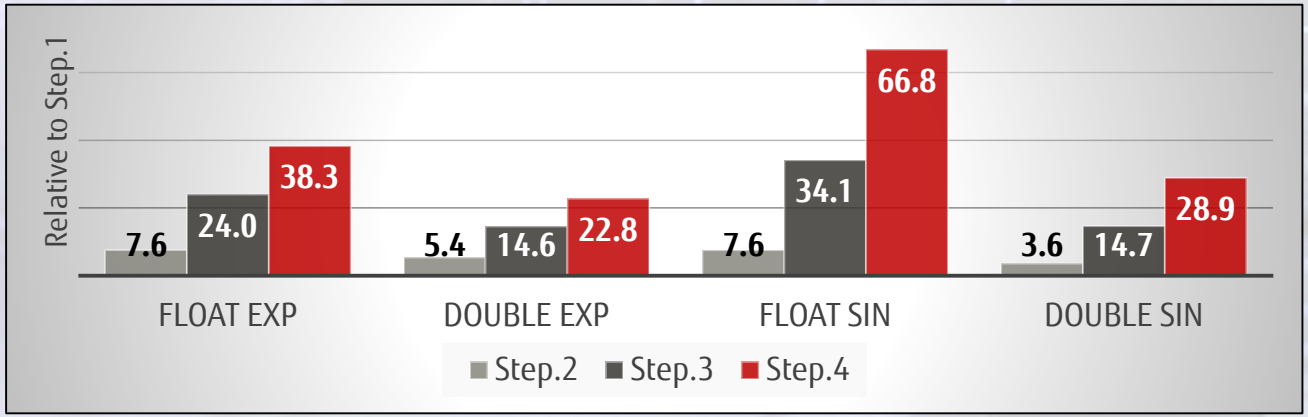
- A64FX's instruction set and compiler achieve high performance on loop of math function
  - **Step 1.** Armv8 coding
  - **Step 2.** + SVE + accel.Instruction coding
  - **Step 3.** + Inlined by compiler
  - **Step 4.** + Applied software pipelining by compiler



LLIO (Lightweight Layered IO-Accelerator)

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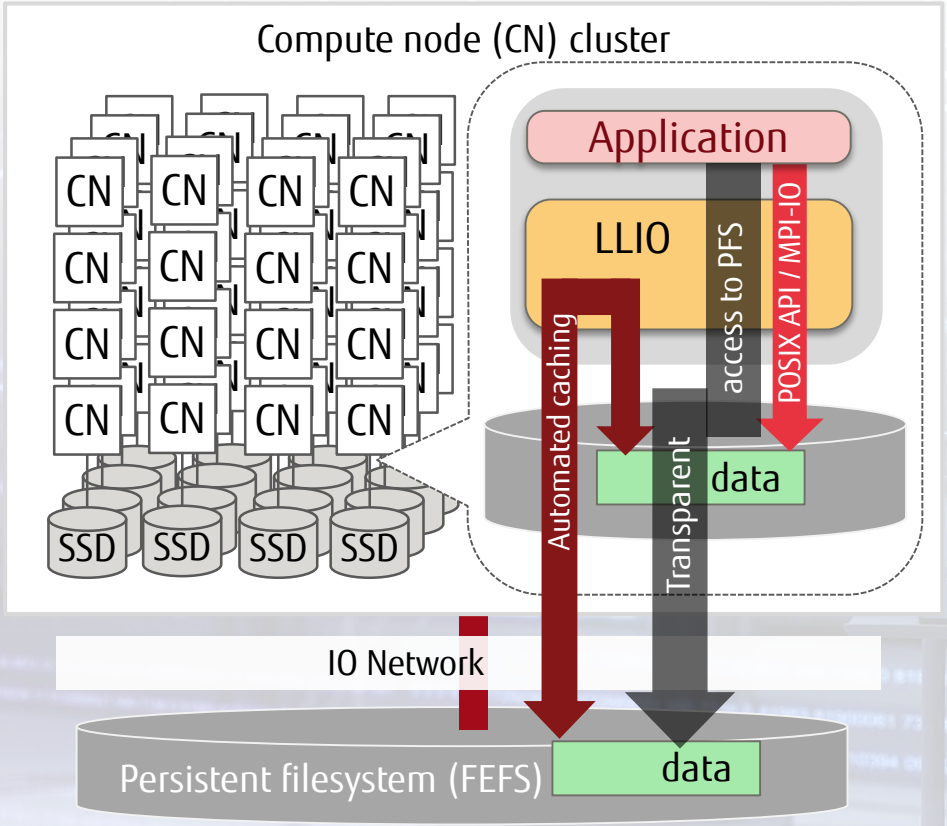
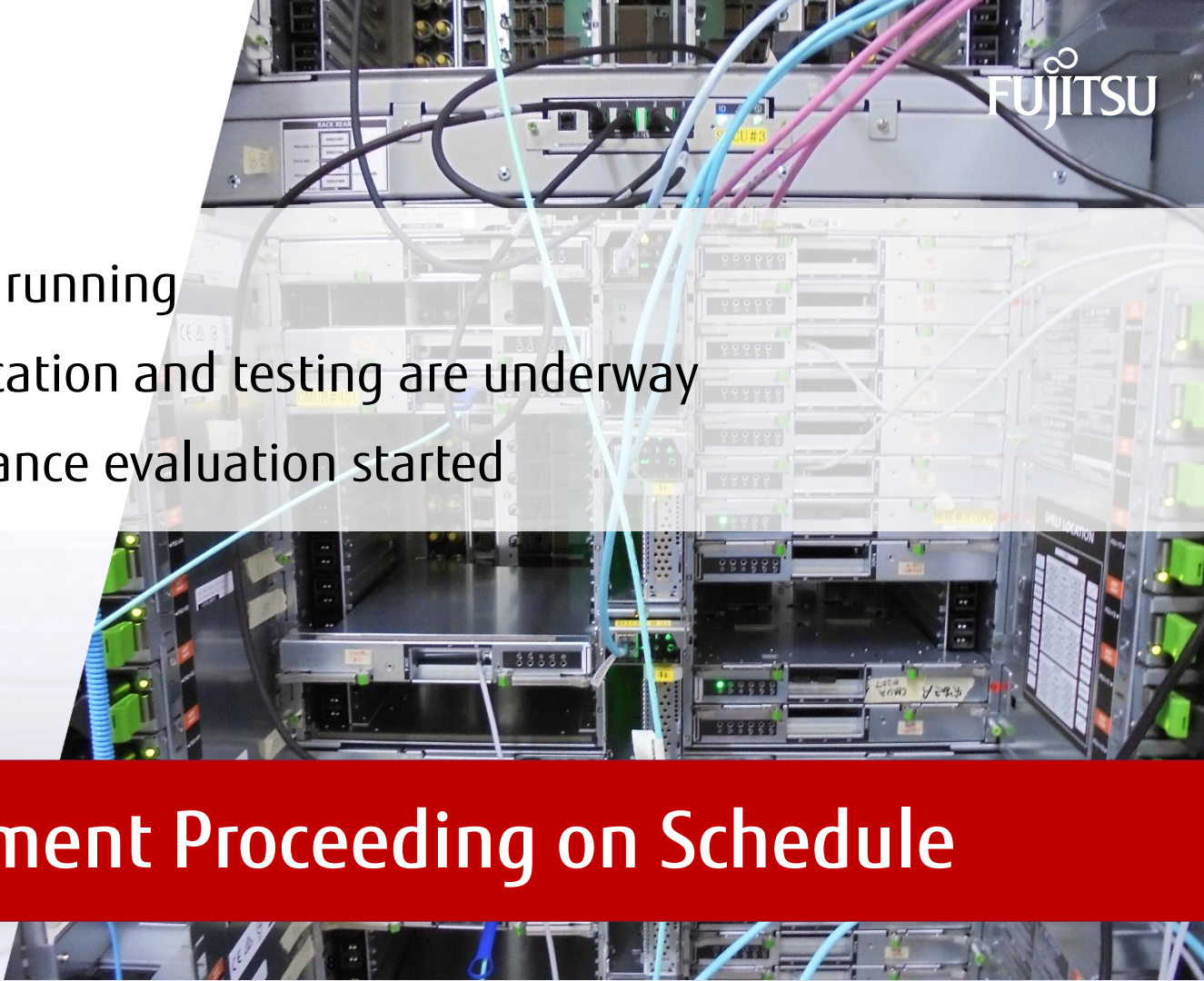
- **Boosts I/O performance w/o modifying Apps**
  - Exploits SSD as a shared cache of persistent filesystem (PFS)
- **Provides two kinds of temporary filesystems for I/O optimization**
  - Shared/Local temporary filesystem



Post-K Computer Current Status

- CPU powered-on, OS running
- System design verification and testing are underway
- Preliminary performance evaluation started



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Development Proceeding on Schedule

Post-K Computer Hardware Features

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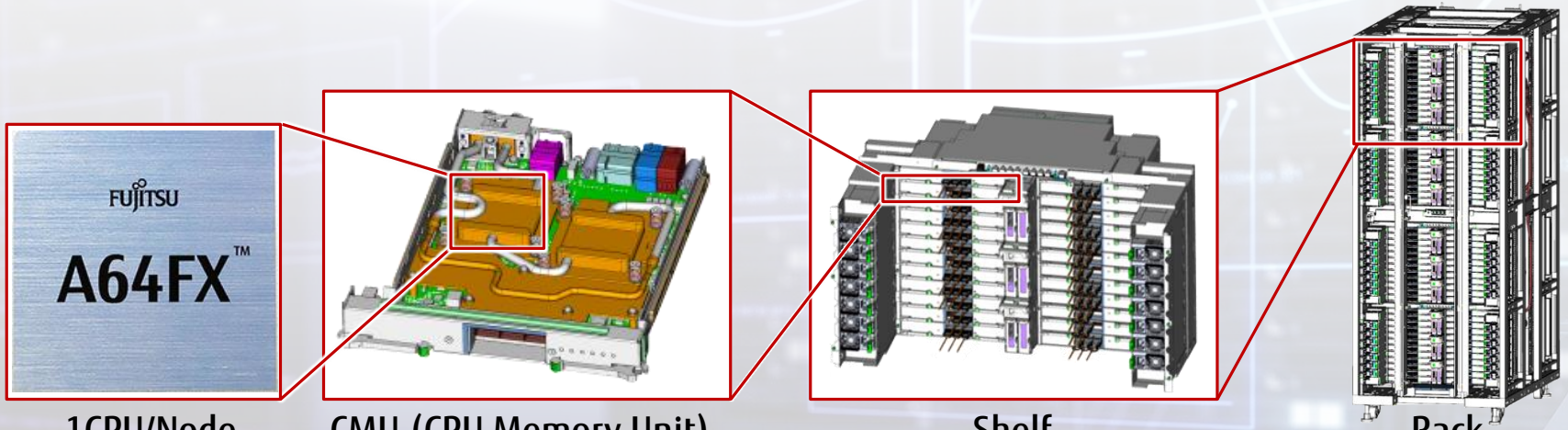
- Post-K computer's high-density mounting achieves over 1 PFlops per rack



1CPU/Node

CMU (CPU Memory Unit)
2 Nodes/CMU

Shelf
24 CMUs/Shelf
(48 Nodes)

Rack
8 Shelves/Rack
(384 Nodes)

(Cont.) Post-K Computer Hardware Features

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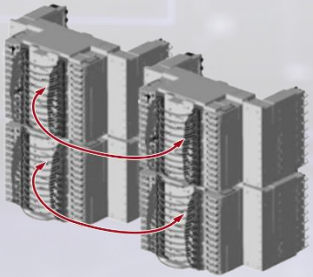
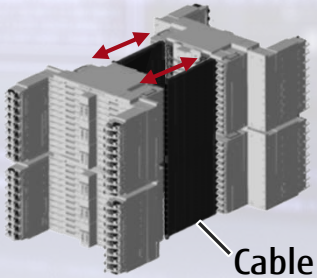
High-density mounting, shortened transmission distance between CPUs

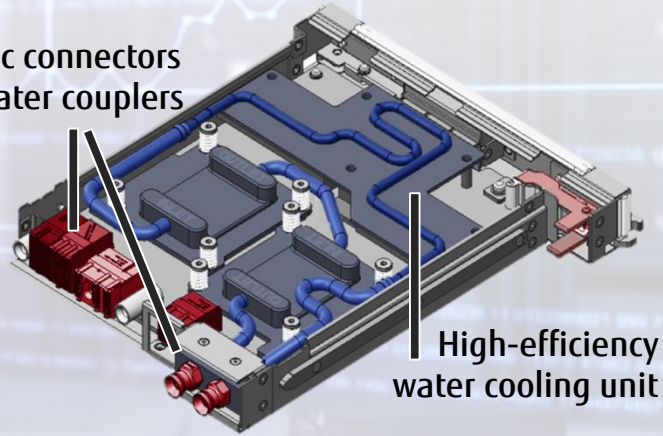
- High-efficiency water cooling unit on the CPU memory unit (CMU) provides 100% water-cooling
- The back-to-back layout and cable box shorten the cables length
- Single action connection of electric connectors and water couplers achieve compact CMU



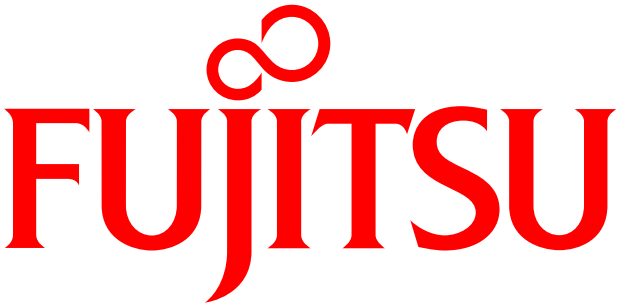
Conventional connection



Post-K computer connection



CMU



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