

Post-K Supercomputer Overview

Post-K supercomputer overview



- Developing “Post-K” as the successor to the K computer with RIKEN
- Developing HPC-optimized high performance CPU and system software
- Selected ARMv8 with SVE ISA for the CPU



Post-K goals and approaches

Goals

High application performance

Good power efficiency

Application portability

Advance from K computer and PRIMEHPC FX series

Good usability for users

Approaches

Develops a custom high performance & scalable CPU

【High performance】 Post-K CPU core design
【Scalability & Power efficiency】 SMaC based Post-K CPU design

Advances system software for Post-K

Optimizes for higher application performance and scalability

Complies with standard specifications for usability and application portability

Post-K CPU core design

- Developing high performance CPU adopting ARMv8 with SVE ISA
 - Contributing to development of SVE (Scalable Vector Extension) with ARM
- Inheriting and enhancing the preceding CPUs' functions

HPC apps acceleration	Post-K	FX100	FX10	K computer
Base ISA + SIMD Extensions	ARMv8+SVE	SPARCV9+HPC-ACE2	SPARCV9+HPC-ACE	SPARCV9+HPC-ACE
SIMD width [bit]	512	256	128	128
Gather Load and Scatter Store	✓Enhanced	✓	-	-
FMA: Floating-point multiply and add	✓	✓	✓	✓
Packed Single Precision SIMD	✓Enhanced	✓	-	-
Math. acceleration primitives*	✓Enhanced	✓Enhanced	✓	✓
Inter-core barrier	✓	✓	✓	✓
Sector cache	✓Enhanced	✓Enhanced	✓	✓
Hardware "prefetch" assist	✓Enhanced	✓Enhanced	✓	✓

*Mathematical acceleration primitives include trigonometric functions, exponential functions, etc.

SMaC based Post-K CPU design

- Improves Fujitsu's proven μ -architecture, SMaC(Scalable Many Core) optimized for HPC applications

SMaC example for FX100

Middle-sized, general purpose, out-of-order, superscalar processor core

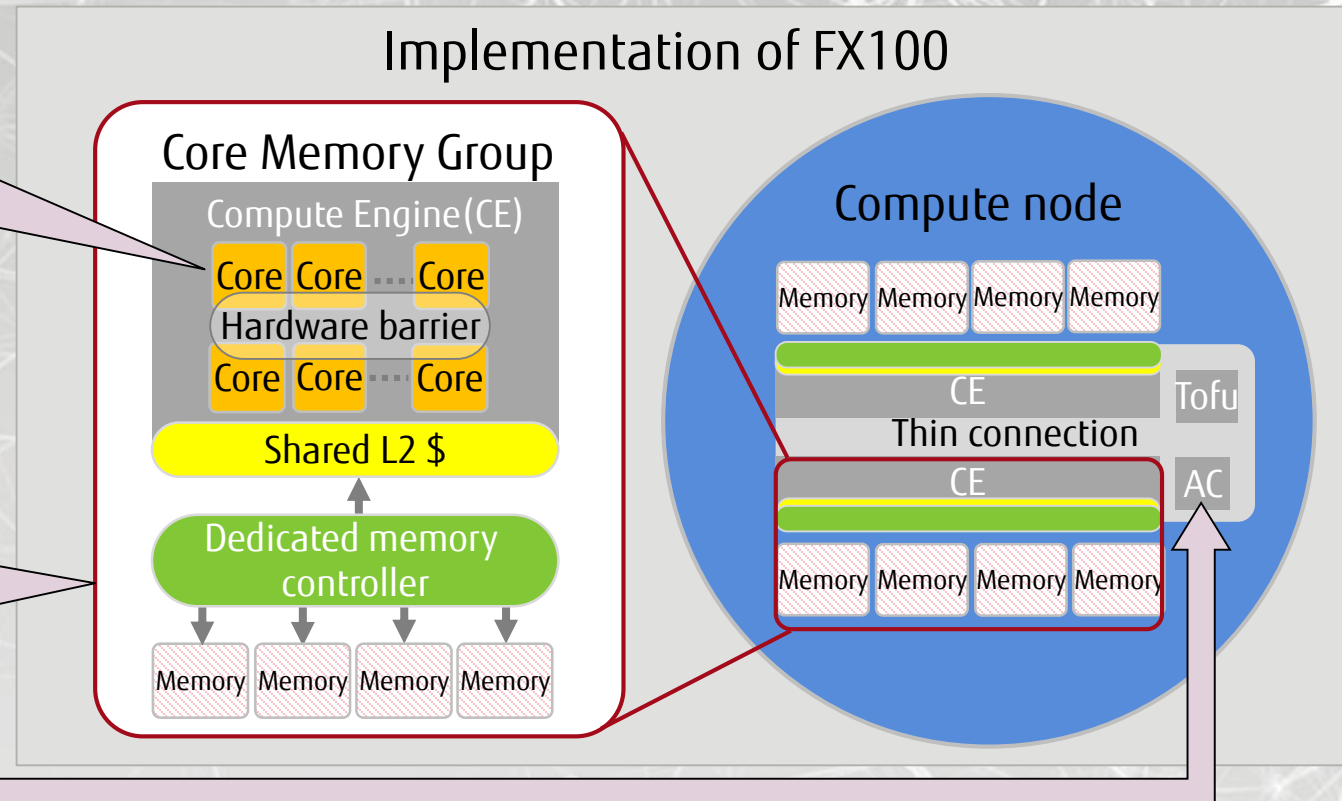
- Good performance for variety of apps
- Low power with power management functions

Assistant core

- OS jitter reduction and assistance for IO, async MPI
- Scalable for massively parallel system

Core Memory Group (CMG), many core building block, ccNUMA thin connection

- Hierarchical structure for hybrid parallel model
- Optimized area and performance



Advanced system software for Post-K

- Developing based on co-design scheme with application developers
- Keeping application portability by providing programming environment

Post-K applications

FUJITSU Technical Computing Suite / RIKEN Advanced system software

Management software

System management
for highly available & power
saving system operation

Job management
for higher system utilization &
power efficiency

Hierarchical file I/O software

Application-oriented
File I/O middleware

Lustre-based
cluster file system
FEFS

Programming environment

XcalableMP

MPI(Open MPI, MPICH)

OpenMP, COARRAY, Math Libs.

Compilers(C,C++,Fortran)

Debugging and tuning tools

Linux OS / McKernel(Lightweight Kernel)



Post-K system hardware

Optimizes for higher application performance and scalability



- Develops HPC-optimized technologies
- Enhances the features of K computer, PRIMEHPC FX10/FX100 systems

Hardware:

- Fujitsu-designed CPU with SVE
- Tofu 6D mesh/torus interconnect

System software:

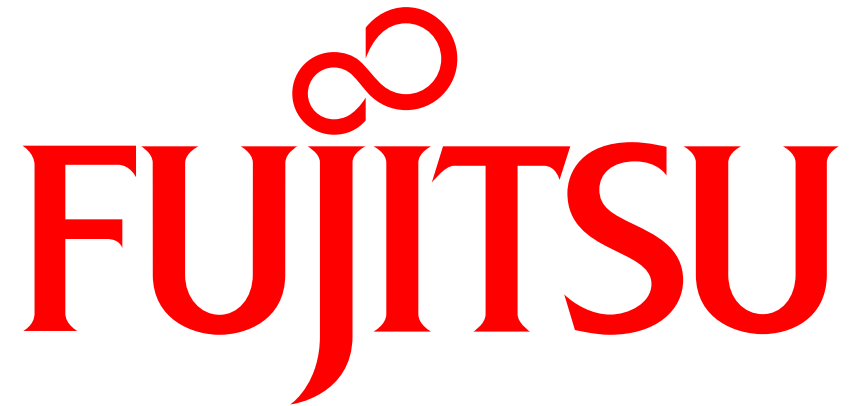
- McKernel with Zero OS jitter
- Distributed file system FEFS
- Parallelizing compilers
- Tuned MPI libs
- Management software

Complies standard specifications for usability and application portability

■ Compliance with ARM standard platform specifications

- To co-operate ARM/Linux community and utilize system software and OSSs
- To ensure binary level application portability

- ISA ARMv8-A with SVE
- System architecture SBSA level3, SBBR
- Firmware interface UEFI, PSCI
- API, library Linux APIs, Standard MPIS
Standard math. libs
- Languages
 - Fully supported: Fortran 2008, C11, C++14, OpenMP 4.5
 - Partially supported: Fortran 2015, C++1z, OpenMP 5.0



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