**SDRAM-I/F-Type 128M-bit Consumer FCRAM™ for System in Package**

**MB81ES123245-10 (X32-bit)**

A 128M-bit Consumer FCRAM™ developed for System in Package (SiP) that offers optimal memory for SiP with programmable page function, BIST function.

* System in Package (SiP)

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### Introduction

Recent emerging growth of digital consumer products such as digital video cameras and digital still camera has been requiring the work RAM realizing higher performance with lower power consumption. In terms of space-saving, SiP that is housing the logic chip and the memory chip in one package has been introduced into the market rapidly. One solution for such a market requirement, FUJITSU has developed a 128M-bit Consumer FCRAM as an optimal memory for SiP.

This product is capable of high-speed data transfer rate up to 432 MB/sec at 108 MHz operation and low power consumption adopted by a programmable page function. Furthermore, FUJITSU original “BIST (Built-In Self-Test) function” simplify memory test after SiP assembly as well as a drastic reduction of external pin count. This product can be offered in FCRAM wafer form in addition to the SiP form together with FUJITSU logic chip.

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### Product Features

- **Low power consumption**
  - FCRAM core technology
    The FCRAM core technology has realized the low power consumption of 63 mW (108 MHz, with 64 pages)*.

  * Calculated at random memory access.

- **1.8 V single power supply**

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Table 1 shows the major features of this product.

- **SDRAM interface**
*Programmable page function*

The programmable page function can reduce active power consumption by optimizing the active memory area. Three steps (256 pages/128 pages/64 pages) of page length is available using the register setting.

Fig.1 shows the comparison of operation current at each page length.

This function is suitable for applications in which small data accesses occur frequently such as image processing and movie processing. In addition, the peak operation current can be reduced by minimizing the active memory area, and noise designing in SiP development can be simplified.

*Deep power-down function*

Deep power-down function achieves lowest standby current with no data retention capability. Power consumption is reduced drastically by turning OFF the internal power supply.

*Automatic temperature compensated self-refresh function (ATCSR)*

In the self-refresh mode, ATCSR function configures refresh interval automatically according to the actual temperature in order to drastically reduce the standby power consumption.

*Partial array self-refresh function (PASR)*

In the self-refresh mode, PASR function reduce power consumption by adjusting the self-refresh area according to the necessary data refresh area. It is possible to set the refresh area in two steps (128M/64M) using the register setting. This function and the above ATCSR function can provide optimal power management for the actual application.

*High-speed data transfer rate*

This product realizes a high-speed data transfer rate of 432 MB/sec (108 MHz, ×32-bit) even with a single chip. It supports a higher transfer rate of 864 MB/sec with two-chip mounting.

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**Table 1** Major Features

<table>
<thead>
<tr>
<th>Product Configuration</th>
<th>1M-bit × 32-bit × 4 banks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (VDD=VDDQ)</td>
<td>1.8±0.1V</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>108MHz (Max.)</td>
</tr>
<tr>
<td>Clock cycle (CK)</td>
<td>CL=3: 9.2ns (Min.), CL=2: 18.5ns (Min.)</td>
</tr>
<tr>
<td>RAS cycle time (RCS)</td>
<td>CL=3: 82.8ns (Min.), CL=2: 9ns (Max.)</td>
</tr>
<tr>
<td>Access time from clock (TAC)</td>
<td>CL=3: 7ns (Max.), CL=2: 9ns (Max.)</td>
</tr>
<tr>
<td>Operation current (IDD1)</td>
<td>256 pages: 60mA (Max.), 128 pages: 45mA (Max.), 64 pages: 35mA (Max.)</td>
</tr>
<tr>
<td>Power-down current (IDD2PS)</td>
<td>0.5mA (Max.)</td>
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<tr>
<td>Burst mode current (IDD4)</td>
<td>CL=3: 70mA (Max.), CL=2: 40mA (Max.)</td>
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<tr>
<td>Self refresh current (IDD6)</td>
<td>TJ=35°C: 200µA (Max.), TJ=95°C: 800µA (Max.)</td>
</tr>
<tr>
<td>Deep power-down current (IDD7)</td>
<td>15µA (Max.)</td>
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<tr>
<td>Junction temperature (TJ)</td>
<td>−25 to 95°C</td>
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<tr>
<td>Refresh characteristic</td>
<td>4K refresh cycle/64 ms</td>
</tr>
</tbody>
</table>

* These are provisional specifications and are subject to change.
Unique testing functions

- **BIST function**
  FUJITSU original BIST circuit, makes it possible to test the memory cell operation after SiP mounting without the external memory pins.

- **WLT (Wafer Level Test) function**
  The WLT function can guarantee device characteristics in wafer form.

- **Self burn-in function**
  The self burn-in function provide dynamic stress test equivalent to the conventional burn-in test by applying the specified voltage level on the specific terminal; it can be used to support high reliability request.

- **Edge pad assignment**
  All pads are assigned on the chip edge which takes advantage for chip stack configuration.

- **Programmable driver size**
  Programmable driver size option is used to adjust the delay time and suppress the output noise problems during high-speed operation. It is also possible to set the driver capacity to four steps (100%/70%/60%/30%) using the register setting.

Future development

This article introduced the 128M-bit Consumer FCRAM for SiP with unique testing functions in addition to low power consumption and high bandwidth for next-generation mobile devices. We will continue to provide memory solutions for market needs.

Fig.2 provides the road map of Consumer FCRAM.

NOTES

* FCRAM is a trademark of FUJITSU LIMITED.