Millimeter-wave CMOS Transceiver Techniques for Automotive Radar Systems

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Recently, advanced driver assistance systems (ADAS) with the keyword of "safety" have attracted attention in the world. Many mega-suppliers (Tier 1) and the others have been carrying out development for safe systems using cameras, lasers, and millimeter-wave radar to realize a self-driving system in the near future. Fujitsu Laboratories has been developing millimeter-wave monolithic microwave integrated circuits (MMICs) and modules for automotive radar systems, and is now interested in MMICs based on complementary metal oxide semiconductors (CMOS). In this paper, we describe millimeter-wave amplifiers and a 4-ch transmitter based on accurate device measurement and modeling techniques using the on-wafer calibration method. A phased locked loop (PLL) which operates at 0.96 GHz/μs, the world's fastest modulation speed, is also discussed.

1. Introduction

Automotive radar systems are regarded as one of the key components to realize a self-driving car. This is required for avoiding collisions and detecting blind spots. As is well known, there are some radar systems using image sensors with camera technology and infrared sensors, and so on. While millimeter-wave radar has a great advantage in the case of night-time driving and adverse weather conditions compared with those of other radar systems, the millimeter-wave circuitry requires semiconductor devices to operate at high frequencies. Therefore, compound semiconductor device technologies, such as gallium arsenide (GaAs) and silicon germanium (SiGe), are utilized for conventional radar products. However, recently, there has been rapid and remarkable progress in the silicon complementary metal oxide semiconductors (Si-CMOS) technology. Especially, the performance of digital circuits is becoming comparable to that of a compound semiconductor. A transceiver circuit integrated with CMOS technology is expected to provide a system that can be mass produced at a low cost. Therefore, several results with a CMOS transceiver in the 77 GHz and 78–81 GHz band have been reported. For a broader field of view, the azimuth detection accuracy is important because more targets may be in the expanded detection area. An electric beam scanning radar system is already on the market, but a higher resolution scanning radar system is not yet available.

In this paper, we describe our latest millimeter-wave CMOS transceiver techniques for an automotive radar. The performances of radio frequency (RF) building blocks, phase-locked loop (PLL) for fast-chirp modulation, and multi-channel transmitter ICs are shown and discussed.

2. Millimeter-wave CMOS

In sub-millimeter waveband monolithic microwave integrated circuit (MMIC) designs, an accurate transistor model is required because the small differences in parasitic capacitances and the inductances between the model and actual device have a large impact on the MMIC characteristics. Actually, a capacitance of 1 femto farad (fF) causes a phase shift of about several degrees at 100 GHz and results in the amplifier performing poorly due to an impedance mismatch in the multi-stage amplifier. In this situation, a de-embedding technique that extracts the device under test (DUT) from the test pattern including the pad and the lead line is a key point.

To extract the DUT characteristics from the test pattern, the reported and well-known de-embedding

method is generally used. However, this method has a serious de-embedding error in sub-millimeter waveband MMIC design because the dimensions of the proving pad occupied several tens of square micrometers and this was not considered. The de-embedding error described here causes a serious phase shift on the matching network in the sub-millimeter waveband and cannot be ignored. Therefore, accurate de-embedding of the error term is necessary. For this purpose, we employ the on-wafer transmission reflection line (TRL) calibration method.

Figure 1 (a) shows the test pattern for the on-wafer TRL calibration. This calibration method utilizes the Open, Short, Thru/Line, and DUT TEG patterns, respectively. These patterns must be formed on the same wafer with the DUT to be modeled. The pad and the lead line shown in Figure 1 (a) use the same pattern for the DUT as in **Figure 1**. After measuring the S-parameters of these calibration patterns, all error terms can be calculated correctly and de-embedded.

Next, we measured the transistor TEG and the test patterns for the calibration on a 65 nm CMOS wafer. The measured frequency is from 240 GHz to 320 GHz. As can be seen in **Figure 1 (b)**, the traces of S_{11} and S_{22} show reasonable curves based on the general small signal equivalent circuit of the transistor. We also calculated the maximum available gain (*MAG*) and maximum achievable gain (G_{acv}) defined in equation (1)–(3), respectively.

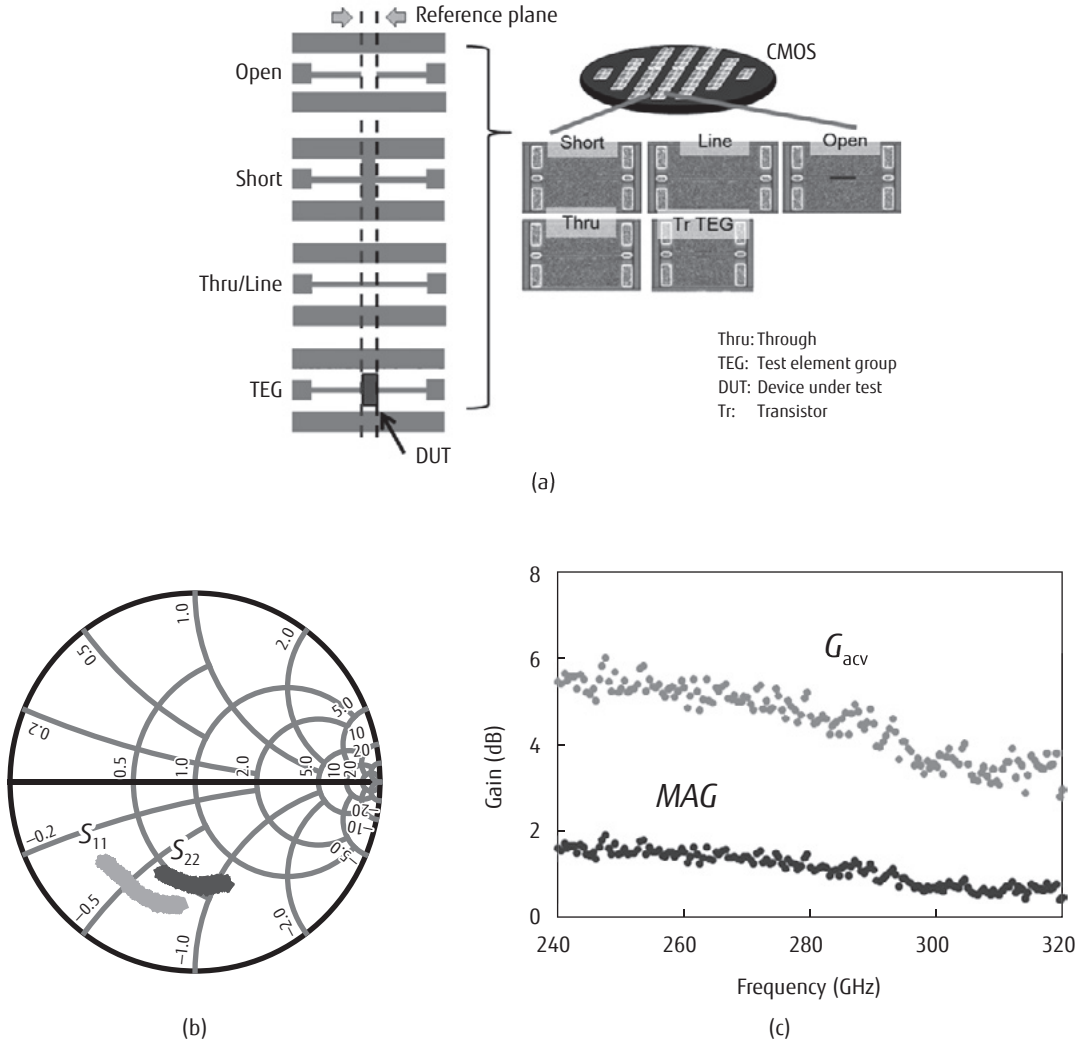


Figure 1
(a) Calibration patterns on CMOS, (b) S-parameters, (c) maximum available gain and achievable gain.

$$MAG = \frac{|S_{21}|}{|S_{12}|}\left\{K-(K^2-1)^{1/2}\right\} \quad (1)$$

$$U = \frac{|Y_{21}-Y_{12}|^2}{\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22})-\mathrm{Re}(Y_{12})\mathrm{Re}(Y_{21})} \quad (2)$$

$$G_{acv}=2U-1+2\{U(U-1)\}^{1/2} \quad (3)$$

As can be seen in **Figure 1 (c)**, a maximum oscillation frequency F_{max} of more than 320 GHz is obtained. If we can neutralize the feedback capacitance, a gain of 3 to 6 dB in the measured band can be expected. Therefore, amplifier operation up to 320 GHz can be expected.

3. Millimeter-wave circuitry

Next, we describe the millimeter-wave power amplifier design. An accurate transistor model plays the key role when designing millimeter-wave circuits. However, the general BSIM (Berkeley Short-channel IGFET Model) 4 models provided by a foundry do not support such a high frequency band. Thus, in this work, we have employed a customized transistor model. Additional inductance, capacitance and resistance elements were added to the BSIM4 model provided by a foundry. The measured and simulated results of the transistors are shown in **Figure 2 (a)**. The unit finger width of the transistor was 1 µm. The measured MAGs in several bias conditions are shown in the figure, and there is a good agreement between the measurements and simulations. The measured MAG biased with 0.75 V for a gate and 0.8 V for a drain was 8.8 dB at 79 GHz and this is a good performance in 65 nm CMOS.

Generally, in a CMOS transistor there is a large capacitance between the drain and source compared with that of a compound semiconductor. The large output capacitance causes an RF signal loss in a lossy Si substrate and decreases the output impedance. The output matching network of the amplifier and the trace of the network on a Smith chart are shown in **Figure 2 (b)**. In this case, the output matching circuitry is 1st order L-C low pass filter network to match the optimum impedance from 50 Ω. The efficiency of the output matching circuitry is described in equation (4), where Q_L and Q_m are quality factors of the passive device and matching network, respectively.

$$\eta = Q_L / (Q_L+Q_m) \quad (4)$$

Here, Q_m means the ratio of the real part and imaginary part of impedance at each point on the Smith chart. As shown in the equation, if we assume Q_L is constant, the loss of the matching circuitry increases as the gate width W_g of the transistor increases. This is because Q_m increases with W_g. As is well known, in a typical CMOS process, Q_L is around 15. Therefore, if the loss of an output matching network keeps within 1 dB, Q_m should become less than 1. For that purpose, the gate width of the transistor in the final stage is several tens of µm. The circuit schematic of an 80 GHz power amplifier is shown in **Figure 2 (c)**. To obtain 10 mW-class output power, a gate width of more than 100 µm is needed. Hence, a power amplifier using four-way power combined with 40 µm of the unit amplifier is designed. The loss of output matching circuitry can be made to be less than 1.5 dB at 80 GHz. **Figure 2 (d)** shows the measured output power and power added efficiency (PAE) with peak power and PAE of 11.5 dBm and 13.6%, respectively. As shown in the figure, the measurement and simulated results are in very good agreement. Therefore, the accuracy of the transistor model is demonstrated.

4. Fast-chirp Modulation PLL

In this section, we describe the low-noise PLL circuitry for the radar core system. Usually, radar utilizes the frequency modulation continuous wave (FMCW) method to detect both the distance and velocity of the targets. However, the linear fast-chirp pulse compression radar system has a unique performance as high-resolution radar. The waveform of the transmitted signal frequency is a pulsed shape with high-speed modulation. The transceiver architecture is similar to the FMCW radar system. The received signal is demodulated with the transmitted signal to produce a beat signal. Its beat frequency (f_b) is proportional to the target range R. Then the target range R is calculated by the following equation,

$$R = cf_b/2K_c \quad (5)$$

where, K_c [Hz/s] is the frequency chirp rate. Notably, the principle of target detection is different from the conventional FMCW radar system. In the fast-chirp pulse radar, the Doppler frequency is negligible, because the chirp rate is sufficiently high. Therefore, the target is identified with only range calculated by equation (5). This is an advantage compared to the FMCW radar

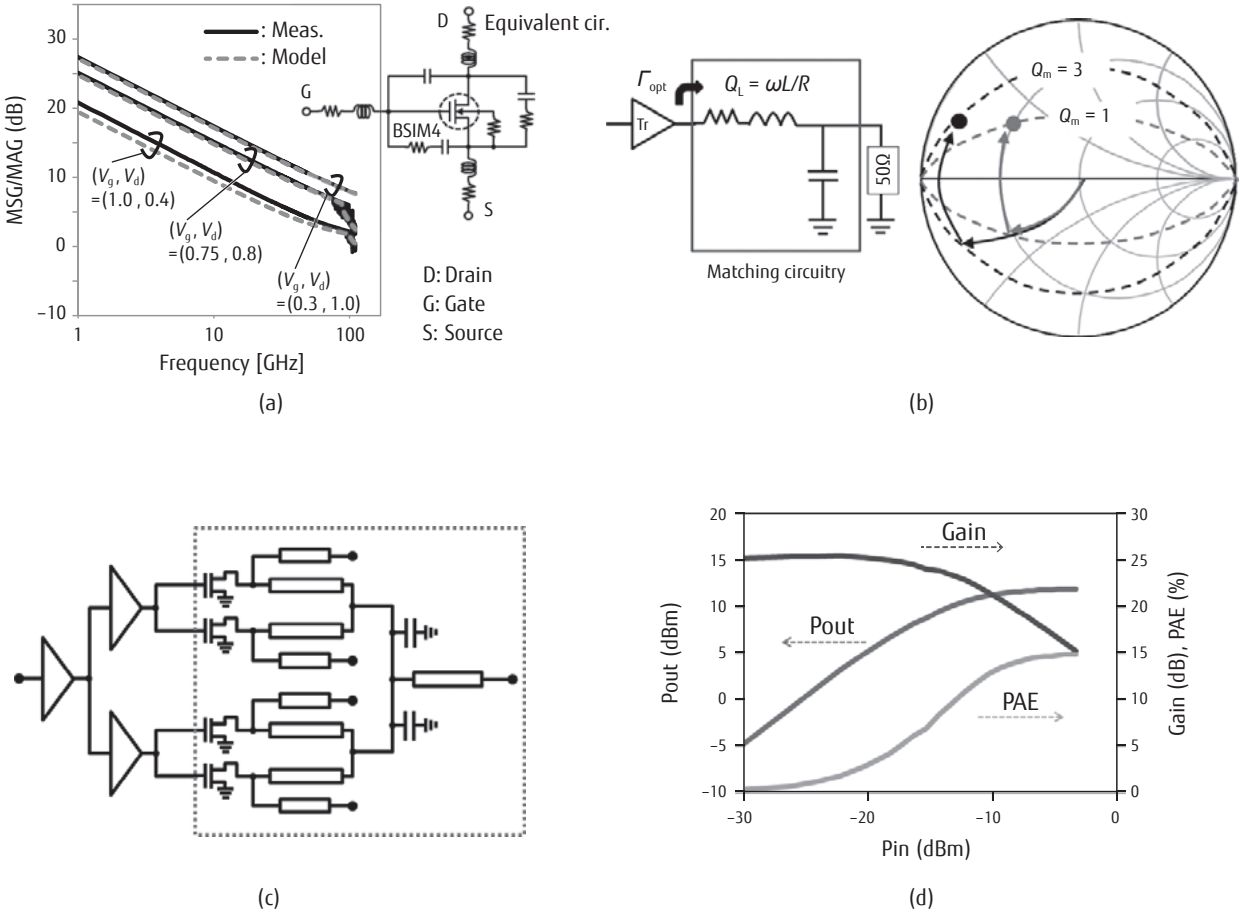


Figure 2
(a) Measurement and simulated results, (b) impedance trace on Smith chart, (c) PA schematic, (d) measured results of PA.

system. FMCW radar has a critical ambiguity in multi-target identification, which is caused by the Doppler effect.

PLL frequency synthesizer architecture with high-speed control circuits is proposed for the fast-chirp pulse generator, as shown in **Figure 3 (a)**. In this architecture, the generator outputs a 40 GHz chirp signal. For automotive radar applications, the transmission and local signals can be obtained with frequency doubling. The generator consists of a 40 GHz voltage-controlled oscillator (VCO), high-speed counters, a phase comparator, a 100 MHz crystal oscillator, an on-chip loop-filter and an integrated high-speed frequency controller. For fast-chirp pulse generation, the high-speed counters are important blocks. High-speed performance is also required for the frequency controller. It consists of a frequency code word generator and a delta-sigma modulator, which operate with a 200 MHz clock. The FCW generator outputs the 33-bit frequency code word in every clock cycle. In order to achieve a high chirp linearity, the quantization error should be reduced sufficiently. For that purpose, a multi-stage noise shaping (MASH) structure is used. The MASH provides high-order noise shaping performance with narrow bit-width accumulators.

For fast-chirp generation, the high-speed programmable counter is the most important circuit block. A pulse-swallow topology is used for high-speed operation, as shown in **Figure 3 (a)**. It consists of three blocks: the dual modulus prescaler, the pulse counter, and the swallow counter. The pulse and swallow counter operate in an auxiliary manner to control the prescaler's modulus. The dual modulus prescaler was designed with current mode logic (CML) circuits, and it consists of a D-flip flop and two and-gated D-flip flops. It employs a multi-modulus topology with cascading

2/3 dual modulus prescalers. To minimize the delay of controller in prescalers, all of the circuits are designed based on high-speed CMOS logic.

The PLL was implemented in 65 nm CMOS process technology. The chip micro photograph is shown in **figure 3 (b)**. The chip has three output terminals that generate a 40 GHz signal, in which one is for high-power use and two are for low-power use. The chip area is 1.87 mm × 3.39 mm. The measured transient response of the generated frequency is shown in **Figure 3 (c)**. The chirp rate was 0.48 GHz/μs in this case, and the maximum chirp rate with linearity was 0.96 GHz/μs. The standard deviation of the frequency error showed 1.21 MHz-rms, as shown in **Figure 3 (d)**. To our knowledge, that result is a record for the modulation speed of PLLs.

5. 4-ch Active phased array

In this section, we discuss the 4-ch transmitter for the active phased array system in which a millimeter-wave beam can be formed and steered electrically. The block diagram of the transmitter and the chip photo are shown in **Figures 4 (a) and (b)**, respectively. The input RF signal with a frequency of 40 GHz is input and doubled by the frequency doubler. The signal is up-converted to 80 GHz, divided by 1 : 4 using a Wilkinson divider and provided to a phase shifter in each channel. All of the biases for the circuits are provided by multi-channel DACs. The temperature sensor and the power detectors are implemented in the MMIC to sense the conditions of the MMIC. The power consumption for the operation of all channels is 0.62 W. The measured saturated power is 7.8 dBm, when the input power at 40 GHz is -20 dBm.

To control the phase of the output signal, the monitor function for the phase in each channel is needed. For that purpose, we designed and implemented a phase detector mixer in the chip. The mixer is comprised of two double balance mixers which have a symmetrical layout. When the input signals with the same frequency and different phases are input, DC bias voltages are output from the output terminals. **Figure 5**

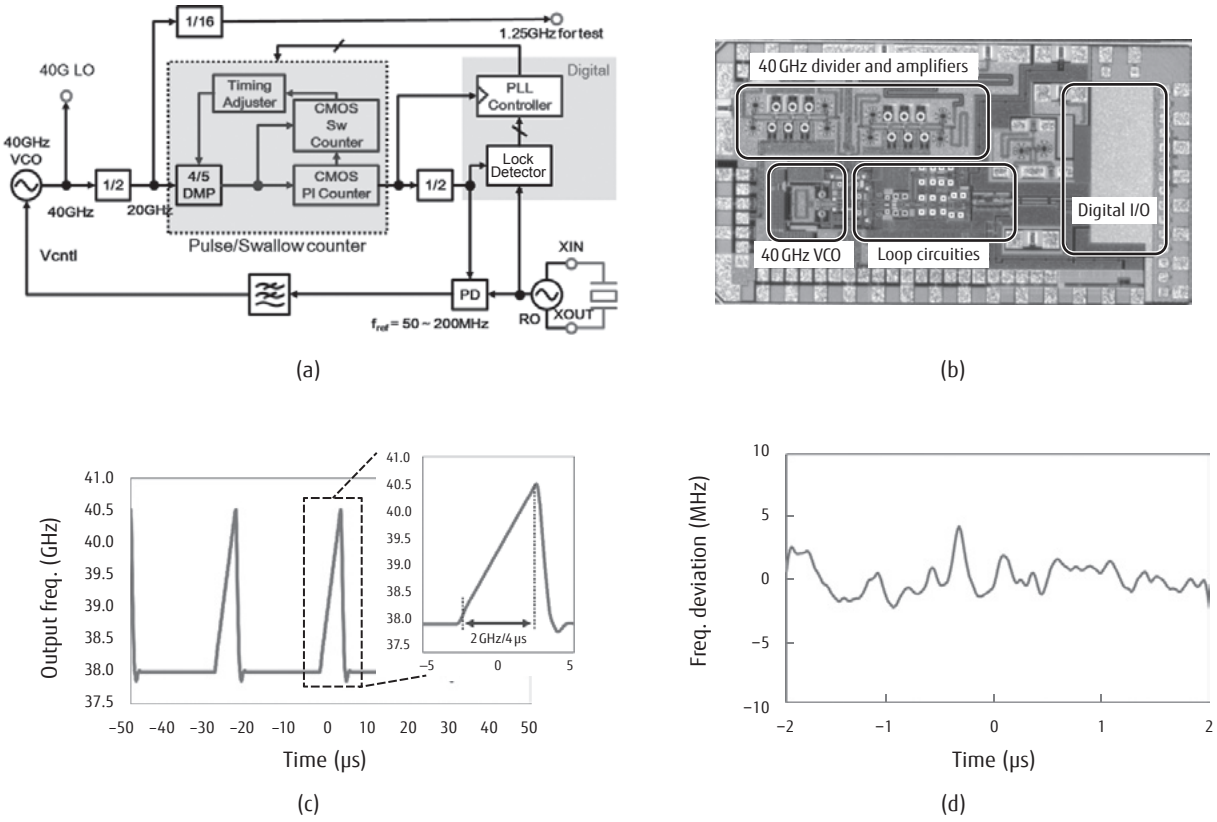
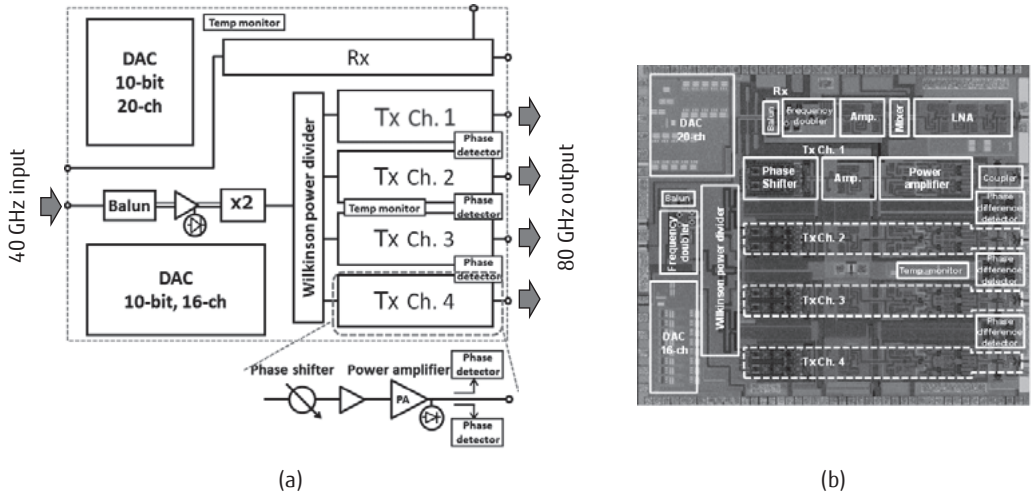


Figure 3
(a) PLL block diagram, (b) chip photo, (c) measurement result, (d) linearity result.



(a) (b)

Figure 4
(a) Transmitter block diagram, (b) chip photo.

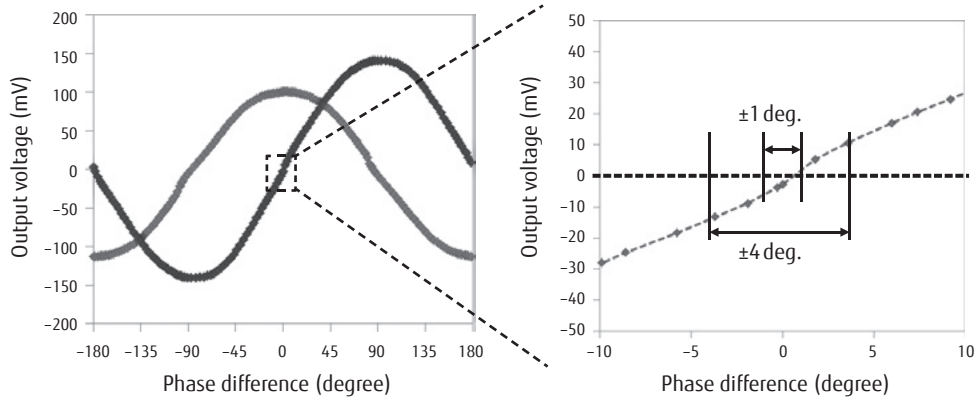


Figure 5
Measured phase difference between each channel.

shows the measured output voltage of the phase detector mixer, when the outputs of the Tx MMIC are in saturated mode. As is known, there are less sensitive areas around the peak and bottom shown in the phase versus the detector output curves. Hence, we designed a phase detector that can output both sine and cosine waves, as shown in Figure 5, and so the sensitive area around the zero-cross point can be employed in all phase ranges. As shown in Figure 5, when the phase difference is±1 degree, the output voltage change is more than a few volts, which is detectable by using conventional AD converters. These initiatives result in accurate phase control for the transmitter and realize a beam steering function.

6. Conclusion

Millimeter-wave CMOS circuits for automotive radar systems were described in this paper. The accurate measurement and de-embedding techniques using on-wafer TRL calibration were discussed. The RF building blocks including a power amplifier were designed based on an accurate transistor model. The large signal performances of the power amplifier were 11.9 dBm of the peak output power and 15% of PAE. A good agreement between the measurements and simulation was also demonstrated. The PLL for the signal generator was designed and showed 0.96 GHz/μs, which is the world's fastest chirp-speed for FCM. The 4-ch transmitter having phase-shifters and detectors also demonstrated accurate phase control operation.

These results are expected to accelerate the development of active phased array radar systems.

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