# Nanocarbon Technology for Development of **Innovative Devices**

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Graphene, a one-atom-thick honeycomb lattice made of carbon, and a carbon nanotube, a rolled-up graphene sheet, have excellent electrical properties, such as high electron mobility and tolerance to a high current density. They also have high thermal conductivity and mechanical strength, and are therefore promising materials for future electronic devices. Facing the limit of scaling (miniaturization) of semiconductor devices represented by silicon transistors, our group is researching ways to apply nanocarbon materials (graphene and carbon nanotubes) to electronics for a breakthrough. In this article, we first explain the electronic states and properties of nanocarbon materials, as well as expectations for applying them that come from their excellent properties. We then describe the method of growing nanocarbon materials, followed by an explanation of our efforts to apply such materials to transistors, interconnects, and thermal interface material (TIM). Finally, we briefly explain a technology to synthesize graphene nanoribbon, a narrow strip of graphene, which we are working on in order to develop devices with superb properties.

# 1. Introduction

Silicon large-scale integrated circuits (LSIs) have been improved in terms of their speed, power consumption, and cost by miniaturization (scaling). This miniaturization, however, has slowed down recently, and it is predicted that the limit may be reached around 2020 or later when the channel length of transistors becomes about 10 nm or shorter. Beyond that limit, it is considered that consumers will still demand better and better electronic devices. Moreover, much higher computing power is thought to be required to make artificial intelligence (AI), a hot topic, literally realistic. Although the computing power is not determined only by the performance of individual device elements, we are put in a situation where we have to find a new route, different from miniaturization, to further improve device performance.

There are several proposals that aim to improve device performance, such as three-dimensional integration. One of the approaches is to improve device elements by introducing new materials. We believe that nanocarbon materials, such as graphene and carbon nanotubes (CNTs), are promising candidates for new device materials. The introduction of nanocarbon materials does not necessarily extend the scaling limit, and we do not intend to claim that such materials will solve all the challenges electronic devices currently face, either. However, the excellent properties of nanocarbon, such as high electron mobility, and tolerance to a high current density, and peculiar phenomena such as Klein tunneling that occur in graphene, make us feel that nanocarbon materials have the potential to overcome the limits of the current electronic devices. Nanocarbon materials are also promising as materials for More-than-Moore devices, such as high-frequency devices and various sensors.

In this article, we first describe the electronic states, properties, and promising applications of graphene and CNTs. We then explain our actual efforts to allow graphene and CNTs to be applied in areas such as transistors, interconnects, and heat dissipation. Furthermore, we briefly describe our on-going project to synthesize graphene nanoribbons (GNRs), which are building blocks for ultimate electronic devices.

# 2. Graphene and carbon nanotubes

Graphene is a single layer of graphite, a layered material, and has a two-dimensional honeycomb lattice [Figure 1 (a)]. The unit cell consists of two unequivalent carbon atoms. This lattice structure leads to electronic states where the dispersion between energy and wave number is linear around K and K' points in the wave-number space, as shown in Figure 1 (b). This linear relationship means that the velocity that is obtained by differentiating the energy with respect to the wave number is constant. In fact, electrons in graphene obey an equation similar to that for a massless neutrino (the electron velocity is 1/300 of the speed of light). This electron band structure causes peculiar phenomena, such as absence of backscattering, Klein tunneling, and half-integer quantum hall effects.<sup>1)</sup> The absence of backscattering leads to a long ballistic length and high electron mobility (10<sup>6</sup> cm<sup>2</sup>/Vs at liquid helium temperature) in graphene. However, as shown in Figure 1 (b), graphene does not have a bandgap (the gap between the top of the valence band and the bottom of the conduction band), and it is therefore difficult to use it as a transistor channel as it is.

A CNT has a structure of a rolled-up graphene

sheet [Figure 1 (c)]. The electronic states can be obtained in a similar manner to the case of graphene. However, depending on how they are rolled, one-third of CNTs become a metal, and the others, a semiconductor. In addition, the bandgap of semiconducting CNTs is inversely proportional to their diameter. The electronic states of GNRs are also different from graphene, as CNTs are. In fact, all armchair-edged GNRs as shown in Figure 1 (d) have a bandgap, exhibiting semiconductor properties.

Graphene and CNTs are, because of their high mobility and tolerance to a high current density (1,000 times higher than Cu), expected to be used as a transistor channel and interconnects. They also have a high thermal conductivity and a high mechanical strength, being a good candidate for heat dissipation materials and reinforcing fillers in resins. In fact, some graphenereinforced resins are already on the market. From the next section, we will explain our efforts for synthesizing nanocarbon materials and developing applications.

# 3. Synthesis of nanocarbon materials

Graphene and CNTs can be grown by chemical vapor deposition (CVD) on silicon and other substrates.

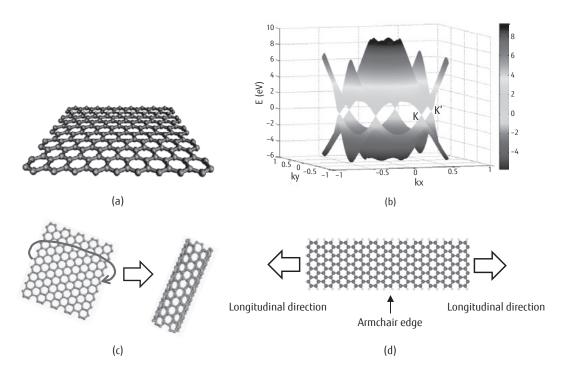


Figure 1

(a) Schematic of atomic structure of graphene (b)Three-dimensional plot of the energy band structure of graphene (c) Illustration of a CNT made of a piece of graphene sheet (d) GNR with armchair edges.

A catalyst film such as iron, nickel, or cobalt is first deposited on the substrate. The substrate is then heated to 500–1,000°C in a reaction chamber, to which a hydrocarbon gas, such as methane or acetylene, is introduced as the source gas. If the catalyst film is as thin as a few nanometers, it forms into particles: the seeds for CNT growth. On the other hand, when the catalyst film is around several tens of nanometers or thicker (depending on the growth condition), graphene is formed on top of the catalyst film.<sup>2</sup> While multilayer graphene is typically formed with Fe, Ni, and Co as the catalyst film, single-layer graphene is selectively formed on a Cu film.

## 4. Application to transistors

Graphene and CNTs are expected to be a channel material for future transistors because of their high carrier mobility. In fact, simulations show that transistors made of multiple GNRs or CNTs have a higher current drivability than Si nanowire transistors and conventional Si transistors.<sup>3)</sup>

Even if pristine graphene, which does not have a bandgap, is used as a transistor channel, the channel current can be modulated by the gate voltage, because the density of states around the Fermi level changes depending on the gate bias. **Figure 2 (a)** shows a top-gate transistor we fabricated using CVD-grown graphene. The transistor characteristics are shown in **Figure 2 (b)**.<sup>4)</sup> Although the drain current is actually modulated by the gate bias, the degree of modulation is much smaller (about 20%) than the conventional transistors whose current can be modulated by 4–6 orders of magnitude. Graphene nanoribbons, which have a bandgap, should be used instead in order to increase the on-off current ratio.

The transistor shown in Figure 2 exhibits ambipolar behavior, which can be utilized to design a novel device. Figure 2 (c) schematically shows a dual-gate transistor with a graphene channel. By applying a positive or negative bias,  $V_{bg}$ , to the back gate, the response,  $I_d$ , to the top-gate bias,  $V_{tg}$ , can be shifted, as shown in Figure 2 (d).

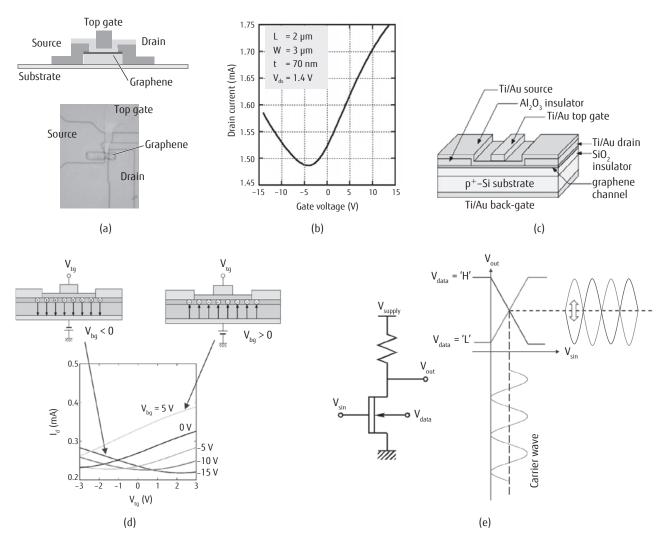
We can fabricate a binary phase-shift keying modulator by using the simple circuit shown in **Figure 2 (e)**, which makes use of these interesting characteristics. Phase-shift keying is a digital modulation method that is widely used in wireless local area networks. In the device here, the phase of the output signal,  $V_{out}$ , is changed by 180 degrees from the input to the top gate,  $V_{in}$ , depending on whether the back gate bias is positive (H) or negative (L). The device demonstrates that we can fabricate novel and different devices by making good use of the interesting characteristics of graphene.

## 5. Application to interconnects

Graphene and CNTs are also promising candidates for scaled LSI interconnects because of their long ballistic length and tolerance to a high current density. We have worked on interconnect applications for more than 10 years. Graphene and CNTs should be synthesized at around 400°C or lower, in order to incorporate these materials into the back-end-of-line process of LSIs, where low-temperature processes are required. We actually succeeded in growing CNTs at around 400°C. However, we have not yet obtained graphene and CNTs with electrical properties required for interconnects at such a low temperature. Therefore, we recently employed a new strategy, in which graphene and CNTs are grown on a different substrate at a high temperature and they are then transferred onto a target substrate to make interconnects.<sup>6), 7)</sup>

**Figure 3 (a)** shows a scanning electron microscopy (SEM) image of a multilayer graphene interconnect using a transfer process. The interconnect has a thickness of about 10 graphene layers (3–4 nm). The cumulative distribution of resistivity of 4  $\mu$ m-wide interconnects is shown in **Figure 3 (b)**. The best resistivity was around 40–50  $\mu$ Ccm, which is close to that of bulk graphite. The results imply that the quality of our CVD-graphene is as high as that of bulk graphite. However, the resistivity obtained is still one order of magnitude higher than that of bulk copper, and therefore it is still difficult to replace Cu interconnects with pristine graphene.

In order to lower the resistance further, we employed an intercalation process, where alien molecules are intercalated into multilayer graphene to increase the carrier density in graphene. The distributions of sheet resistances before and after intercalation are shown in **Figure 3 (c)**. The median of the resistance decrease ratios obtained by intercalation was about 1/20. The best resistivity estimated by considering the thickness was 1.5  $\mu\Omega$ cm, which is better than that of



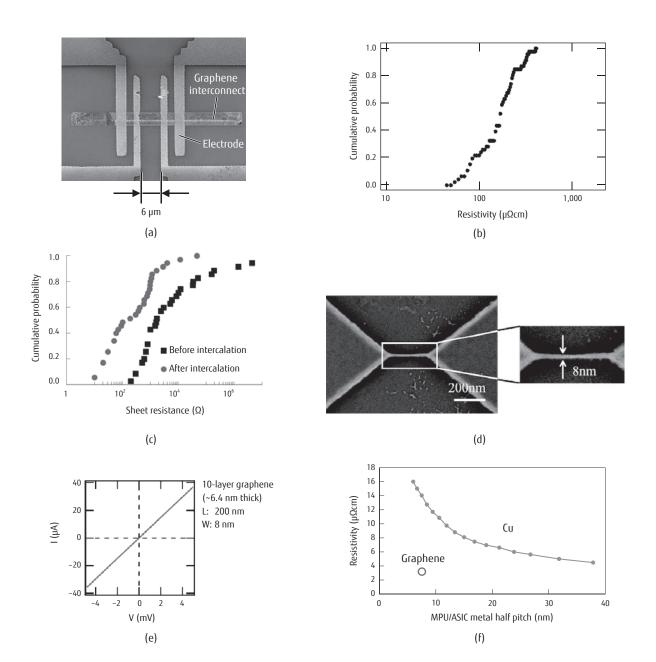
#### Figure 2

(a) Schematic and optical microscope image of a top gate transistor with a channel of CVD-grown graphene. The width (W) and length (L) of the channel are 3  $\mu$ m and 2  $\mu$ m, respectively. The thickness of the gate insulator is 70 nm, and the drain voltage is 1.4 V. (b) Characteristics of the top-gate transistor shown in (a). (c)Schematic of a dual-gate transistor. (d) Figure showing how transfer curves in terms of the top-gate bias (V<sub>19</sub>) are shifted depending on the back-gate bias (V<sub>19</sub>), indicating the polarity of a transistor can be controlled. (e) Schematic diagram (left) and output characteristics (right) of binary phase-shift keying modulator consisting of the dual-gate transistor shown in (c) and a resistor. The positive and negative back-gate biases correspond to H and L of V<sub>data</sub>, respectively. The polarity of the sine wave input at the top gate is inverted and output at V<sub>out</sub> when V<sub>data</sub> is H.

#### bulk copper.

The results above are for 4 µm-wide interconnects. We further narrowed down the interconnects to widths below 10 nm by using a state-of-art electron beam lithography system. An SEM image of an 8 nm-wide multilayer graphene interconnect is shown in **Figure 3 (d)**. **Figure 3 (e)** shows the current-voltage characteristics of the interconnect. The current is linear to the applied voltage, and the interconnect did not exhibit a substantial drop in conductivity after being

narrowed down, which is often seen in GNRs fabricated by lithography. The resistivity of this interconnect is  $3.2 \mu\Omega cm$ , which is better than predictions for scaled Cu interconnects (from ITRS2011), as shown in **Figure 3 (f)**. This resistivity is our best value, and we still have process issues to address to suppress scattering in the data. However, this is probably the first result that has shown that sub-10 nm graphene interconnects can have lower resistivity than Cu interconnects, thus indicating a bright future for graphene



#### Figure 3

(a) SEM image of a multilayer graphene (MLG) interconnect. (b) Cumulative probability distributions of resistivity of MLG interconnects. (c) Cumulative probability distributions of sheet resistances of MLG interconnects before and after the intercalation process. (d) SEM image of an 8-nm-wide MLG interconnect. Electron-beam resist is deposited on the graphene. (e) Voltage-current characteristics of the 8-nm-wide interconnect shown in (d). (f) Resistivity of the graphene interconnect shown in (e), along with predicted Cu resistivity as a function of interconnect width (Metal half pitch). (From International Technology Roadmap for Semiconductors (ITRS) 2011).

interconnects.

# 6. Heat dissipation applications

Nanocarbon materials are also expected to be used as heat dissipation materials due to their high thermal conductivity. Because CNTs also have a high flexibility, we try to insert between a CPU and heat spreader a high-conductivity sheet consisting of a bundle of CNTs as thermal interface material TIM [**Figure 4 (a)**]. Indium and resins with high-thermalconductivity fillers are usually used as a TIM. The thermal resistance of a TIM is expected to decrease by employing CNTs.

For using CNT bundles as a TIM, the site density

of CNTs should be increased to lower the thermal resistance. To this end, we not only optimized the growth condition of CNTs, but also developed a new CNTtransfer method. As shown in Figure 4 (b), CNTs are first transferred onto a piece of horizontally expanded silicone rubber. After the transfer, the rubber is shrunk back to its original size, making the CNT density three times larger than the original density.<sup>8)</sup> The height of the fabricated CNT sheet was about 140 µm with a CNT occupation ratio of 8-9%. The sheet was then inserted between two Cu blocks (one was connected to a heater and the other cooled as a heat sink). The temperature difference between the blocks was 1.06°C, which is close to that of an indium TIM. CNT-TIMs can be applied to multiple chips with different heights, where indium TIM is difficult to use. Furthermore, CNT-TIMs have a lower thermal resistance than a resin (with filler) TIM, which is typically used for multiple chips. Therefore,

CNT-TIM is expected to be launched on the market in the near future.

# 7. Bottom-up synthesis of graphene nanoribbons

As described above, graphene does not have a bandgap, and graphene must be made into a nanoribbon in order to form a bandgap. However, the required width is extremely narrow, a few nanometers or narrower. We have tried to form GNRs by using electron-beam lithography and by direct etching with helium ion beams.<sup>9)</sup> However, we have not yet obtained GNR-channel transistors with good performance. This is probably because the GNR edges became defective in the top-down GNR formation process. Therefore, we are now working on bottom-up synthesis of GNRs from precursors formed by organic chemical reactions, which was first demonstrated by Cai et al.<sup>10)</sup>

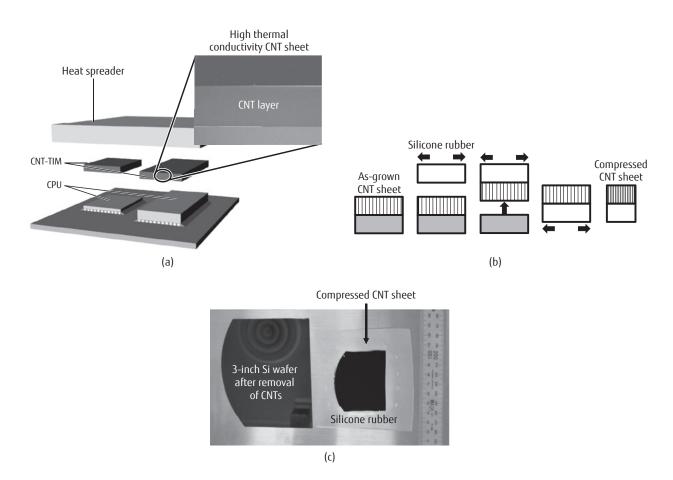


Figure 4

(a) Illustration of CNT sheet used as TIM (b) Compression process of a CNT sheet using silicone rubber. (c) Top view of a compressed CNT sheet. A CNT sheet where the size of the Si substrate on the left was compressed to the size shown in black on the right.

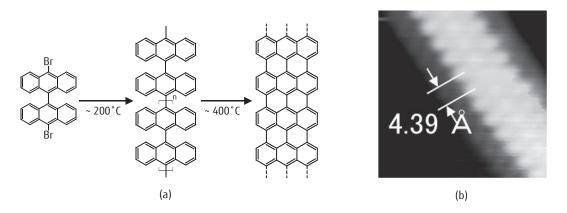


Figure 5

(a) Schematic of GNR formation process. Shown on the right is a precursor synthesized by organic chemical synthesis. (b) Scanning tunneling microscope image of a synthesized GNR.

**Figure 5 (a)** shows a process of forming GNRs and **Figure 5 (b)** is a scanning tunneling microscope image of a GNR we synthesized. It is possible to make bottom-up GNRs with various properties by changing their width, edge structure, and edge functional group. We believe that such GNRs can be building blocks of future nanoelectronics devices. We would like to develop low-power-consumption transistors, high-frequency devices, and high-sensitivity sensors using GNRs in the near future.

# 8. Conclusion

In this article, we described the properties and synthesis of nanocarbon materials, graphene and CNTs, as well as their applications we have worked on. Nanocarbon materials have excellent properties, and we can develop really innovative devices if we can make best use of such properties. The synthesis and device technologies of nanocarbon materials have made substantial progress for the last ten years. However, realizing innovative devices using new materials is not an easy task, and we still need some more breakthroughs. We would like to develop innovative and essential devices for a future Internet of Things (IoT) society using nanocarbon materials and realize a more comfortable life for people.

Part of this research was performed at the National Institute of Industrial Science and Technology and supported by the Japan Society for the Promotion of Science (JSPS) through its "Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program)." This research was also

partly supported by JST, CREST.

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