3D Packaging Technology to Realize Miniaturization/High-Density and High-Performance Servers

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With LSI micro-fabrication technology reaching its scaling limits, miniaturizing LSIs based on Moore's Law is unable to satisfy the CPU/memory module performance for high-speed and low-power servers. Fujitsu Laboratories has developed a 3D packaging technology that connects between multiple devices in the shortest distance. This technology is a revolutionary next-generation packaging technology for high-performance servers to support Fujitsu's existing information and communications technology (ICT) business. We were the first to verify 3D logic device operation by integrating the following technologies: through silicon via (TSV) technologies, in which signals are connected in the shortest distance between top and bottom stacked LSIs; super multi-pin connection technology for bandwidth expansion; and transmission design technologies considering power integrity and signal integrity (PI/SI) between stacked chips. Further, by optimizing the design of TSV and a redistribution layer (RDL), we have been successful in greatly shortening the connection distance between chips and increasing data transmission volumes, and high-speed transmission of 25 Gbps has been confirmed. Additionally, we have developed solder materials and a process to be used in fine TSV in which large amounts of current flow and connection terminal sections on chips, achieving stable supply of 200-Watt-class power. In this paper, we will discuss the important key technologies in 3D packaging technology for realizing high-performance processors.

1. Introduction

To miniaturize LSIs, improvements in integration density based on Moore's Law are reaching their limits in terms of the physical devices and micro-fabrication dimensions.[1] On the other hand, in the packaging process, technologies such as System in Package (SiP) that integrates a number of devices having multiple functions into one package have started to come into use, mainly in mobile devices.[2] Further, recently attention has turned to 3D high-integration technology, which improves overall system performance by stacking LSIs on the top and bottom and interconnecting in the shortest distance through a through silicon via (TSV).[3)–5]

3D packaging integration is a technology that further improves LSI performance and functionality based on scaling rules without using cutting-edge miniaturization technology.

With the aim of helping to increase the performance of fundamental technologies for servers and supercomputers to support the information and communications technology (ICT) business, the next-generation smart device development project was started with assistance from the New Energy and Industrial Technology Development Organization (NEDO) from 2013 in Japan, to develop processors integrating multiple functions that are compact, low-power-consumption and capable of processing at high speeds.

In this paper, we will explain the important power integrity and signal integrity (PI/SI) design technologies, TSV backside technologies and high-reliability micro bump formation technologies, as 3D packaging integration for realizing high-performance processors.

2. Basic configuration of 3D processors

With the development of high-performance processors, specifications that excel in power consumption (200 to 300 W), heat generation, number of electrodes and large chip area are required, necessitating a major

technical leap from the conventional 3D packaging technologies.

A schematic diagram of the 3D packaging CPU module in this development and a cross-sectional image of the 3D packaging device prototype are shown in **Figure 1**. A TSV with a diameter of 10 μm is fabricated on the bottom chip with a thickness of 50 μm, and the chips are stacked on the top and bottom using 40 μm pitch micro bumps. In a verification experiment of the processor stacking, with the focus on power performance, the shortest connection between the top and bottom nodes was achieved, with the aim of realizing a low power consumption of 200 W. On the other hand, in order to apply the 3D packaging technology to products, design technology based on accurate physical and electrical parameters is required. The development items and achievement level in this study are shown in **Table 1**. The following three technologies were developed with the aim of realizing a specification that greatly improves on the conventional 3D LSI technology.

1) PI/SI design technology

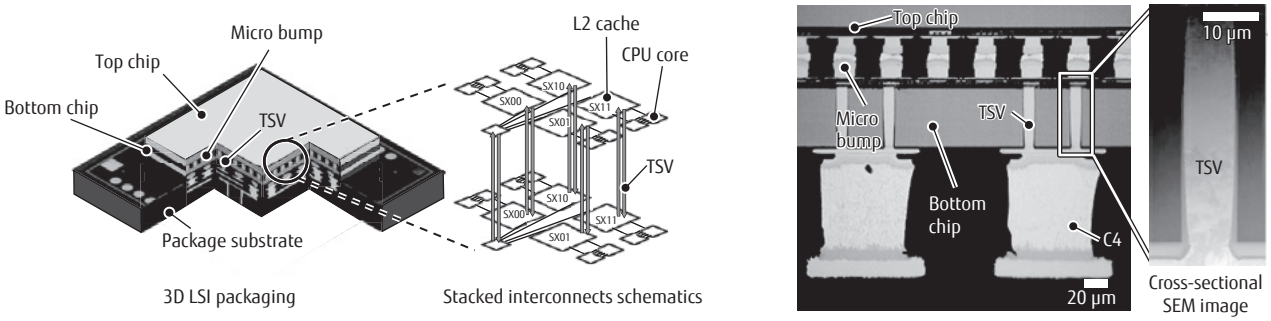
This is TSV and electrode design technology to achieve the two aims of 25 Gbps high-speed transmission and a large power supply. We are establishing design rules for signal wiring and power lines via TSV, and developing evaluation technology for their verification and analysis.

2) TSV backside technology

This is structure design and process technology for newly adopted TSV and backside (reverse side) electrodes. We have established process technology that enables both thin device wafers corresponding to TSV formation with a diameter of 5 to 10 μm and fabrication manufacturing of TSV and backside electrode structures.

3) High-reliability fine pitch bump formation technologies

This is a large-current, high-heat dissipation and high-precision stacking technology. We have developed a process technology for fine-pitch micro bump junctions supporting large current and high-precision I/O bumps stacking chips with 200,000 or more pins.



(a) Schematic diagram of 3D LSI

(b) Cross-sectional image of 3D LSI

Figure 1
Diagrammatic illustration and cross-sectional image of developed 3D CPU packaging module.

Table 1
Element technology items for 3D LSI and comparison of conventional technology and development target.

Element technology items	Conventional technology	Development target
TSV backside process	>300 μm: 23 mm square chip	<100 μm: 23 mm square chip
C4 bump tolerable current	25 mA	>100 mA
Micro bump material	<10 mA/bump: SnAgmaterial	>50 mA/bump: Intermetallic compounds junctions
Stacked die area	100 mm^2	>500 mm^2
Number of micro bumps	150,000	300,000
TSV transmission performance	20 GHz	40 GHz

3. PI/SI design technology and transmission characteristics

TSV that penetrates the bottom chip may cause local stress distribution, and this may affect a Metal Oxide Semiconductor Field Effect Transistor (MOSET) and circuit characteristics.[6),7)] In order to avoid the effects of TSV stress, a keep out zone (KOZ) needs to be established in which transistors cannot be allocated; and this is being studied using a structure analysis simulation and stress measurement tests.[8)] However, as the sensitivity to mobility changes in relation to tensile strength and compression stress differ in CMOS circuits between the p type and n type, it is difficult to predict an accurate KOZ for actual circuits. For this reason, with the aim of predicting highly accurate KOZ for actual circuit movements, we have constructed an analysis technology that integrates technology CAD (TCAD) and Simulation Program with Integrated Circuit Emphasis (SPICE) circuit simulations, and developed a more realistic KOZ prediction technology.[9)]

The results of estimating KOZ from the pMOS and nMOSFET drain current (I_d) and oscillation cycle of ring oscillator (ROSC) are shown in **Figure 2**. With a TSV diameter of 10 µm and distance from the TSV edge of 2 to 25 µm, we performed a simulation of 65 nm node planar type MOSFET I_d characteristics. The transistor mobility change and V_d/I_d parameters were derived with TCAD using the stress propagation from TSV, and the KOZ when operating the actual circuit was obtained by running the SPICE circuit simulation.

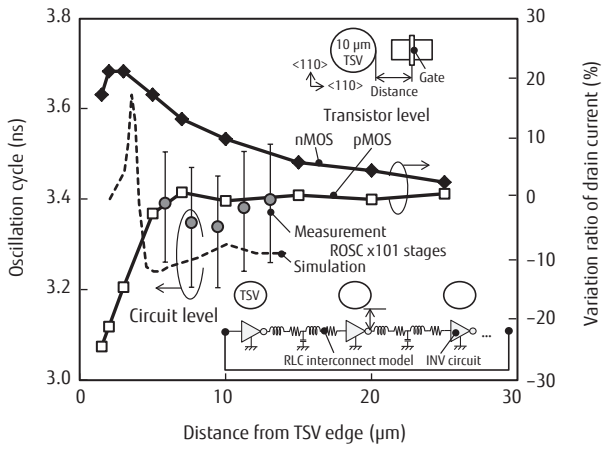


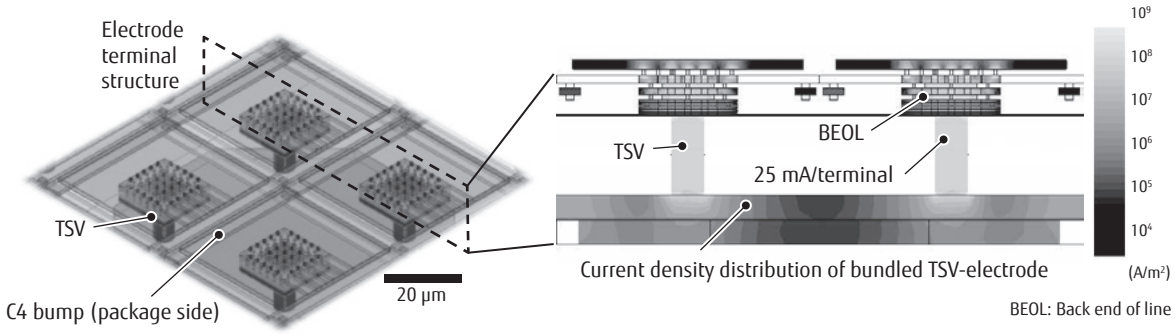
Figure 2
Variation ratio of drain current of MOSFET and analytical result of TSV KOZ with ROSC circuit oscillation frequency evaluation.

The distance dependency between TSV for the I_d change rate of pMOS and nMOS respectively has an increased change rate in the vicinity of TSV for both pMOS and nMOS and this polarity is different. Further, if we define KOZ as the distance at which I_d changes by 10%, nMOS is more highly affected by TSV stress and KOZ can be estimated at approximately 10 µm from the TSV edge.[8)] Further, when the ROSC circuit (101 stages) is located in the vicinity of TSV, the KOZ estimated from SPICE circuit simulation oscillation cycle changes (dotted line) are 5 µm or less from the TSV edge, and shorter than in case of the single MOS transistor unit. This is because the actual driver circuit is made up of both nMOS and pMOS transistors and the inverter operation speed is determined from a balance of the electric charge and discharge characteristics of each.

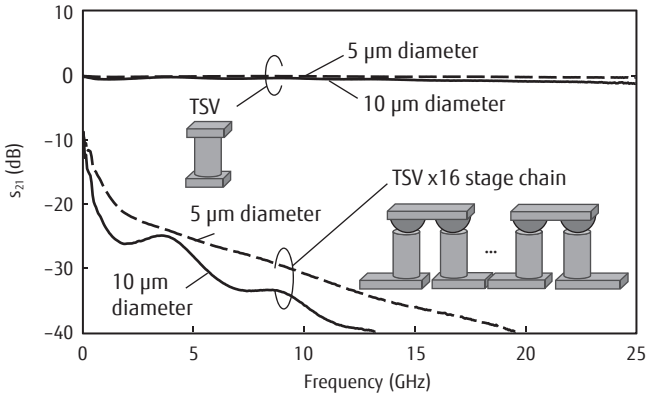
As the measured value of the ROSC oscillation cycle for the actual stacked chip matches the results of the simulation closely, it is considered possible to include precise KOZ into circuit design. It has been shown that the method of KOZ estimation that integrates stress propagation and circuit simulation is effective in device design.[10)]

The next issue in PI design is to ensure a stable power supply for a high-performance processor with power consumption over 200 W. It is important for each through electrode and electrode linking 3D stacked chips to have a structure design that can withstand a high current density. In order to be compatible with a large current supply, we developed a multi-TSV electrode structure where multiple TSV-micro bumps are bundled, made up of C4 bumps (50 µm pitch) on the organic package side and TSV-micro bumps (40 µm pitch). **Figure 3 (a)** shows the results of power current analysis of the four-cell bundled structure, and the over 100 mA for C4 bump allowed current could be obtained as opposed to the previous 25 mA/bump of power cell allowable current, enabling stable supply of power for a high-performance processor.

For SI, it is necessary to transmit signals between the top and bottom chips via TSV at high speeds of over 30 Gbps without loss. Signal propagation via the stacked chips adds resistance and capacity of TSV and the micro bumps. The transmission loss (S_{21}) for 5 µm diameter and 10 µm diameter TSV units and TSV16 stage chains are shown in **Figure 3 (b)**. TSV



(a) Analyzing power cell current density of four-cell bundled electrode terminal structure



(b) Transmission loss in high-frequency property of TSV

Figure 3
PI/SI electronic design and TSV transmission characteristics.

unit transmission loss, in the case of 12.9 GHz signal transmission, is −0.2 dB for 5 µm and −0.3 to 0.5 dB for 10 µm, and it is clear that the TSV unit can transmit at sufficiently high speed. These values are considered to be good characteristics as they can withstand the use of signal transmission between layers in 3D-LSI.[11)]

4. TSV backside process technology

We have developed processes from TSV formation to backside electrode structure in relation to logic device wafers. In 3D packaging, in order to supply power and transmit signals between the top and bottom chips, micro bump electrodes that are required for providing a junction between the TSV penetrating the Si chip and the chip, and a redistribution layer (RDL) on the backside of the chip are fabricated. The fabrication process flow of a 3D packaging device is shown in **Figure 4 (a)**. A series of processes up to chip stacking have been newly added, including the following four TSV backside electrode fabrication processes.

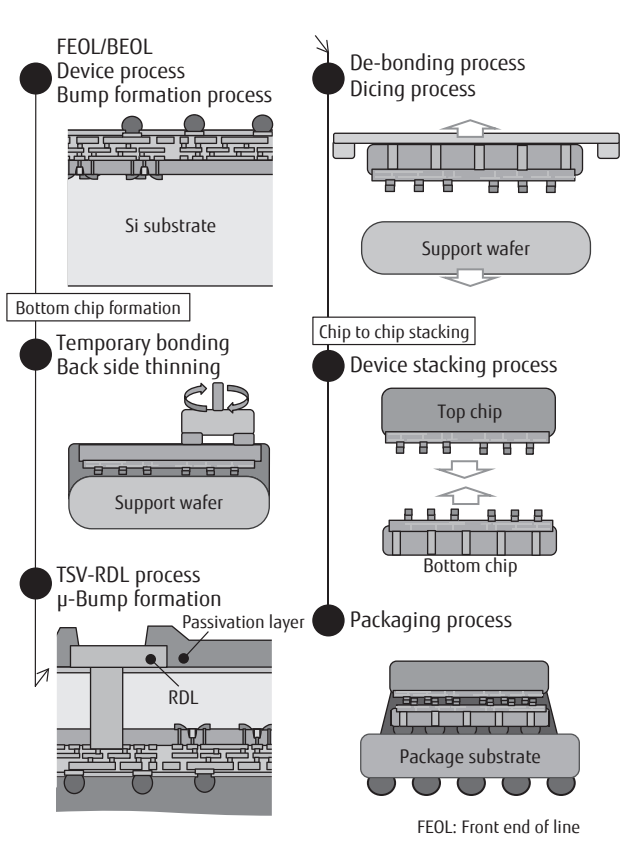
1) Backside thinned process to the bottom chip
2) Process of TSV-backside interconnect to the bottom chip device
3) Micro bump process to the top and bottom chips
4) Device stacking process and packaging process

In the process to thin the backside of the bottom chip, temporary adhesive and support wafers are used and the logic chip is thinned down to a thickness of 50 µm using a backgrinding method. High-precision control of 2 µm or less is required for the total thickness valuation (TTV) of the 300 mm diameter wafer at this time. Next, the via-last method is used from the backside of the thinned wafer to fabricate the 10 µm diameter TSV, and further form the RDL and micro bumps.

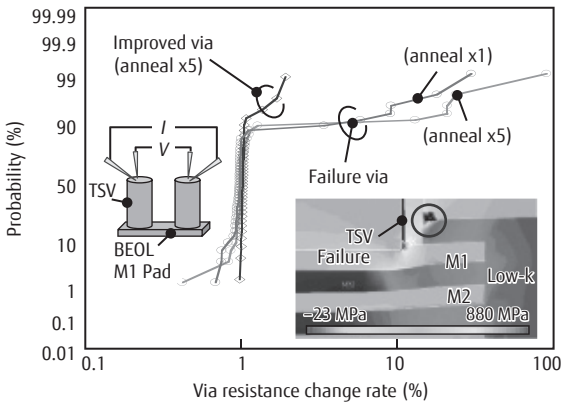
As there is a large difference in coefficient of thermal expansion (CTE) between Cu and Si crystals used in TSV, if there is a problem with the process when TSV is formed, it is easy for contact failures to occur due to problems in the thermal cycle. This is because as

TSV-Cu thermally expands, compression stress tends to be applied to the Cu/Low-k (low dielectric constant interlayer insulating film) wiring on the device side.[12] **Figure 4 (b)** shows the variability rate in the contact resistance between TSV and interconnects, indicating that a defective via has a higher rate of increase in resistance. It is clear from physical cross-section analysis and thermal stress analysis that if the coverage of a Ti barrier adhesion layer worsens under a via, and a large deformation occurs in the shear direction below TSV due to thermal expansion, this may cause stress fractures in the vicinity of the device interconnects. Therefore, by improving the via shape and Ti barrier adhesion layer coverage when TSV is formed, a TSV with high thermal reliability could be obtained.[13),14)]

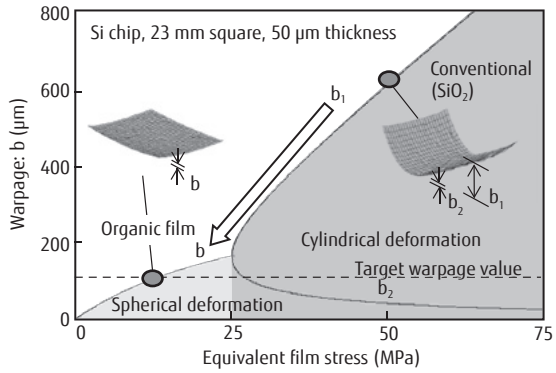
To make it easier to fabricate TSV and reduce RLC transmission loss, a via-through structure with as low an aspect ratio as possible is desirable. On the other hand, with the wafer process to thin the via-last process, the optimal thickness is 50 µm from the perspectives of ease of manufacturing, chip handling and electrical characteristics. However, if the thinned Si chips exceed 23 mm square, warpage becomes an issue. As shown in **Figure 4 (c)**, as stacking can be difficult due to the peculiar buckling distortion of the thinned chip, it is necessary to develop deformation control technology for the device layer on the front side of the chip and the RDL dielectric layer on the backside.[15),16)] We developed an RDL process using organic passivation materials that can create film stress in relation with the chip surface, and by reducing the warpage to approximately one-sixth the level of conventional structures, this has simplified the 3D stacking structure formation of thin devices.



(a) Fabrication process flow of 3D LSI CPU module



(b) Improvement of TSV process issue



(c) Structural optimization of device of thinned device chip

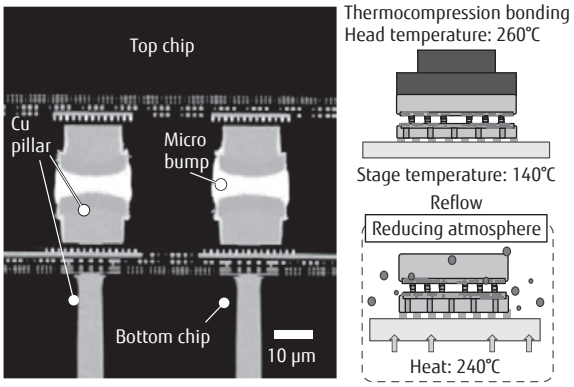
Figure 4
TSV backside process technology.

5. Fine-pitch bump terminal connection technology

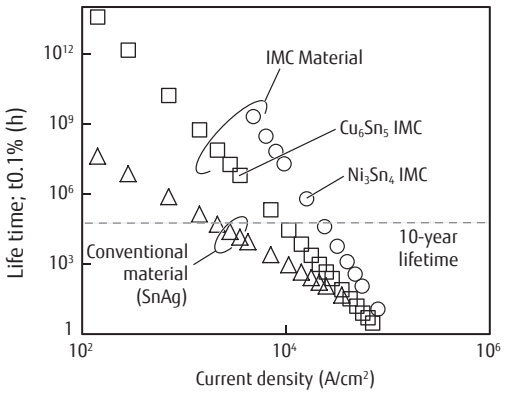
In order to connect stacking chips with more connection pins, high-precision stacking technology using fine-pitch micro bump formation becomes important. In particular, in the case of large chips exceeding 20 mm square, the number of bumps between chips exceeds 100,000, and with this ultra-high-density pin junction, which is incomparable to previous implementations, it is necessary to develop advanced stacking technology to control exactly the accuracy of the fine-pitch micro bump terminal junction position and a bump structure with excellent heat dissipation for large currents. We developed a chip stacking technology using reflow processing in a fluxless reducing atmosphere in order to improve the micro bump interconnection with high accuracy. **Figure 5 (a)** shows a cross-section SEM image of fine-pitch micro bumps, and a cross-section image of the results in which high positional accuracy was secured using the self-alignment effect of micro bump terminal junctions and the stacking flow.

In the stacking chip area, 20 µm diameter micro bumps at 40 µm pitches were formed on to a 23 mm square size stacking chip, achieving an ultra-high-density pin junction of more than 290,000 pins. The micro bumps were joined with the top and bottom chip with Sn-2.3Ag being formed on the Cu pillar. The bottom chip was joined to an organic package board via a 10 µm diameter TSV and 80 µm diameter C4 bump (160 µm pitch).

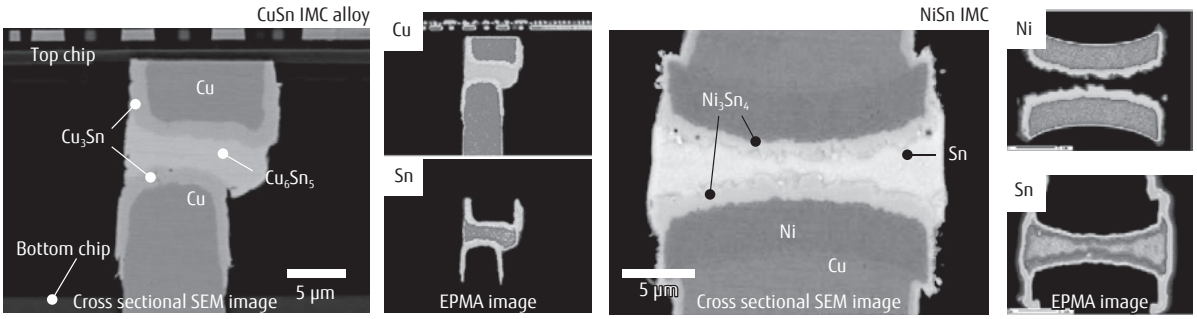
As the developed fine-pitch micro bump junction process adopted reflow processing within a reducing atmosphere including gas with oxygen-depleting characteristics, this has the effect of reducing the oxide film formed on the solder surface and self-alignment effects through surface tension of the SnAg solder materials. A process was constructed that made it possible to create a micro bump junction of comparatively large chips of more than 20 mm square, and positional slip at a level of one-tenth that of previous processes has



(a) Cross-sectional SEM image and process flow in micro bump stacking process



(c) Improved EM life time with IMC material



(b) EPMA analysis of intermetallic compound (IMC)

Figure 5
High-reliability large die stacking technology and micro bump joint technology.

been achieved, realizing high-precision micro bump interconnection.[17)]

6. Reliability of large die stacking

When stacking logic devices with large power consumption, minute micro bump junctions compatible with a large current power supply to the top chip side are required. With the aim of achieving a high melting point for fine-pitch terminal connections, we have studied the formation of intermetallic compounds (IMC) with high current density resistance and improvements in electromigration (EM) resistance.

Figure 5 (b) shows a cross-sectional SEM image of a micro bump alloy junction section and the results of analysis using an electron probe micro analyzer (EPMA). When a Ni barrier is not used as the IMC junction technology for micro bumps Cu_6Sn_5 alloys are formed; and when a Ni barrier is used Ni_3Sn_4 alloys are formed. From the EPMA analysis image, we can see that IMC is formed in the micro bump junction area. IMC junction technology was established by clarifying the bump connection temperature and time in which IMC can be well controlled and formed.[18),19)]

The rupture life (defect rate 0.1%) for a micro bump EM joined with IMC is shown in **Figure 5 (c)**. Compared with the current density for a 10-year guaranteed lifetime, the case of IMC alloy joining achieves a current density resistance that is four times better than that of conventional SnAg solder materials, and this has proven to be effective for a high-performance processor. Thus, we have created a micro bump structure that can withstand power provision of 50 mA or more per 200-Watt-class terminal. It has also been clarified that the EM lifetime is different between the alloy types of Cu_6Sn_5 and Ni_3Sn_4 formed by IMC junctions. Controlling the process conditions of junction fabrication temperature and alloy phase change promises to achieve higher levels of reliability.[20)]

7. Conclusion

In this paper, we have developed a 3D stacking technology as a fundamental technology for a next-generation high-performance processor. By developing TSV fabrication technology compatible with large-size chips for a high-performance processor and overcoming the problem of warpage and reduced propagation characteristics, we have achieved a TSV propagation characteristic of 40 GHz with a 23 mm square stacking chip. Further, we have developed a fine-pitch micro bump junction structure compatible with a large current and verified that this is a 3D packaging structure with a guaranteed lifetime of 10 years even when supplying 200-Watt-class power. By integrating the 3D device fabrication technologies developed this time, stable operation at 1.6 GHz was confirmed by the function evaluation test circuit Test Element Group (TEG) using a 65 process nm technology of logic LSIs. We will continue to develop this technology in Fujitsu products moving forward, as an innovative function packaging technology for realizing high-performance servers.

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