Hardware Platform Supporting Smartphones

● Toru Ogawa ● Kenichi Ito ● Koji Matsushima

In recent years, propelled by Apple Inc. and Google Inc., the popularity of smartphones has skyrocketed. By the end of March 2012, the proportion of smartphones in relation to all mobile phones sold in Japan exceeded 70%. Their user interface, unlike that of feature phones, is a touchscreen, which is getting bigger with higher resolution. Moreover, as network speeds continue to increase (particularly for Internet access), data traffic volumes are increasing exponentially. This has led to a challenging problem—giving smartphones the processing power required to handle large volumes of data (power equivalent to that of PCs just a few years ago) while keeping power consumption at a level appropriate for a mobile device. This paper describes the evolution of the application processor used on the high-performance hardware platform supporting Fujitsu's smartphones and Fujitsu's approach to solving the technical problems related to the performance and power saving required of smartphones.

1. Introduction

Mobile phones produced in Japan are evolving in a manner unique to Japan, and multifunctional devices are being embraced by many users. A diverse range of functions are now available, such as one-seg TV, FeliCa (an RFID smartcard system), and a high-resolution camera, and users are being continuously tempted to buy the latest model phones with new and more advanced functions.

Unlike the case for feature phones, potential smartphone customers are shown the CPU-related specification ("spec") sheets (listing number of cores, maximum CPU speed, internal memory capacity, etc.). This situation is the same as that in the PC marketplace.

In addition, as a result of the advent of high-resolution displays, enhanced communication features, and so on in recent years, data traffic volumes are increasing exponentially. The processing load on smartphones is therefore increasing rapidly, creating a need to increase their CPU performance. This has led to an increase in the power consumption of smartphones, leading to the common complaint that smartphones have poor battery life.

This paper describes the evolution of the application processor used on the high-performance hardware platform (the main component) of Fujitsu's smartphones and the technologies used for reducing the power requirements. It also describes Fujitsu's efforts towards satisfying the needs of the market (namely, high performance and low power consumption).

2. Evolution of application processor and various technologies

The configuration of the hardware platform currently used in Fujitsu's smartphones is shown schematically in **Figure 1**. The platform is composed of an application processor, a modem (baseband), a wireless unit, a power supply, an audio LSI, synchronous dynamic random access memory (SDRAM), and flash memory. As described in the following subsections, various technologies that form the core of the rapidly evolving application processor have been evolving rapidly.

2.1 Evolution of application processor

The application processor is composed of a CPU, a graphics processing unit (GPU), and controllers for its memory, peripheral devices, and display (**Figure 2**). These are the key components for attaining the high performance and functionality needed for a

smartphone.

A smartphone needs much higher performance than a feature phone. Specifically, the application scenarios of smartphones are substantially different from those of feature phones; for example, their high-resolution display supports the viewing of on-line video and browsing of websites designed for viewing with a PC. As a result, they must process a much greater volume of data. Moreover, when their display resolution was increased from 800 × 480 pixels (wide video graphics array) in 2010 to 1920 × 1080 pixels (full HD) in 2012, the data volume increased 5.4 times. The graphic performance of the display has been increased to 60 frames per second, so the GPU performance needed for executing graphics processing at high speed has become a key factor in ensuring operability. This demand for increased performance has driven the evolution of the CPU and GPU in the application processor.

The evolution of the ARM CPU commonly used in mobile phones is shown schematically in **Figure 3**. In three years (from 2010 to 2012), the operating frequency was increased from 1 to 1.7 GHz, and the number of CPU cores went from one to two and then from two to four. The increase in CPU performance due to the increase in CPU operating frequency has reached the limit of semiconductor-process technology, so CPU performance is being increased by using multiple CPU cores.

The GPU is built-in for specialized processing of graphics—which has become ever more complex. In general, if certain processing can be done by either hardware or software, power efficiency is better if it is

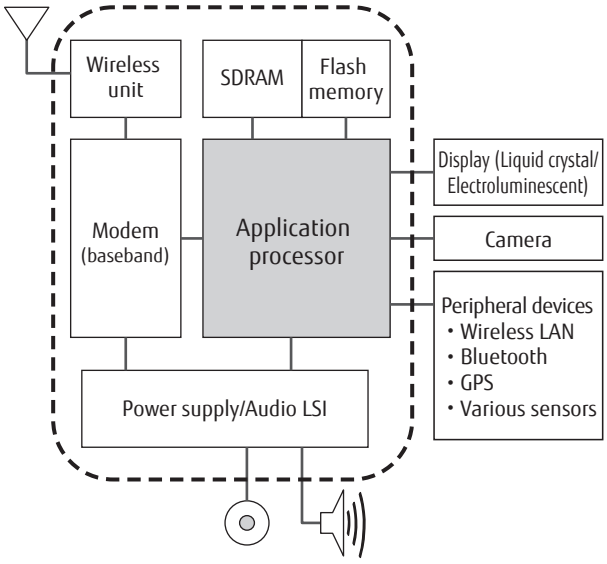
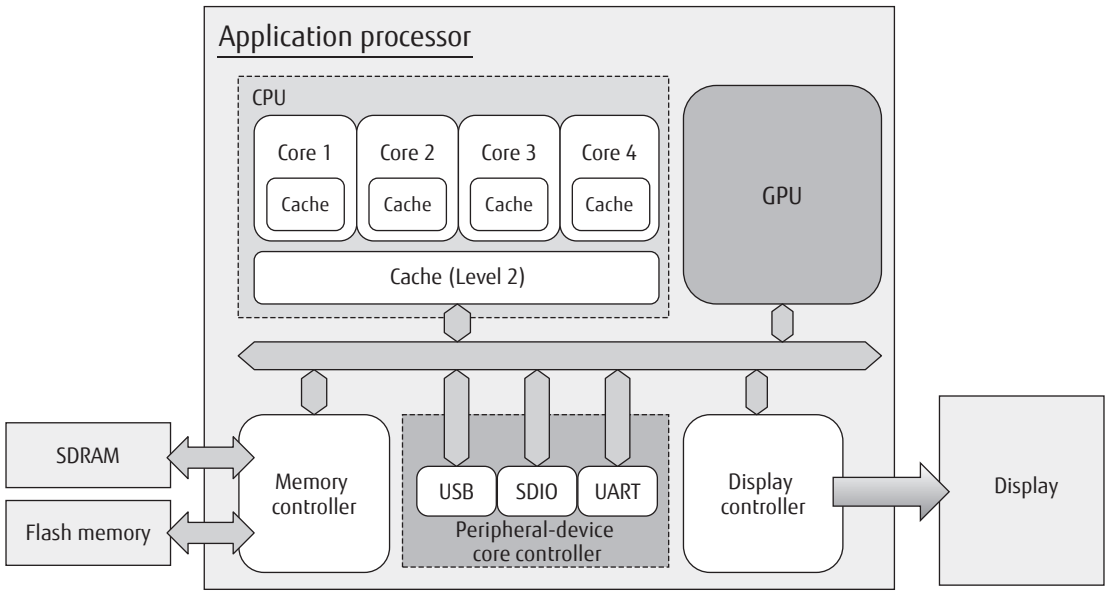


Figure 1
Configuration of hardware platform.



SDIO: Secure Digital Input/Output
UART: Universal Asynchronous Receiver Transmitter

Figure 2
Configuration of application processor.

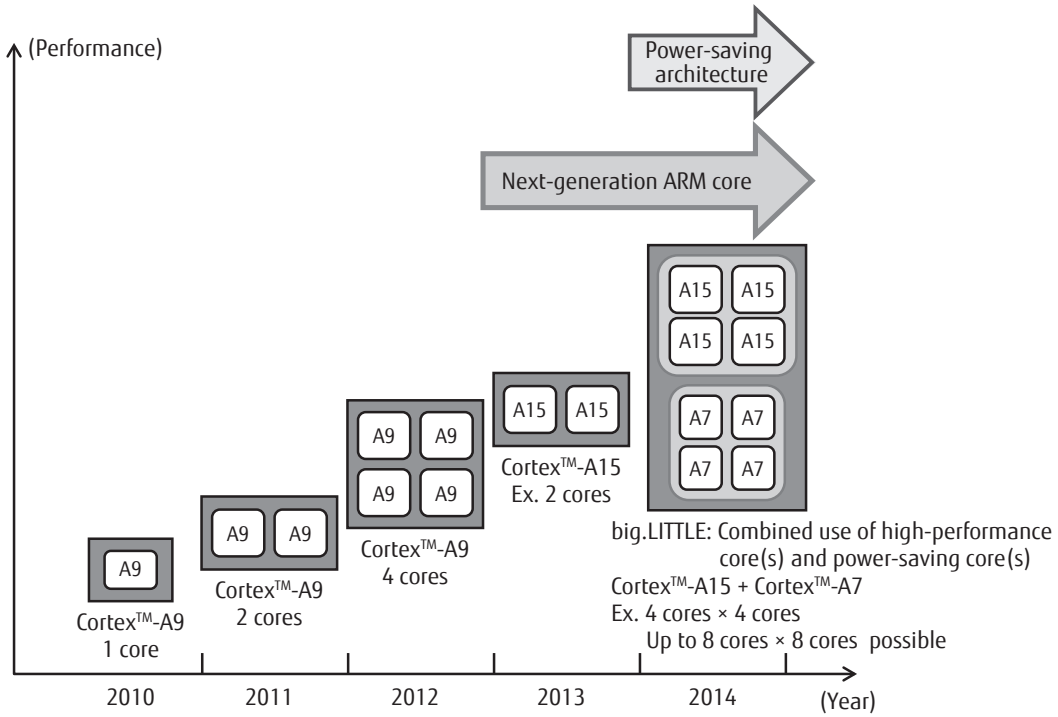


Figure 3
Evolution of ARM CPU.

done by specialized hardware. The operation frequency of GPUs as well as that of CPUs has been boosted and the number of cores has multiplied in recent years.

2.2 Scaling down of transistors and process technology

Another trend is the increasing size of the application processor in smartphones as a result of the increasing need for performance and functionality. Accompanying this increase in size is a scaling down of the transistors–with the aim of achieving high integration and low power consumption. Up until 2011, the length of a transistor gate was 40 or 45 nm; it is now 32 or 28 nm. By 2014, mass-produced transistors will likely have a gate length of 14 nm.

Although this scaling-down of transistors will result in increased leakage current, it will reduce power consumption. The leakage current can be reduced by using a gate insulating film with a high dielectric constant in place of the SiO_2 dielectric commonly used. Since 30 to 50% of the power consumed by a smartphone is accounted for by the application processor, the evolution of power-saving technologies due to advances in the semiconductor manufacturing process will become even more important.

2.3 Trends in regard to performance and power consumption

Despite the reduction in power consumption achieved by scaling-down the transistors, the increasing performance of the application processor, the increasing resolution of the display, the increasing speed of communication, and the exponential increase in data traffic are causing the total power consumption of a smartphone to trend upwards. This means that battery life and heat generation are becoming major concerns. Since smartphones are expected to be compact and thin, their planar and cubic dimensions are typically small. This means that, to avoid having a heat-generation problem, they should have effective heat dissipation during continuous use at an average power consumption of 2.5 to 3 W (**Figure 4**). Although various ways have been found to save power for feature phones, further efforts are necessary for smartphones.

Increasing the number of CPU cores is not simply a matter of increasing the number; it also involves changing the architecture (such as further decreasing power consumption by mounting a combination of

cores with low power consumption). Two technologies are available that support these efforts.

- variable symmetric multiprocessing (vSMP)
- big.LITTLE processing (concurrent use of high-performance core[s] and power-saving core[s])

With these technologies, the combination of high-performance and power-saving cores is optimized in accordance with the load scenario (light load or heavy load) so as to suppress total power consumption. They are described in detail in the following section.

3. Power-saving technologies

The power-saving technologies incorporated in the application processor and the control software for that technology are described in the following two subsections.

3.1 Application processor

Reducing the power consumption of the application processor involves two approaches. The first approach is to improve the hardware (namely, reducing the semiconductor-process design rules and adopting new architectures); the second approach is to reduce the operating frequency and operating voltage of the processor and to reduce its power consumption in accordance with demand by means of multi-core control. Several power-saving technologies have been incorporated into many application processors.

1) Clock gating and power gating

The power consumption of the application processor is generally reduced by using gating clocks (i.e., clock gating) while operation of the module has stopped and by shutting off the clock supply to the circuits for a short time period. Furthermore, dividing the application processor into power-supply domains, as illustrated in **Figure 5**, enables the use of a power-gating function for blocking the power supply to each domain.

This clock-gating function saves power in accordance with the use case of the application scenario by reducing the leakage current of inactive circuits (by blocking the power supply of the corresponding clock-gated circuit) and by reducing the power wasted during standby (when internal circuits are inactive). Moreover, separating the power supplied to each core within the multi-core CPU makes it possible to perform power gating for each core (Figure 5).

2) Dynamic voltage and frequency scaling

The dynamic voltage and frequency scaling (DVFS) function dynamically changes the operating voltage and frequency of the application processor for each power-supply domain. Appropriate control of these parameters results in power saving. Although power consumption can be suppressed by reducing the

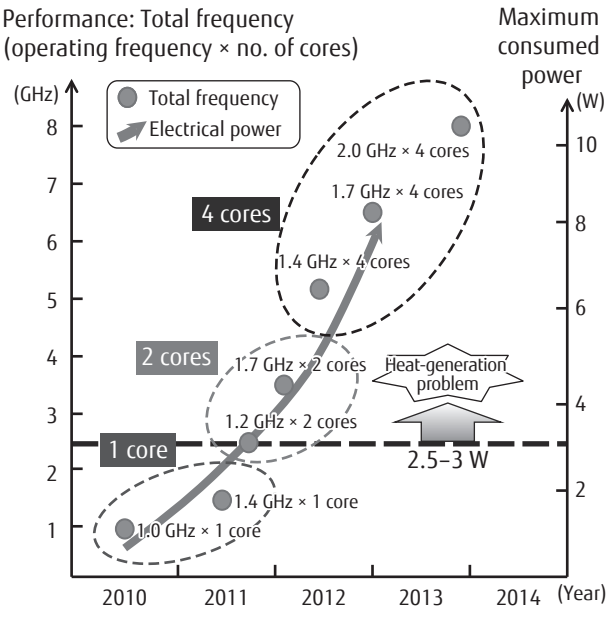


Figure 4
Trends in performance and power consumption.

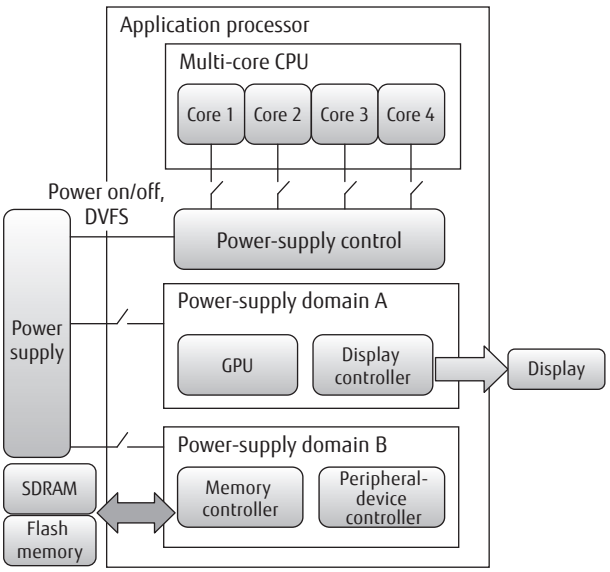


Figure 5
Power gating.

voltages, if the voltage is lowered, the frequency must be reduced to a level at which the processor is operable. This combination of voltage and operation frequency at which the processor is operable depends on the specifications of the application processor (process rules, etc.). Multiple operation points are generally set for each frequency, and stepwise changes in voltage are made accordingly (**Figure 6**).

3) Concurrent use of high-performance core(s) and power-saving core(s)

One way to achieve high performance and power saving using a multi-core configuration is to use NVIDIA's vSMP technology for optimally controlling the high-performance and power-saving cores in combination. The vSMP architecture combines four high-performance cores and one power-saving core,[1] and power is saved by dynamically switching operation to the core or cores most suited to the application scenario.

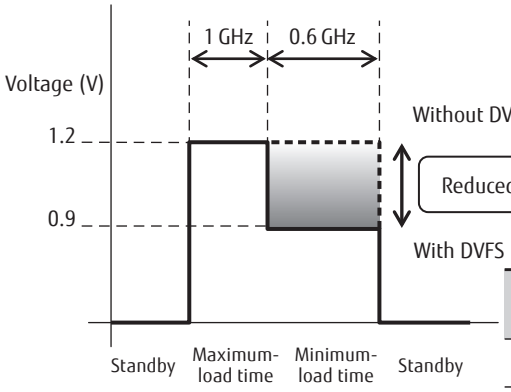
For a scenario that does not require high performance, only the power-saving core (using low-speed transistors) is operated, resulting in low power consumption. For one that requires high-speed processing, one or more high-performance cores (using high-speed transistors) are operated, resulting in high processing performance. The next-generation architecture, ARM's big.LITTLE technology, is becoming mainstream.[2] Processing requiring high performance is done on a high-performance core with a long pipeline and a high degree of parallelism while processing not requiring high performance is done on a power-saving core (with high power efficiency) with a short pipeline. In the latter case, performance is maintained while total power consumption is reduced.

3.2 CPU cores

As mentioned above, 30 to 50% of the power consumption of a smartphone is accounted for by the application processor. Most of that amount is accounted for by the CPU cores. Accordingly, reducing CPU core power consumption is vital to extending battery life. A widely used approach to achieving this is to switch to sleep or stand-by mode when there are no tasks to process. However, this approach is not sufficient for smartphones due to the increase in performance of the application processor. Power saving is thus achieved by dynamically controlling the CPU operating frequency and number of cores operating in accordance with the processing performance required by the application to be processed.

1) Controlling CPU operating frequency

The operating frequency of the CPU used in Fujitsu smartphones is controlled by a function in the Linux framework of the Android OS. Three control modes are provided: a performance-oriented mode, a power-saving-oriented mode, and a low-latency mode (providing fast response to CPU load). The basic parameters for these control modes are the timing of the operating frequency transition and the magnitude and duration of the up or down step applied to the operating frequency. Both are key factors for optimization. The load on the CPU is monitored for a certain period of time,



Operating frequency	Operating voltage with DVFS	Operating voltage without DVFS
1 GHz	1.2 V	1.2 V
0.6 GHz	0.9 V	1.2 V

Figure 6
Principle of power reduction by DVFS.

and the operating frequency transition is set accordingly. In particular, it is necessary to ensure a balance between user interface operability and power saving and to tune them optimally. The operating frequency should be varied in accordance with the performance required by the current application so as to avoid power wastage.

2) Multi-core control

Multi-core control improves processing performance without increasing the operating frequency by increasing or decreasing the number of cores in use in response to the current load on the CPU. It controls the transitions among the high-performance cores and the power-saving core. More specifically, the increase or decrease in the number and mix of operating cores is determined on the basis of the current load on the CPU and an arbitrary threshold value, and the power supplies to the cores are turned on or off accordingly. Controlling the power supplied to the CPU cores in such a manner that they are turned on when multiple tasks are executed and turned off immediately when the tasks have been executed results in power saving. This combination of controlling the number and mix of operating cores and their operating timing is the key to achieving power saving for smartphones.

4. Efforts of Fujitsu

Fujitsu is putting to practical use the mechanisms described above and is implementing an optimal tuning of performance and power saving.

1) Analysis of power consumption in CPU cores

To minimize the power supplied to the CPU cores, it is essential to acquire basic data on power consumption in relation to the operating frequency and number of operating cores. These data are needed for controlling the operating frequency so that it matches the performance and power characteristic of the CPU cores as well as to control the number and mix of cores in operation. It is thus necessary to identify the frequency (i.e., the point) at which power efficiency (i.e., the balance between power saving and performance) is maximized. Such an analysis is illustrated in **Figure 7**.

Moreover, battery power is monitored, and the control method is switched accordingly between controlling the CPU operating frequency and controlling the number of cores in operation. When the remaining battery life drops below a threshold, control is executed in a manner that shifts to the power-saving side in a stepwise manner so that the remaining battery life is extended.

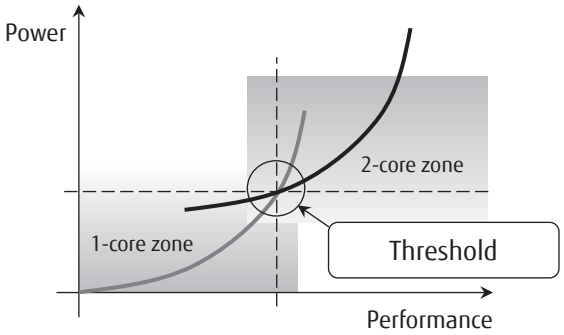


Figure 7
Power consumption vs. performance analysis.

2) Utilization of power-saving core

The high-performance cores and power-saving core are used in combination, as described above, and the difference in performance is utilized in accordance with the processing required by the current application. When high processing performance is required, processing is done on the high-performance cores, and when low processing performance is required, processing is done on the power-saving core (with high power efficiency). For example, when low processing performance is sufficient (e.g., when displaying home pages, browsing e-mails, and playing music), the power-saving (low-power-consumption) core is used, and when high processing performance is required (e.g., when using browsing software and playing games), one or more high-performance cores are used. In this manner, the CPU operating frequency and number of cores are controlled, and the performance level and power saving are optimized.

3) Tuning of each application

The operating frequency of the CPU cores is controlled on the basis of the performance required by each application. For example, in the case of watching one-seg TV broadcasts, playing movies, and so on, although high processing performance is not required, the minimum required processing performance must be ensured. That is, by maintaining a minimum operating frequency and adjusting the frequency so that it does not easily shift to high frequency, the viewing time can be maintained at almost the same level.

4) Optimization of user-interface performance

Since smartphones are operated by using a touch-screen, power saving and operability are improved by implementing a mechanism by which a "touch event" (i.e., touching the screen with a finger) triggers an increase in the CPU-core operating frequency. The operating frequency instantly increases to the minimum clock frequency that ensures comfortable user handleability, and adequate performance during operation is ensured by keeping that frequency constant.

It is necessary to consider the balance between performance and power saving, and the display resolution and processing volume (depending on the application being processed) vary during the period that the operating frequency is kept constant, so they are optimized. Fujitsu is working to achieve power saving by exploiting CPU-operating-frequency control and multi-core control as well as power-saving technologies (such as utilizing a power-saving core) in our effort to develop smartphone hardware platforms that achieve both high performance and energy saving.

5. Conclusion

This paper has described the evolution of the application processor used on the high-performance hardware platform supporting Fujitsu's smartphones and the technologies used for reducing the power requirements. It also described Fujitsu efforts towards achieving high performance and low power consumption.

The processing performance demanded of smartphones will continue to increase, so the application software and hardware platform will become even more closely integrated. This means that efforts to achieve a balance between performance, functionality, and power saving will become more and more important.

References

1) NVIDIA Inc., "Power-saving core". *http://www.nvidia.com/content/PDF/tegra_white_papers/tegra-whitepaper-0911b.pdf*
2) ARM Ltd., "big.LITTLE". *http://www.arm.com/products/processors/technologies/bigLITTLEprocessing.php*

Toru Ogawa
Fujitsu Ltd.
Mr. Ogawa is engaged in developing smartphone hardware platforms.

Kenichi Ito
Fujitsu Ltd.
Mr. Ito is engaged in developing smartphone hardware platforms.

Koji Matsushima
Fujitsu Ltd.
Mr. Matsushima is engaged in developing smartphone hardware platforms.