Packaging Technology for Image-Processing LSI

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The main function of a semiconductor package is to reliably transmit electric signals from minute electrode pads formed on an LSI chip (semiconductor chip) to the mounted terminals of the semiconductor package. To ensure a good LSI performance, it is becoming important to optimize the package structure according to the characteristics of the LSI and product use environment. Image-processing LSIs must process a large amount of image data at high speeds, which makes it necessary to have high-speed, high-quality data communication with a high-capacity external buffer memory. Semiconductor package structures are becoming more elaborate so that such LSIs can reliably perform these operations. Image-processing LSIs are used in mobile devices such as digital cameras, mobile phones, and smartphones, and they adopt high-density mounting technologies including packaging technology to miniaturize them and give them a system in package (SiP) structure with mixed mounting of multiple LSIs. This paper presents advanced semiconductor packaging technologies used in semiconductor packages for image-processing LSIs.

1. Introduction

The fundamental functions of a semiconductor package include reliable transmission of electric signals from minute electrode pads formed on an LSI chip (semiconductor chip) to the mounted terminals of the semiconductor package and protection of the fragile silicon chip on which a minute circuit is formed from the external environment.

In addition to these fundamental functions, packages have recently been undergoing physical changes including miniaturization and adoption of multi-terminal and area array structures to meet the demand of electronic devices on which they are mounted. They have also made significant progress in terms of functionality, including support for transmission characteristics in accordance with interfaces that are becoming increasingly high-speed such as USB 3.0, PCI Express, and DDR3, and heat release property for effectively releasing heat generated by LSI chips.

Image-processing LSIs are in wide use for mobile and stationary device applications and there is a diverse range of semiconductor packages that fill their needs. For example, fine-pitch ball grid array (FBGA), which is commonly used for mobile devices, has a semiconductor chip sealed with epoxy resin and the electrode pads (Al pads) on the semiconductor chip surface are connected with a printed circuit board (package interposer) by means of thin metallic wires (Au or Cu wires) as shown in **Figure 1**. In this way, electric signals are connected via the package interposer to the mounted terminals in the shape of balls (solder balls). The electrode pads of a semiconductor chip are arranged at a pitch of about 40 μm at the minimum and the minimum terminal pitch of the main board is 0.4 mm. It is important to use wire bonding and a package interposer for expansion to fill this dimensional gap.

This paper describes semiconductor packages used for image-processing LSIs and mounting technologies.

2. Mounting technology trends

Figure 2 shows typical packages used for image-processing LSIs. They all are of a surface mounted type and have terminals arranged in the shape of a grid on the bottom surface of a semiconductor package (area array arrangement) to allow multi-pin structures and miniaturization.

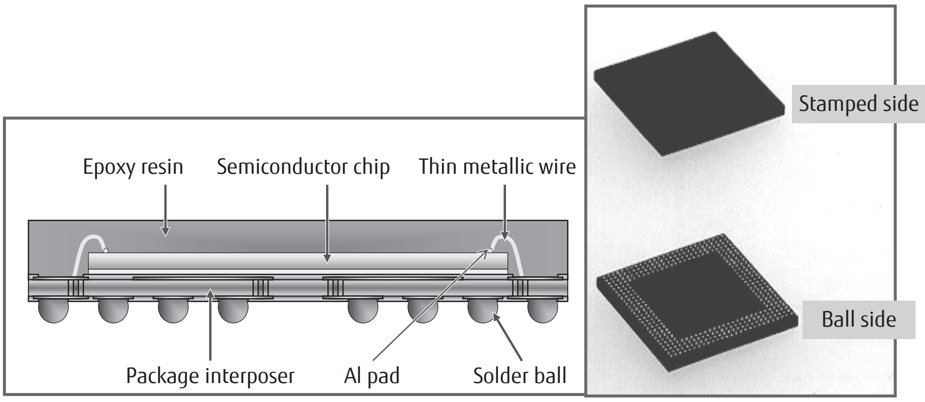
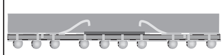
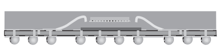
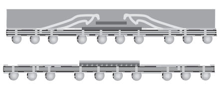
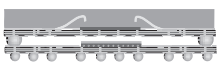
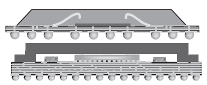


Figure 1
FBGA structure.

Type	Structure	Characteristics	Application
WL-CSP Bumped Die		Up to 300 pins Minimum size (area, height)	Mobile phones Smartphones
FBGA		Up to around 500 pins	Digital cameras (low-end)
PoP FBGA (SiP)		Integrated with memory (SiP)	Digital cameras (high-end)
FBGA (SiP) PoP		Optimized memory size	Digital single-lens reflex cameras
FBGA (SiP) PoP		Top package may have CoC structure	Camcorders
PBGA FCBGA		Up to 1000 pins High-speed processing CoC, multi-pin, high heat release property	Digital TVs Amusement devices

Camcorder: Portable video camera and videocasette recorder

Figure 2
Packages for image-processing LSIs.

Figure 3 shows the roadmap for semiconductor packages. The evolution of semiconductor packages can be roughly classified into miniaturization and thinning for mobile electronic devices such as mobile phones/smartphones and digital cameras/camcorders; multi-terminal structures intended for stationary electronic devices such as digital devices including digital TVs and hard disk recorders and desktop PCs; and performance enhancement aimed at improving signal transmission quality and heat release property. An extension of this is high integration, which structures a subsystem by incorporating some of the peripheral circuits on the main board into the package. This incorporates image-processing and peripheral LSIs and components into one package and offers superior functions as compared with mounting in individual packages. Systems in package (SiPs) and modules fall under in this category and contribute to functional enhancement and miniaturization of products.

3. Trends in development of packages for mobile devices

While functional enhancement is demanded of mobile devices, they have also become increasingly

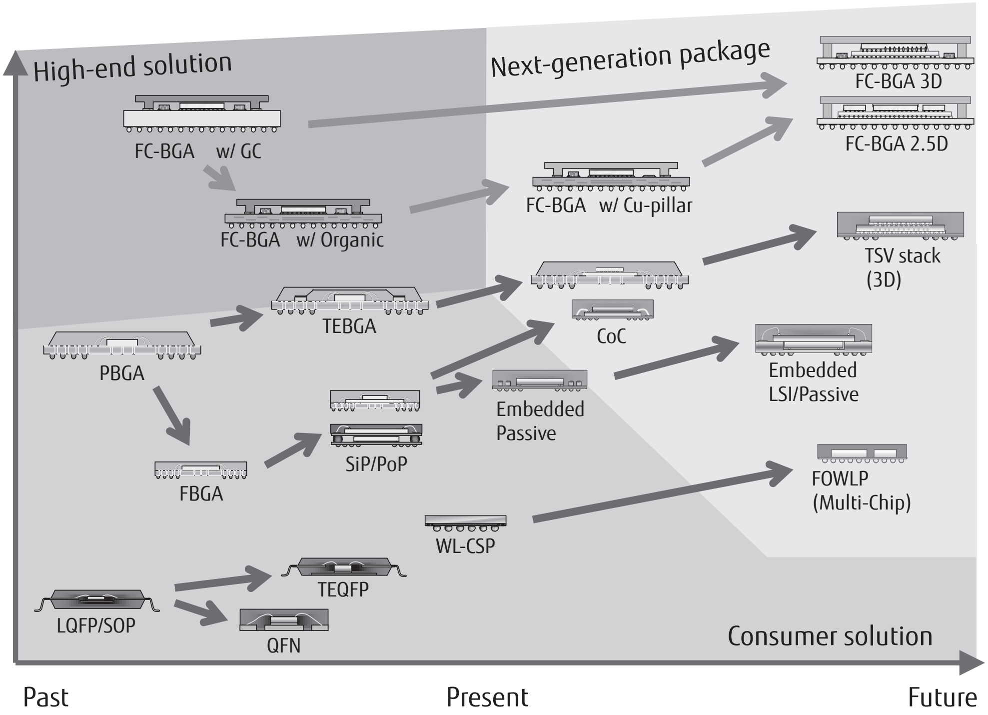


Figure 3
Roadmap for semiconductor packages.

miniaturized and lightweight. Accordingly, to satisfy the need for integrating the required number of electronic devices within housing that has a limited space, advanced mounting technologies are required also for semiconductor packages.

To reduce the size of mobile phones, ball grid array (BGA) that uses a flexible printed circuit (FPC) board was developed in the mid-1990s, and it has led to smaller mounting areas and volumes. Miniaturization has further progressed and FBGA that uses a package interposer is now the mainstream. Main boards of mobile phones are also increasingly multilayered and fine-structured and semiconductor packages are manufactured accordingly with a terminal pitch of about 0.4 mm and with terminals of up to about 1000 pins.

Electronic devices are being further miniaturized and high integration is positively implemented to reduce the mounting areas. Commercialization of SiPs and modules integrating multiple semiconductor chips and passive components in one package is under way as in combinations of different types of memory such as flash memory and DRAM or of memory and passive components, which mainly include logic devices. In this way, various elemental technologies are developed such as semiconductor chip thinning technology that allows a combination of various devices, interconnect technology (flip chip mounting and wire bonding) and use of package interposers accommodating fine wiring.

4. Structures and functions of packages for mobile devices

In mobile devices, image-processing LSIs are mounted in the main board and camera module of the device's main units as still and moving image processing engines. In general, they are essentially required to be compact and thin and the areas in which they are mounted have been reduced by using area array-type packages. There are several area array-type structures and different package structures are used depending on the LSI circuit scale and application. The following describes package structures for different applications and their functions.

4.1 For mobile phones and smartphones

For mobile phones and smartphones, FBGA mentioned above, wafer-level chip size package (WL-CSP) and bumped die package are used. FBGA packages are increasingly implemented as SiPs.

WL-CSP involves packaging at wafer level and the wafer is made into chips at the end, which provides an outer shape of the real chip size, resulting in the smallest possible package (**Figure 4**). It is adopted for devices with up to about 300 pins and is characterized by its small size and light weight, which makes it suitable for mobile devices. WL-CSP allows Cu plating to be used to form a short connection between the electrode pads of a semiconductor chip and terminals via rewiring. Accordingly, it offers low wiring inductance and is suitable for devices that handle high-speed signals.

4.2 For digital cameras

For digital cameras, FBGA is used when an image-processing LSI is mounted independently and FBGA SiP and package on package (PoP) structures are used when memory is mounted in combination. Digital cameras require high-capacity memory so that they can process image data at high speed [**Figure 5 (a), (b)**]. With a system-on-a-chip (SoC), which has a memory circuit mounted in combination within a chip, the chip area is unavoidably large and the effect of yield is significant. For optimization, a structure with mixed mounting of a logic device and memory within a package is often adopted. In a PoP structure, a logic device and memory are separately packaged and tested, after which they are stacked [**Figure 5 (c)**]. It has a major benefit of reducing one package's worth of mounting area by stacking two packages. In addition, for image-processing LSIs, it allows memory size to be selected

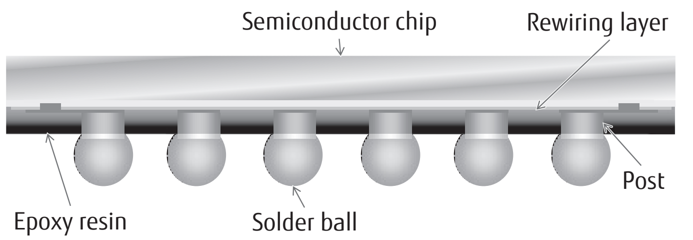


Figure 4
WL-CSP structure.

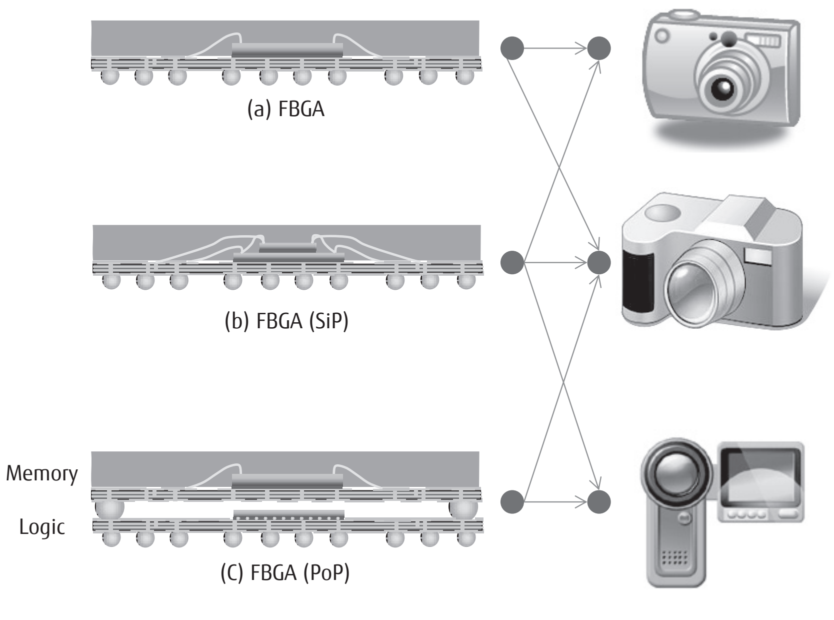


Figure 5
Packages for cameras.

according to the application. It means, for example, the same image-processing LSI can be used with different sizes of memory for multiple applications. Recently, memory products for PoP structures have come to be sold by memory vendors and have become widespread.

4.3 For camcorders

For camcorders, FBGA (single chip), SiP structures and PoP structures are often selected, as with for digital cameras. As compared with digital cameras, they require a high video processing capability and have to handle more signals, which means the packages for them tend to have multi-pin structures. In addition, memory that is to function as the data processing buffer is also tending to become bigger and faster. To meet these needs, SiP structures are increasingly adopted because they have a higher data transfer rate between the memory and image-processing LSI.

5. Mounting technologies for high-performance devices

Many stationary devices are mainly intended for video processing as represented by set-top boxes (STBs) and digital TVs. Accordingly, LSIs with a higher video processing capability than those for mobile devices are often used. LSIs for car navigation systems require high-reliability packages for reasons of their use environment. Packages that meet the needs of these applications are positioned here as packages for high-performance devices and the following explains their technologies and structures.

Image-processing LSIs for digital TVs and amusement applications operate at higher speeds than those for mobile devices and have a larger power consumption. For this reason, plastic ball grid array (PGBA), which has more margins in the package design, is often used. It features wider terminal pitches than FBGA and, while it is larger as a package, it is advantageous in terms of heat release and is used for LSIs for car navigation systems and digital TVs.

For applications that require even higher heat release property and higher-speed signal transmission, flip chip BGA (FCBGA) is adopted. Flip chip technology, which uses metal bumps to allow an LSI and package interposer to be connected over the minimum distance and many metal bumps to be provided in a chip, excels in terms of stability of power supply. In addition, it allows a heat release mechanism (such as heat dissipation fins and heat pipes), which dissipates the heat generated from a semiconductor chip for cooling, to be provided directly on the back of an LSI. FCBGA that makes use of these assembly technologies and high-speed signal transmission design technologies are used in the over 1000-pin region.

6. Latest packaging technologies

As the processing performance of LSIs has been improving in recent years, I/O terminals of semiconductor chips are tending to see a greater number of pins and undergo miniaturization, which makes interconnects between semiconductor chips and package interposers minute. For that reason, the amount of current per cross-section tends to increase and technology to address this issue is called for.

In addition, processing speeds and amounts of data to be processed are expected to increase in the future as they have up to now and packaging technologies to keep pace with them are also progressing.

The following presents these packaging technologies.

6.1 Flip chip methods

In common packages, semiconductor chips and package interposers are connected by wire bonding. To reduce the size of packages, however, flip chip technology is used for an increasing number of packages. Flip chip technology offers different methods of connection and Fujitsu Semiconductor selects from among several methods depending on the application (**Figure 6**).

The Au bump connection method is used for consumer products. This method features high throughput during manufacturing and it can handle a narrow pitch region (45 μm pitch), which is impossible with the controlled collapse chip connection (C4) method.

For high-performance devices, the C4 method is used for bump connection of a few thousand terminals. In the C4 method, solder bumps arranged in a planar manner are heated so that they melt and form a metal joint between the package imposer and semiconductor chip. As bumps are arranged in a planar manner, power can be supplied to the circuit at the center of the chip via short wiring, which makes this method capable of accommodating high-speed, high-performance chips.

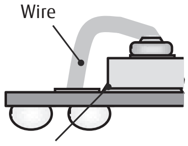
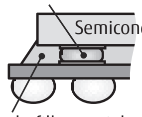
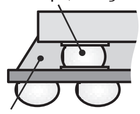
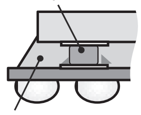
Name of method	Wire bonding	Au bump	Solder bump (C4)	Cu pillar
Joint structure				
Description	Metal joining by metal-to-metal diffusion via thermosonic and thermocompression bonding	Connection with interposer by Au bumps	Metal joining by molten solder	Accommodation of multi-pin structures by application of Cu pillars (under development)
Application	General	consumer devices	consumer/high-end devices	consumer/high-end devices

Figure 6
Comparison of flip chip connection technologies.

6.2 Cu pillar flip chip technology

Means of connection between semiconductor chips and package imposers that have been used other than wires include Au bumps and solder bumps. However, the expected future high integration of chips increases the number of terminals to be connected and decreases the pitch of the corresponding pads. This is beginning to make it difficult to ensure stable connection with the conventional technologies. One technology for avoiding this problem is flip chip technology that makes use of Cu pillars, in which plating is used to form Cu pillars on the terminals of a chip for connection with the package interposer. Because Cu pillars are formed by plating, fine pitches are supported. In addition, Cu is used as the material, and it accommodates larger currents than Au and solder. Furthermore, the amount of solder fed can be reduced in the Cu pillar method, which allows a finer bump pitch than in other methods.

This flip chip technology that uses Cu pillars is expected to be positively adopted for image-processing LSIs, which will be enhanced in terms of performance in the future.

6.3 Chip on chip (CoC) structure

While transmission with memory connected to image-processing LSIs will need to be faster in the future, there is also a demand for reduced power consumption. Accordingly, CoC technology, which connects wide-bus memory capable of reducing interface power consumption, has been developed. It has already been standardized by the JEDEC[1] as Wide I/O and use of this allows flip chip connection between an image-processing LSI and memory chip by means of terminals of about 1000 bumps, which ensures wide bandwidth. In addition, short transmission lines allow the driving force of drivers to be decreased, which contributes to the reduction of power consumption.

As a technology in the near future, 3D mounting technology that uses the through silicon via (TSV) stacking technology is being developed. It uses TSV stacking to achieve larger memory sizes without changing process technologies.

In the future, we intend to integrate the TSV and CoC technologies to realize even higher density.

7. Conclusion

This paper has presented semiconductor packaging technologies used for image-processing LSIs.

Semiconductor packaging technologies assume an important role of connecting LSI chips and customers' products. At Fujitsu Semiconductor, we consider it our duty to proceed with the development of optimum packaging technologies based on a thorough understanding of customers' use environments so that we can provide them in the form of high-performance and easy-to-use devices.

Smartphones have been rapidly gaining popularity in place of mobile phones in the last year or two. Smartphones, which are characterized by high functionality, are posing new challenges in terms of packaging. We are committed to providing solutions to these challenges. As a means to do this, we will further develop packaging technologies such as higher integration by mixed mounting with devices other than LSIs; improved heat release property that accommodates performance enhancement of devices; and power consumption reduction to increase battery life times.

References

1) JEDEC.
http://www.jedec.org/

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