CHIP-PKG-PCB Co-Design Methodology

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For digital devices integrating an image-processing LSI, performance improvement, cost cutting and reduction of the time to market are essential conditions for surviving in the increasingly competitive global market. At the same time, more and more image-processing LSIs are taking the form of large-scale system-on-a-chip (SoC). It is becoming harder to design them as the degree of integration increases, and signal and power integrity issues are appearing due to their processing speed increase and voltage reduction. As a design methodology to address four challenges in recent SoC design (signal and power integrity issues, high-density design, reduction of design turnaround time [TAT], and cost cutting), Fujitsu Semiconductor has established chip-package-printed circuit board (CHIP-PKG-PCB) co-design methodology and made achievements contributing to first-shot full operation of SoCs and digital devices that integrate them. This paper presents our approach to the CHIP-PKG-PCB co-design for dealing with the four challenges above by giving case examples.

1. Introduction

As smartphones and tablet devices become widespread and network infrastructure established, high-definition images and videos have become available for viewing outside the home or workplace. At home, high-definition videos containing large volumes of information are recorded and viewed along with the diffusion of flat-screen TVs and transition to digital terrestrial broadcasting. In the field of automobiles, navigation systems and dashboard panels are being used to display various types of information and there have even been systems announced in recent years that analyze camera images so that vehicles can avoid collisions.

In these fields, there is a need for sending and receiving massive amounts of image and video information at high speeds and analyzing them, and this is made possible with various types of image-processing LSIs. Imaging LSIs must offer diverse functions and high computational performance and they are designed as large-scale system-on-a-chip (SoC) that make use of a microfabrication process with high levels of integration.

SoCs have so far been significantly improved in terms of functionality and performance by miniaturization. Along with this improvement, circuits kept growing in speed and scale and the power supply voltages have been repeatedly reduced so as to restrain the ever-increasing power consumption. Recently, the increased speed and lower voltage of SoCs have decreased their margins to noise, which has made designing them very difficult. In addition, image-processing LSIs are often mounted in mobile devices and designing small packages and printed circuit boards is increasingly important for reducing the size of the devices themselves and ensuring sufficient space for a battery. Furthermore, for these devices to survive in the increasingly competitive global market, bringing high-performance products to market as quickly as possible is an essential condition.

Four issues have emerged in recent years:

1) Signal and power integrity issues
2) Realization of high-density design (light, thin, short and small)
3) Reduction of design turnaround time (TAT)
4) Cost cutting

Chip-package-printed circuit board (CHIP-PKG-PCB) co-design has been attracting attention recently as a design methodology that solves these issues.

CHIP-PKG-PCB co-design is a style that visualizes an image of a design encompassing CHIP, PKG and PCB from the initial phase of design to improve its accuracy while identifying problems and dealing with them. Fujitsu Semiconductor has been adopting this design style since around 2003 and achieved results in the development of SoCs and the digital devices in which they are mounted.[1)]

This paper describes issues with CHIP-PKG-PCB co-design together with examples of their solutions and its effects.

2. Signal and power integrity issues

Around 2002, when DDR-SDRAM started to become widespread as external memory of SoCs, Fujitsu Semiconductor faced a difficulty: It became increasingly difficult to build SoCs that achieved the required performance because signal and power wiring, which only needed to be connected to be made functional until then, generated significant crosstalk and simultaneous switching noise in the input/output (IO) with the existing design. The signal waveform was distorted and thus failed to satisfy standards. In addition, the power supply voltage, which was supposed to be constant, varied due to the operation of the SoC itself or incoming external noise, and this caused unexpected shifts in the timing of circuit operations. These emerged as various types of noise shown in **Figure 1** and caused problems in design sites.

2.1 Signal integrity issues

Crosstalk noise (Figure 1) is related to multiple design parameters across the CHIP, PKG, and PCB including the layout, drive capability, and operation patterns of the IO buffer in the CHIP, wiring routes in the PKG, and wiring routes in the PCB. For that reason, it is desirable to model the whole device to investigate the optimum values of the respective design parameters.

Accordingly, we developed a high-accuracy simulation model that allows designers to study design parameters from the initial phase of design, as shown in **Figure 2 (a)**. **Figure 2 (b)** is an example of analysis that uses this model. To verify the accuracy, two PKG samples were prepared: one with and one without a shield pattern that was included as a measure to combat crosstalk noise. The results were compared with the actual measurement. The solid black waveform lines indicate the results of the simulation and the grey wave ones show the measured results. Both lines coincide well with the actual measurement, showing that the crosstalk noise is represented with high accuracy. By conducting this type of simulation during prototyping in the initial phase of design, sensitivities associated with the respective parameters of the CHIP, PKG and PCB can be identified. It allows designers to derive appropriate design constraints for detailed design, and produces effects such as noise reduction and decrease of reworking.

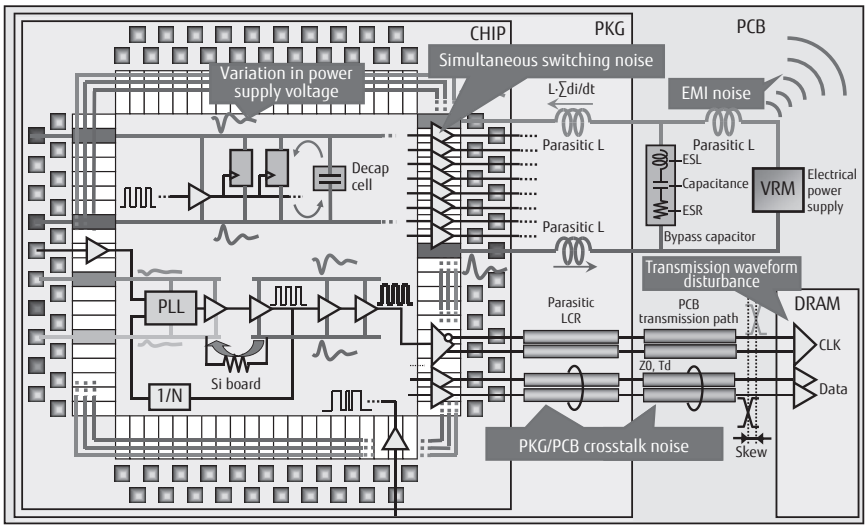


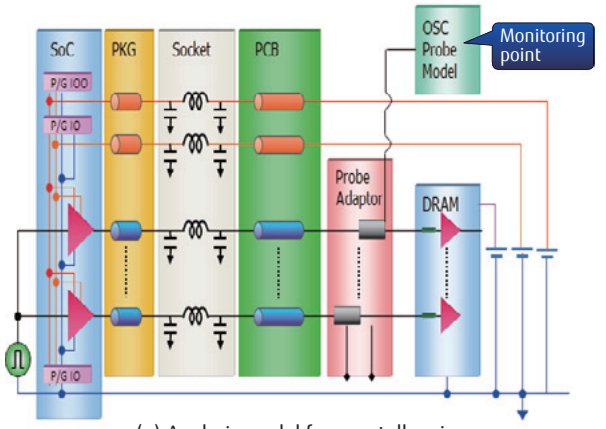
Figure 1
Noise generated in CHIP, PKG and PCB.

2.2 Power integrity issues

For stable operation of an SoC, it should be designed to have a low power supply impedance. In reality, however, there is a resonance frequency with high impedance arising from the parasitic LCR of the CHIP, PKG and PCB and any operating current near this resonance frequency often causes large noise, resulting in faulty operation. The frequency at which this resonance occurs and its magnitude cannot be correctly estimated without taking all of the CHIP, PKG and PCB into account.

To address this issue, we developed a methodology for analyzing power supply impedance by connecting integrated modeling of CHIP, PKG and PCB.[2] **Figure 3 (a)** is a result of verifying the accuracy of some analysis that uses this methodology.

We prepared PCB samples with different numbers of bypass capacitors and verified the accuracy by simulation and actual measurement. **Figure 3 (b)** indicates the result of its transient analysis showing the effect of optimization of PCB bypass capacitors. The optimization reduces the variation of the power supply voltage. The effect of bypass capacitor optimization in impedance analysis was also confirmed by transient analysis.



(a) Analysis model for crosstalk noise

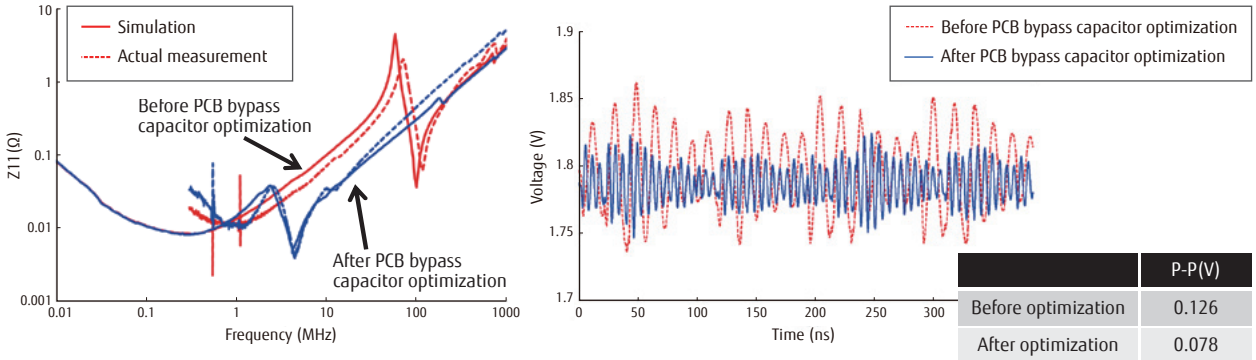
(b) Effect of measure for crosstalk noise

Figure 2
High-accuracy simulation model and example of analysis.

3. Realization of high-density design

To reduce the size of PKG and PCB by having a high-density design, it is important to coordinate the LSI pad and PKG ball layout with the component layout and wiring of the PCB. This should be carefully thought out in the initial phase of design. Otherwise, many wiring crossings are generated in detailed design, and this means vias have to be provided at points where the wiring layers change for crossing. It may lead to a degradation of impedance characteristics, a larger total amount of PKG and PCB wiring and an increase of wiring area, resulting in disadvantages in terms of performance and cost.

Accordingly, we have developed a methodology



(a) Impedance analysis of power supply

(b) Transient analysis of power supply noise

Figure 3
Power integrity analysis.

that allows designers to study an LSI pad and PKG ball layout while ensuring an overall view of the CHIP, PKG and PCB as shown in **Figure 4 (a)**. This methodology provides an overall picture of the wiring routes from an SoC to the device connected, making it possible to determine the optimum pad and ball layout. **Figure 4 (b)** shows an example of studying a PCB portion that needs to have especially high performance, based on the overall image of the CHIP, PKG and PCB investigated in Figure 4 (a). Assignment adjustment has already been made based on an overall picture, and this has made it easier to create detailed wiring. **Figure 4 (c)**, which is the completed detailed wiring, shows that it is realized in accordance with the image in the initial phase of design [Figure 4 (a)].

A similar study is conducted on the wiring in the PKG at around the same time to study the whole picture while incorporating fine adjustments of the ball layout resulting from PKG wireability and LSI floor plan information so as to reduce the PKG size.

4. Reduction of design TAT

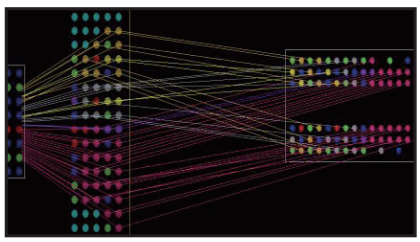
4.1 Extraction of PKG electrical characteristics by electromagnetic field analysis

Integrated analysis of CHIP, PKG and PCB for addressing signal and power integrity issues essentially requires high-accuracy extraction of PKG electrical characteristics.

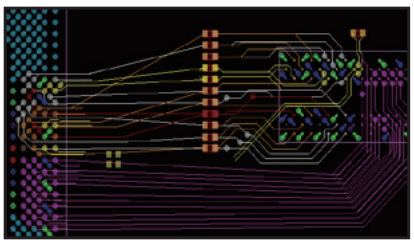
Traditionally, for a high-accuracy model, extraction is carried out by 3D electromagnetic field analysis mainly as an S-parameter model, and this required a very long TAT with a few tens of hours for one analysis. This made it impossible to test many schemes in the initial phase of design and caused a problem in terms of prototyping TAT.

To deal with this issue, we worked in close cooperation with tool vendors to replace electromagnetic field analysis tools, strengthen the computer resources (to eight CPUs from one CPU), automate PKG and PCB pattern capture and establish an environment for automating the configuration of various settings in electromagnetic field analysis.

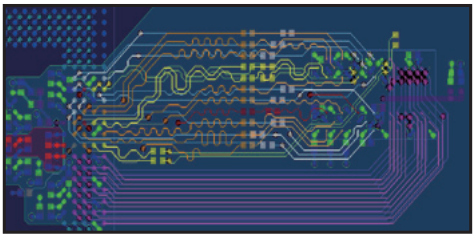
Figure 5 is an example of PKG board analysis. Figure 5 (a) indicates a PKG board pattern and Figure 5 (b) extraction accuracy and time. It shows that, in addition to the good coincidence with the actual measurement, the time required for extraction also has been significantly reduced to 1.7 h from the conventional 48 h. In this way, a short TAT has been achieved and many schemes can now be tested in the initial phase of design, which has allowed design constraints to be optimized for detailed design.[3)]



(a) Study of LSI pad and PKG ball layout



(b) Study of PCB detailed wiring



(c) Result of PCB detailed wiring

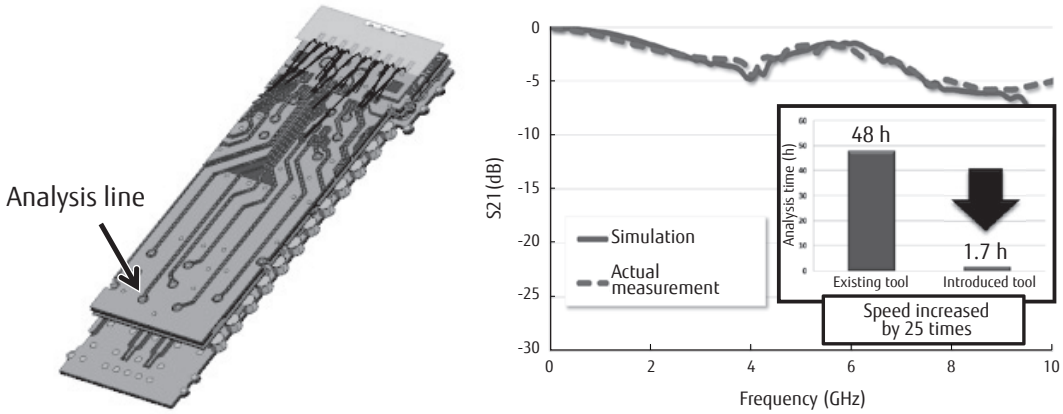
Figure 4
Study of layout and wiring in view of LSI, PKG and PCB.

4.2 Simultaneous switching noise analysis

Memory interfaces such as DDR3 have many IOs, and this may cause the issue of so-called simultaneous switching noise generated when the many IOs switch at the same time.

To analyze simultaneous switching noise, modeling similar to that in Figure 2 (a) mentioned above is carried out but the number of IO cells involved in switching can be as large as about 70. As memory interfaces have been growing in speed in recent years from DDR1 through DDR2 to DDR3, IO cells have become multifunctional. With DDR3 IOs, for example, the number of devices per cell amounts to a few tens of thousands for a transistor-level SPICE netlist, which has the highest accuracy. For this reason, the time required for high-accuracy simulation of simultaneous switching noise was in an ever increasing trend in inverse proportion to the interface speed increase.

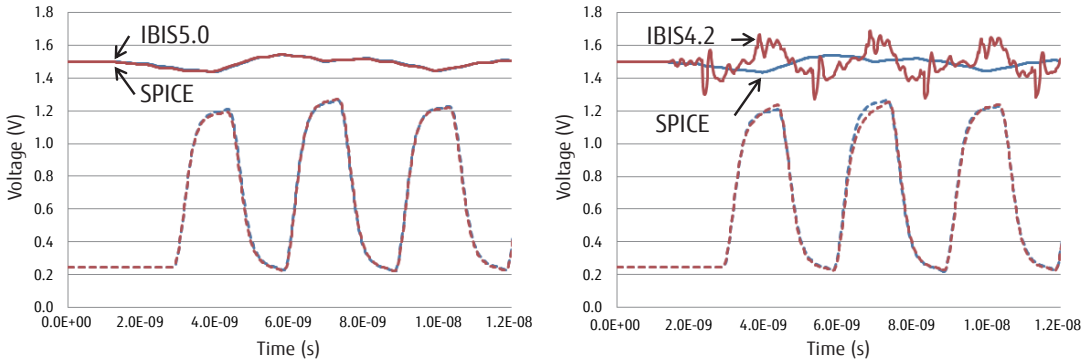
To deal with this issue, we have established an accuracy tuning methodology for IO cells in the IBIS 5.0 format, which is the latest version of IBIS, and a high-accuracy, high-speed simultaneous switching noise analysis methodology that uses it.[4] Regarding the accuracy, the result of analysis using a transistor-level SPICE netlist and that using IBIS 5.0 coincide well with each other as shown in **Figure 6 (a)**. The analysis time has been confirmed to be only 0.2 h when IBIS 5.0 is used, as opposed to 17 h with transistor-level



(a) PKG board

(b) PKG electrical characteristics

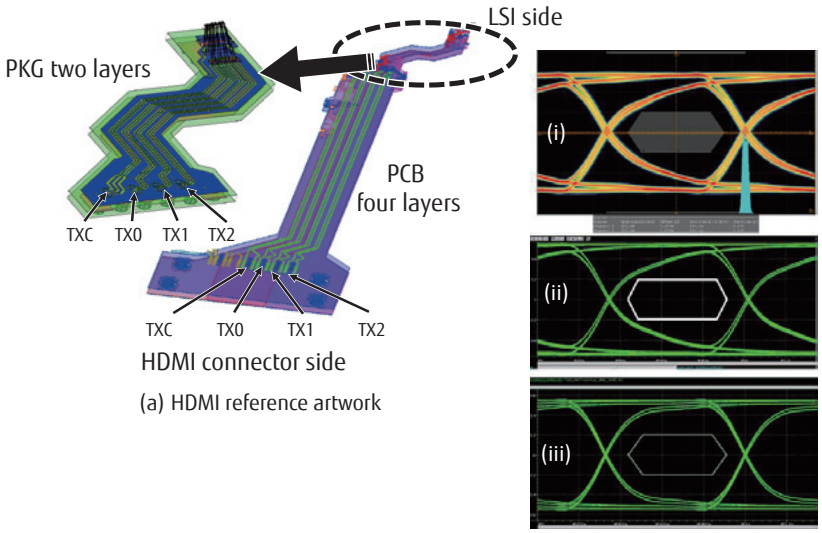
Figure 5
Example of electromagnetic field analysis of PKG board.



(a) Modeling by IBIS 5.0

(b) Modeling by IBIS 4.2

Figure 6
Difference in accuracy of different IBIS versions.



(a) HDMI reference artwork

(b) HDMI performance and cost optimization

Figure 7
Low-cost reference design of HDMI.

analysis. **Figure 6 (b)** shows the result of modeling in the IBIS 4.2 format, which is in widespread use. The specification of IBIS 4.2 does not allow the behavior of simultaneous switching noise to be represented and, if it is forced to be used for analysis, the accuracy cannot be ensured, as shown in the figure.

This is another technology that allows short-TAT simulation and helps designers to efficiently identify problems in prototyping that makes use of integrated analysis of CHIP, PKG and PCB in the initial phase of design.

5. Cost cutting

This section presents cost cutting of PKG and PCB of HDMI interface as an example of CHIP-PKG-PCB co-design.

For high-speed interfaces such as HDMI widely used for image-processing LSIs, we have made use of the modeling and analysis technologies described above to create a reference design for cost cutting.

Figure 7 (a) is HDMI reference artwork including a PKG with two layers and PCB with four layers intended for cutting cost by reducing the number of layers.

The result of comparison between simulation of this artwork and actual measurement with the test chip is shown in **Figure 7 (b)**. In the figure, (i) indicates the result of the actual measurement with the test chip and (ii) the result of simulation on the test chip. A comparison between (i) and (ii) shows that the simulation has sufficient accuracy. The result with the reference design in Figure 7 (a) using the simulation technique is shown in (iii). By tuning the design parameters, cost cutting by reducing the number of layers of PKG and PCB and improved noise immunity shown by even wider opening of the eye[note)] have been achieved at the same time.

6. Application of CHIP-PKG-PCB co-design

This section describes the activities for smooth application of the CHIP-PKG-PCB co-design technology to design sites to produce effects.

6.1 Allocation of coordinators

For implementation of CHIP-PKG-PCB co-design, Fujitsu Semiconductor dispatches engineers called coordinators with knowledge of co-design from its specialized department. Coordinators make proposals

note) The shape made by waveforms in Figure 7 (b) resembles an eye and it is generally called an eye. A thicker line forming the shape of an eye means more variation caused by noise, or a smaller margin. This is referred to as closing of an eye. Conversely, opening of an eye means thinning of the line, or increase of the margin.

to customers about what to do, by when, and to what extent, and take charge of design management until development is completed. In actual design, the schedule and constraint conditions may vary depending on factors such as whether it is new development or derivative development, and coordinating them is the key to success.

6.2 CHIP-PKG-PCB co-design service

Since 2004, Fujitsu Semiconductor has been offering a charged design service for customers that makes full use of CHIP-PKG-PCB co-design. It has produced effects such as reducing customers' PCB design periods by conducting PCB prototyping and various types of analysis for customers according to their PCB conditions, and decreasing noise suppression components by making use of integrated analysis. This service has been used by many set manufacturers so far.

7. Conclusion

This paper has presented issues with recent SoCs, which are being significantly improved in terms of functionality and performance, and described the effectiveness of CHIP-PKG-PCB co-design in solving those issues together with some examples.

For the future, there is an approach to improve the functionality and performance of image-processing LSIs not only by working on a single SoC but also by stacking multiple SoCs in a 3D fashion. We intend to apply CHIP-PKG-PCB co-design also to that approach so that we contribute to bringing high-performance products to market faster and in an inexpensive way.

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