Low-Power Technology for Image-Processing LSIs

● Yoshimi Asada

The conventional LSI design assumed power would be supplied uniformly to all parts of an LSI. For a design with multiple supply voltages and a power gating design, the inside of an LSI must be divided into multiple supply regions, and this complicates the LSI design. This paper introduces low-power technology applied to image-processing LSIs of Fujitsu Semiconductor, which designs such complicated LSIs with high reliability. Fujitsu Semiconductor engages in intensive development with CoolAdjust, a set of technologies to reduce power consumption by controlling power supply. Accordingly, this paper mainly focuses on describing technologies for a design that can handle multiple supply voltages and effectively reduce the dynamic power, and a power gating design that can effectively reduce the amount of leakage power. In a power gating design, when the power switch is turned on to supply power to a circuit, a large current called an inrush current runs so as to charge the parasitic capacitance of the circuit. It is known that this inrush current affects the circuits that are already powered on. This problem has been solved by controlling two types of power switches with a time interval, and this is also presented here.

1. Introduction

While the miniaturization of devices has tended to slow down in recent years, microfabrication with a size reduction of about 0.7 times has still been achieved every two years, which is equivalent to doubling the number of devices integrated per unit area of silicon every two years. Operating frequencies are also increasing and the trend is the same not only with LSIs for high-end systems but also with consumer LSIs and image-processing LSIs taken up in this special issue.

For image-processing LSIs for mobile devices, in particular, there is a strong demand for reduced power consumption from the perspective of battery life extension and weight reduction. Reducing power consumption is also demanded of image-processing LSIs for stationary devices as well as mobile devices in view of packaging and other implementation costs. Due to consumers' and organizations' recent increase in environmental awareness, there are also strong needs to reduce power consumption.

Against this trend toward greater power consumption caused by higher integration and performance of devices, there is a need to continuously provide solutions for low-power technology in order to meet the demand for lower power consumption from the viewpoint of the environment and restrictions on equipment.

Fujitsu Semiconductor is working on reducing power consumption in each of the hierarchical levels of design such as software design, high-level design, architecture design, logic design, circuit design, layout design and device process to reduce the power consumption of SoCs, as shown in **Figure 1**. It is known that taking measures in a higher-level hierarchy generally produces a greater power reduction effect. Meanwhile, low-power technologies applied in lower-level hierarchies are often independent of particular system configurations or designs and applicable to many types of LSIs.

Along with this approach to reducing power consumption, we are also working on power estimation CAD, which is a tool for evaluating the approach. Based on the results of LSI power analysis obtained by means of power estimation CAD, issues with power

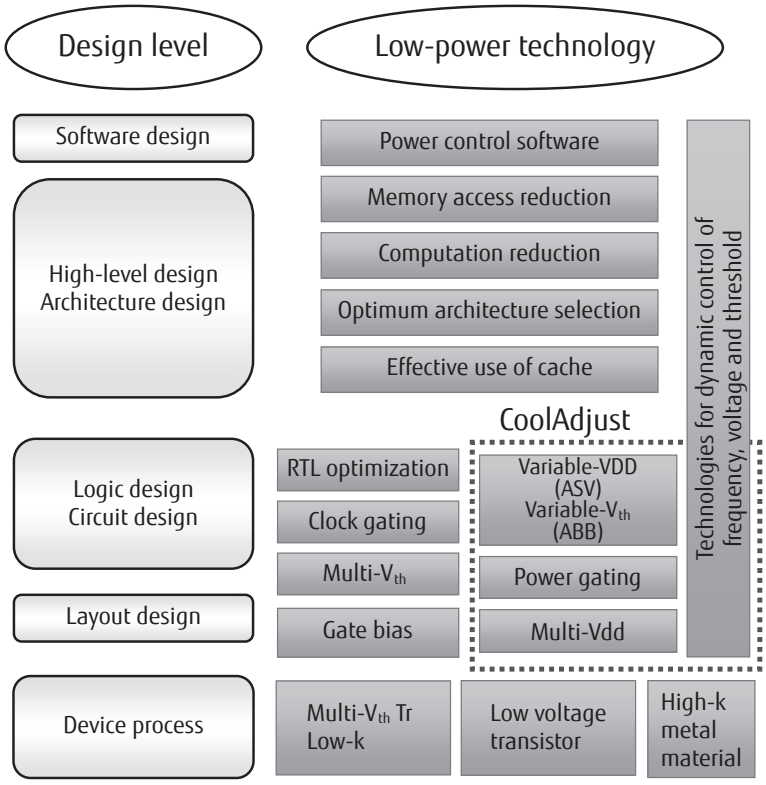


Figure 1
Low-power technologies for respective design hierarchies.

consumption can be identified. This is so-called "visualization of power consumption," and it is used as a means to identify problems from the perspective of power reduction and to take focused measures. This is described in "Verification of System LSIs for Image Processing" contained in this magazine.

This paper presents major low-power technologies applied to image-processing LSIs.

2. Power consumption trends

Figure 2 shows power consumption trends of SoCs including image-processing LSIs. This indicates power consumption with reference to the generation of the 180 nm process rule based on the assumption that 5-mm square LSIs have been realized for the respective generations without applying the low-power design technologies in Figure 1. It shows that, with the 40 nm generation, the dynamic power resulting from circuit operation increases to 6.9 times as much as the 180 nm generation and the leakage power consumed regardless of circuit operation increases to 31 times as much.

Reducing the power supply voltage makes an effective contribution to reducing LSI power consumption. Dynamic power is known to be proportional to the square of power supply voltage and successfully reducing the power supply voltage has a significant power reduction effect. Up to the 130 nm generation, power supply voltage was smoothly decreasing, which has made a great contribution to power consumption reduction. After the 130 nm generation, however, the typical power supply voltage has bottomed out at around 1 V mainly due to the restriction of low-voltage operation of SRAM. On the contrary, dynamic power increase has occurred because of higher integration and operation frequencies. In addition, increase of leakage power resulting from increased integration and process variation is becoming serious.

Fujitsu Semiconductor has systematized a series of low-power design technologies for reducing power by controlling power supply as CoolAdjust and is committed to its development. For image-processing LSIs, a design that can handle multiple supply voltages and power gating design of CoolAdjust are applied, and

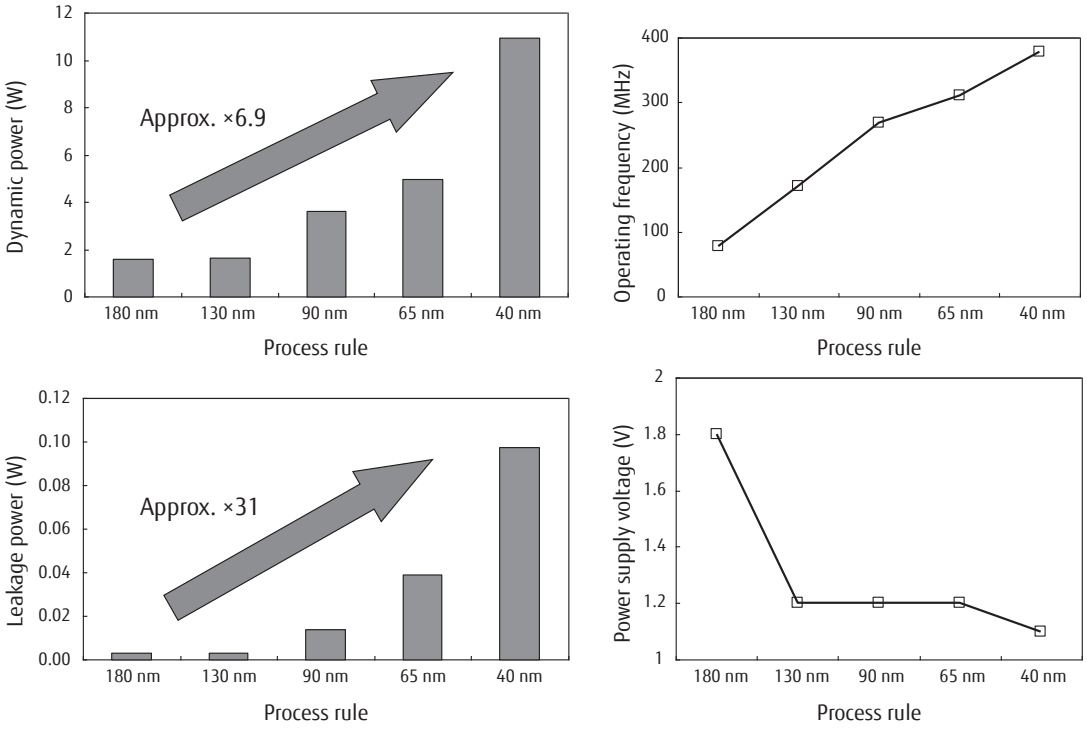


Figure 2
Trends in power consumption of system LSIs.

these are main subjects of the following sections.

3. Technology for reduction of dynamic power

To reduce the dynamic power of image-processing LSIs, we have applied techniques to reduce power consumption such as circuit optimization, which reduces power resulting from unnecessary circuit operation, and incorporating a design that can handle multiple supply voltages.

For circuit optimization, results of the power estimation CAD mentioned earlier are used to identify portions that consume a large amount of power as compared with the target power specification and replace them with algorithms or circuit systems that offer more power efficiency. In addition, circuits are modified for fine-tuned stop control by detecting failure to stop circuit operation.

With the technique of incorporating a design that can handle multiple supply voltages, circuits of an LSI that need to operate at high speed are operated at high voltage, and low-speed circuits are operated at low voltage. The signal lines that connect circuits with different voltages need to have level-shifter circuits, which convert the signal voltage level, inserted as shown in **Figure 3**.

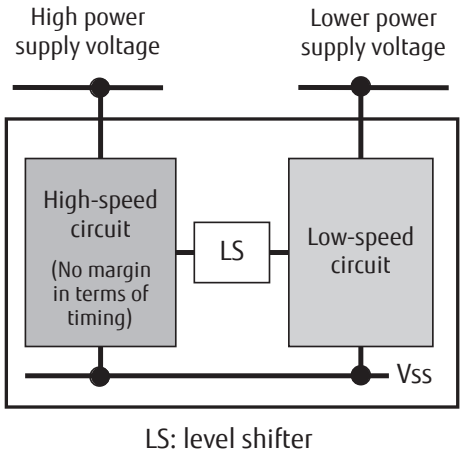


Figure 3
Design for multiple supply voltages.

The following describes examples of a design that can handle multiple supply voltages in an image-processing LSI. Circuits that expect external interrupt signals or those in charge of clock operation

need to be constantly in operation, although not at high speed. Accordingly, for battery-driven devices, power consumption must be reduced to a very low level. For these circuits, which do not use SRAM, the power supply voltage can be lowered to nearly half that of ordinary circuits, and this allows the dynamic power to be reduced. In order to reduce the leakage power as well, low-leakage transistors with a long gate length are used to achieve low power consumption in combination.

4. Technology for reduction of leakage power

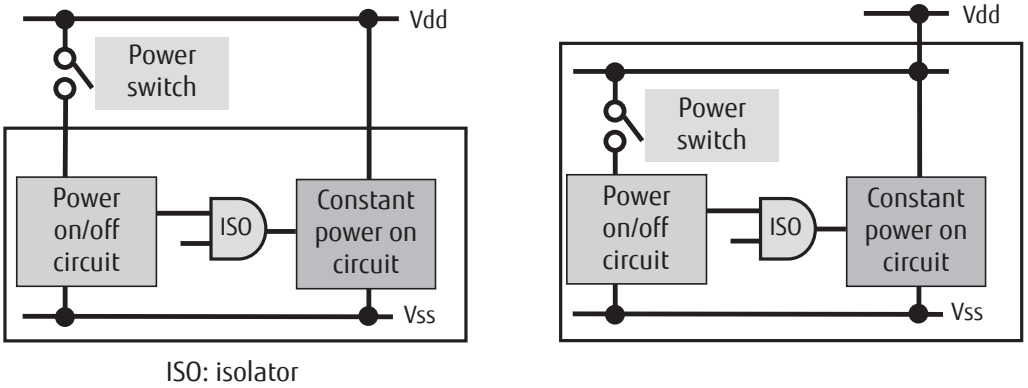
As technology for reducing the leakage power of image-processing LSIs, we have applied techniques to reduce power consumption such as multiple threshold design and power gating design.

In multiple-threshold design, high-speed transistors with a low threshold but large leakage power are used only for the portion of a circuit that needs to be operated at high speed. And, for most of the remaining portion of the circuit not required to operate at a high speed, low-speed transistors with a high threshold and small leakage power are used. By limiting the use of transistors with large leakage power to a small number, high-speed operation can be achieved while the leakage power of the circuit is kept low.

Figure 4 shows the concept of the power gating design. This power gating design is intended for turning off the power switch transistor inserted serially between the circuit and power line to stop power supply to the power on/off circuit while the circuit is not used. It has an effect of significantly reducing leakage power of the circuit while the power switch is cut off by two to three orders of magnitude as compared with the powered-on state. The state of a signal output from the on/off circuit is indefinite when the power is turned off and input of this signal to the constant power on circuit may lead to faulty operation of the constant power on circuit. To avoid this situation, a circuit called an isolator intended for preventing propagation of indefinite signals from the power on/off circuit must be inserted.

The following describes the characteristics required of the power switch. First, an unwanted change in the power supply voltage fed to the circuit resulting from the resistance of the power switch must be suppressed as much as possible. In addition, the circuit must become operable as soon as possible after the power switch is turned on. Another point is that, if the power switch is inadvertently turned on, a large current called an inrush current flows into the power line of the LSI for charging the capacitance of the power on/off circuit. This may cause an unwanted change in the power supply voltage of the LSI and adversely affect operation of the constant power on and other circuits, which must be avoided.

The configuration shown in **Figure 5 (a)** was used for the conventional power switches. To avoid the problem of inrush currents, the voltage of *signal g* for controlling the power switch transistor of a size and capacity large enough to supply the operation current of the circuit was slowly changed for preventing a large

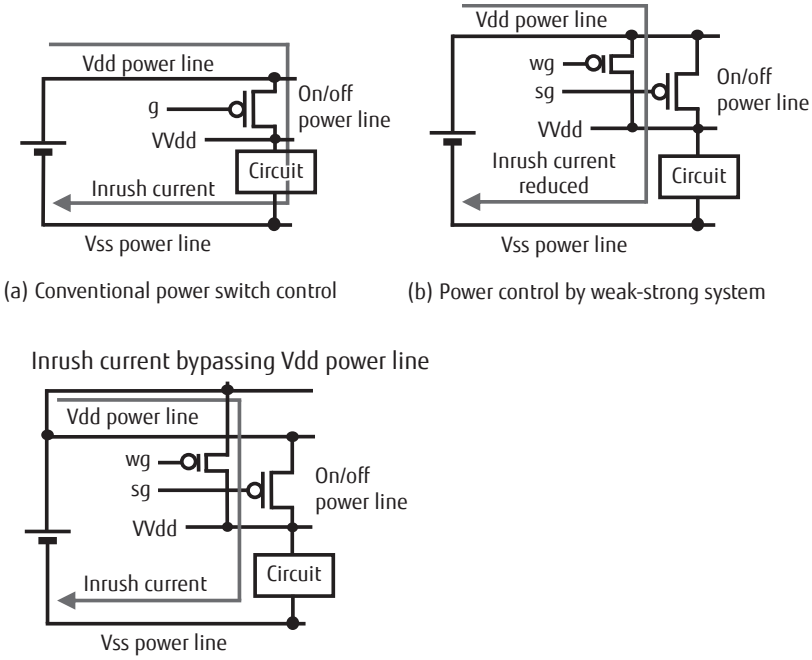


ISO: isolator

(a) Example with power switch provided outside of LSI

(b) Example with power switch provided inside of LSI

Figure 4
Concept of power gating design.



(a) Conventional power switch control

(b) Power control by weak-strong system

(c) System with inrush current bypassing Vdd power line added

Figure 5
System for power switch control.

current from flowing into the power switch, thereby suppressing unwanted changes in the power supply voltage that were generated in the Vdd power line. In this case, the circuit operation cannot start until the voltage of *signal g* has completely finished transition. As a solution to the challenge of reducing the time before the circuit becomes ready for use while avoiding an adverse effect on other circuits caused by inrush currents, configurations as shown in **Figure 5 (b)** and **Figure 5 (c)** can be used. In Figure 5 (b), a power switch of a small size capable of charging the circuit capacitance (weak switch controlled by *signal wg*) is turned on first. The weak switch is adjusted to a size just enough for charging the on/off power line of the circuit. After the potential of the on/off power line has been sufficiently increased by the weak switch, a power switch capable of feeding the operation current of the circuit (strong switch controlled by *signal sg*) is controlled. This allows mutually independent optimization of the characteristics of the current to charge the power line of the circuit and power supply current to be fed into the circuit during operation. As a result, this suppresses any voltage variation in the power switch and reduces the restoration time to a few microseconds, while avoiding faulty operation caused by an inrush current.

As a method to further reduce an adverse effect due to an inrush current, we have devised a system as shown in Figure 5 (c).[1)] To deal with the inrush current generated when the on/off power line is charged by the weak switch, it is run through the dedicated inrush-current-bypassing Vdd power line rather than into the Vdd power line, which minimizes variation in the power supply voltage generated in the Vdd power line. VVdd is a virtual power rail and it serves as a power line when the power switch is ON.

5. Design and verification technology for multiple power supplies

Of various low-power design technologies for image-processing LSIs, we have described so far those belonging to CoolAdjust with the focus on a design that can handle multiple supply voltages and power gating design. To apply these low-power design technologies, we must divide an LSI into multiple power supply regions and insert a level shifter or isolator for the signal connecting between the regions. In addition, a power gating design requires a power switch to be inserted

between the power supply and circuit.

There have been examples of an LSI design that can handle multiple supply regions in the past. However, this design was carried out without awareness of power supply specification in the register transfer level (RTL) design, logic verification and logic synthesis phases. And, in the placement and routing phase and layout phase, which are final physical implementation phases of an LSI, multiple supply voltages, power gating or other power supply specifications were applied to design. In this way, a power supply specification was not taken into account in the RTL design phase, which caused problems. They include, for example, designing a circuit that uses a signal from a circuit in the powered-off state and, for a circuit after restoration from the powered-off state, designing without assuming the loss of the internal state before power off. In addition, different power supply specifications were provided for different design tools, which led to inconsistent designs and tended to cause problems in design quality.

Fujitsu Semiconductor participated early on in the standardization of Common Power Format (CPF), which is an industry standard format for LSI power supply information description, and introduced it into the LSI design flow. CPF is a language for describing power supply and circuit specifications of low-power LSIs owned and managed by the Low Power Coalition under the Silicon Integration Initiative (Si2), a standardization consortium for LSI design technologies. Once a circuit specification has been described based on CPF in specification design and RTL design, the original CPF can be used as the master to input to design tools in the design phase including logic synthesis, placement and routing, simulation, verification and testing.

As a result, delivery of power supply information, which was traditionally obscure in the respective design phase, can be clarified, allowing for a highly reliable design.

In addition, simulation of the powered-off state of a circuit, which was impossible with the conventional logic simulation, becomes possible and the quality of logic verification of LSIs with multiple power supply regions can be improved.

Fujitsu Semiconductor established an LSI design flow integrating CPF for the first time in the world and has applied it to various LSI products. As of July 2012, it has been applied to more than 50 types of LSI design.

We are elaborating the LSI design flow to also accommodate design using Unified Power Format (UPF), a format of description of power supply information standardized by the Institute of Electrical and Electronic Engineers (IEEE) independently of CPF.

6. Future prospects

As described in the section on power consumption trends, low-voltage operation of SRAM in particular is becoming increasingly difficult along with the progress of process miniaturization. This is because SRAM transistors are the smallest in an LSI and susceptible to process variation, which make them prone to reduced operating margins. To address this issue, new transistor technology capable of reducing transistor variation[2)] and technology for ensuring operating margins of SRAM cells can be adopted to allow operation of SRAM at a low voltage. As a result, it becomes easier to reduce power consumption by having low-voltage operation, and greater effects of the design that can handle multiple supply voltages presented in this paper can be expected. There is also a technology called dynamic voltage frequency scaling (DVFS), in which the operating frequency and power supply voltage are controlled according to the processing capability required in order to achieve power reduction, and another technology called adaptive supply voltage (ASV) for chips with the central value of process variation on the fast side, which reduces power consumption by control for reducing the power supply voltage according to the variation. The effect of these technologies intended for power reduction by means of controlling the power supply voltage can be increased as well.

7. Conclusion

This paper has described recent power consumption trends and presented low-power technologies applied to image-processing LSIs with the focus on a design that can handle multiple supply voltages and power gating design. These power techniques for reducing power consumption require the inside of an LSI to be divided into multiple power supply regions and a level shifter, isolator, power switch, and such like to be implemented. To carry out such design with high reliability, a design technique using CPF has been introduced, and this was also explained in this paper. In the future, approaches to reducing process variation and

ensuring SRAM operating margins to reduce the operating voltage are important. As the size of a transistor on a chip is decreased, it becomes difficult to control its size variation, and size variation causes a variation in the electrical characteristics of the device (or MOSFET or transistor). But a very effective way to reduce power supply consumption is to reduce the operating voltage, and it is strongly desired. In the future, it will be important to take approaches to reducing size variation and ensuring SRAM operating margins to reduce the operating voltage.

References

1) K. Kawasaki et al.: A Sub-μs Wake-up Time Power Gating Technique with Bypass Power Line for Rush Current Support. Proceedings of 2008 IEEE Symposium on VLSI Circuits, pp. 146–147.
2) K. Fujita et al.: Advanced Channel Engineering Achieving Aggressive Reduction of VT Variation for Ultra-Low-Power Applications. IEDM Technical Digests, 2011, 32.3.1–32.3.4.

Yoshimi Asada
Fujitsu Semiconductor Ltd.
Mr. Asada is currently engaged in development of low-power technology.