LSI Design Flow Development for Advanced Technology

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LSIs that adopt advanced technologies, as represented by imaging LSIs, now contain 30 million or more logic gates and the scale is beginning to approach the level of 100 million gates. As compared with the 90 nm process generation, this is three to ten times the number of gates. With advanced technologies such as 40 nm and 28 nm, the process characteristics become remarkably complex and wiring resistance rapidly increases, which unavoidably means that more sign-off corners and more accurate sign-off and layout tools are required. In addition, mask design rules, which are process requirements, are constantly increasing in complexity and the 28 nm process requires twice as many mask design rules as the 90 nm one. To address these changing needs in the areas of design and technology, Fujitsu Semiconductor is developing new features for the LSI design environment called Reference Design Flow for introduction into LSI design. This has reduced the turnaround time (TAT) of LSI development adopting advanced technologies. This paper describes the characteristics and effects of Reference Design Flow newly enhanced for advanced technologies.

1. Introduction

Imaging LSIs are increasingly designed into system-on-a-chip systems and the increasing scale of LSIs and accompanying shift to advanced technologies have become remarkable. Meanwhile, time-to-market of LSIs is in a trend toward further reduction so as to beat the global competition. In order to satisfy conflicting requirements of "scale increase of LSIs" and "reduction of LSI design periods" at the same time, Fujitsu Semiconductor has developed an LSI design environment called Reference Design Flow[1)] and applied it to the design of microcontrollers, application-specific integrated circuits (ASICs), and application-specific standard products (ASSPs).

Of the various parts of the Reference Design Flow, this paper puts special focus on layout design and describes issues including measures for handling LSIs, measures for addressing increase of sign-off corners, improvement of layout tool accuracy, and measures for accommodating new mask design rules. These are essential for developing the LSI design environment for advanced processes such as 40 nm and 28 nm. This paper also presents solutions to those issues and their effects.

2. Measures for handling LSIs

LSIs that adopt advanced technologies now contain 30 million or more logic gates and the scale is beginning to approach the level of 100 million gates. This means that, as compared with the 90 nm process generation, the number of gates has increased by three to ten times. The International Technology Roadmap for Semiconductors (ITRS) has shown a roadmap indicating that the trend toward LSIs is expected to continue in the future[2)] as shown in **Figure 1**. For that reason, measures for handling LSIs are the highest priority issue in developing the LSI design environment.

There are several techniques for designing LSIs in a short turnaround time (TAT), and a representative one is hierarchical design. Application of hierarchical design allows the scale of the circuit as the layout design object to be arbitrarily controlled and layout design can be completed within a TAT that meets the schedule and with the memory included in the computer used.

However, there are some layout processes to which hierarchical design cannot be applied. Design planning is one such process. **Figure 2** shows an outline of the processing flow of design planning. Design

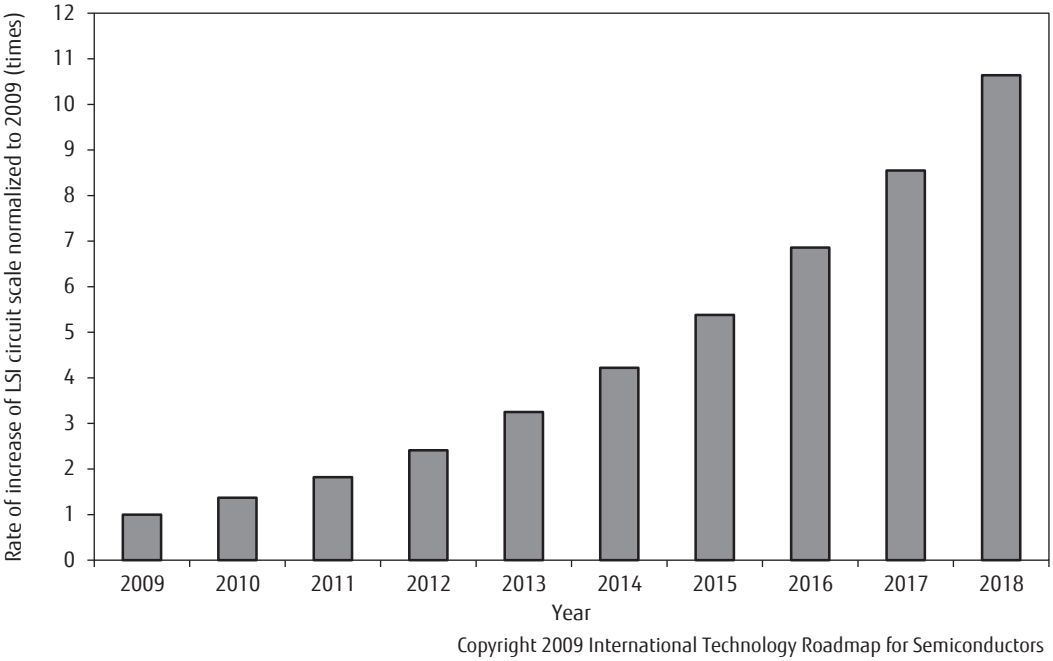

Figure 1
Trend of increasing LSI scale.

planning is a process carried out in the first half of layout design and includes the following steps.

- IO placement
- Hierarchical block placement
- Macro placement and cell placement
- Power routing
- Hierarchical block pin placement
- Signal routing
- Timing optimization
- Hierarchical partitioning

As shown in the figure, hierarchical partitioning is performed in the last step of design planning, which means that design planning itself must be processed by flat design. For that reason, completing design planning in a short TAT while maintaining accuracy is an issue in the development of the LSI design environment.

Reference Design Flow resolves this issue by introducing three new features, which are described below.

1) Introduction of netlist reduction feature

As the first measure, the netlist reduction feature has been introduced. The following outlines the feature.

- The layout tool itself deletes unnecessary circuit information from the memory according to the content of the process of design planning
- The relevant design planning is carried out
- After the process is completed, the deleted circuit information is automatically restored so that the next design planning step can be started

This feature reduces the scale of the circuit handled by the layout tool itself, thus allowing the processing time and amount of memory used to be reduced.

2) Introduction of automatic macro placement feature

With LSIs, the number of macros including memory has reached a few thousand, crossing the limit of what is possible with manual macro placement. To address this issue, an automatic macro placement feature has been introduced as the second measure. With this feature, results very close to manual macro placement with minimum dead space can be generated in short periods of time. As an example, a macro placement that took two days when done manually has been completed in six hours.

3) Introduction of high-speed processing engine for cell placement, signal routing and timing optimization

In design planning, a lot of time is spent for LSI feasibility verification including:

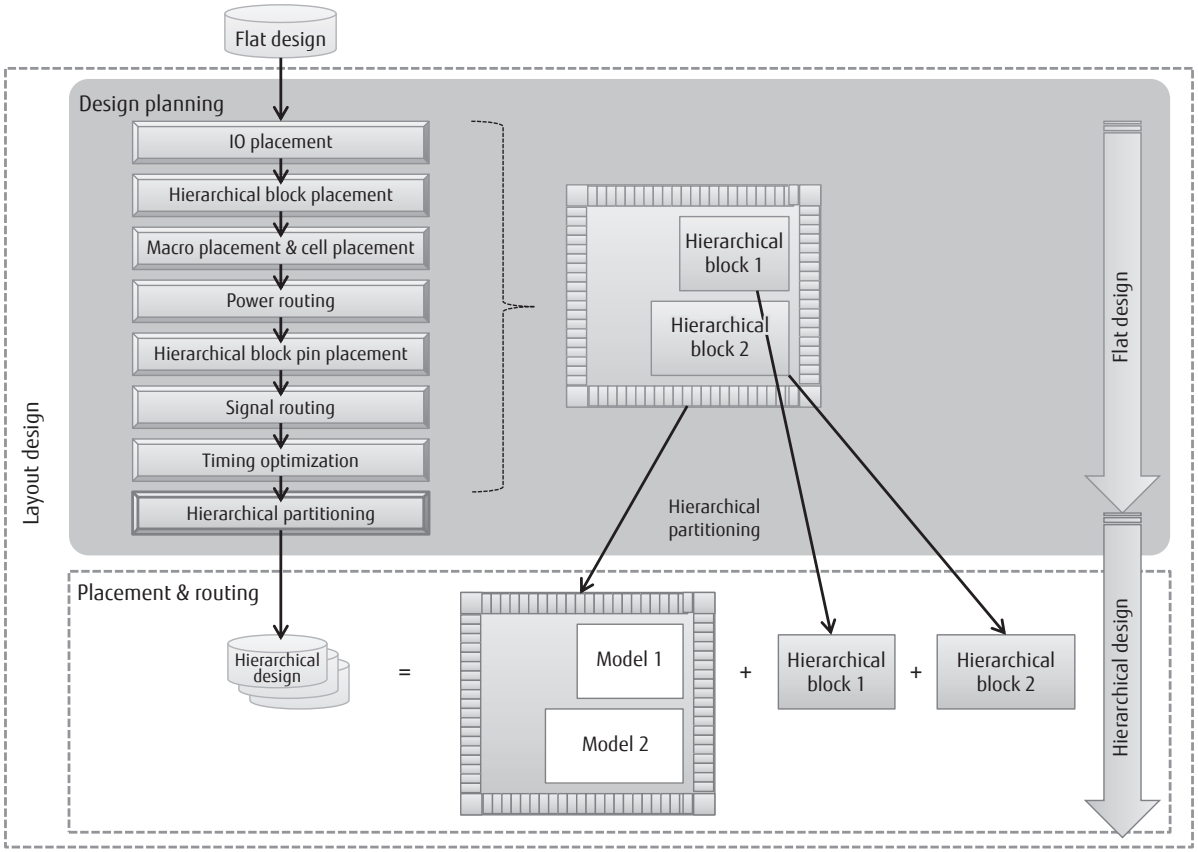

Figure 2
Outline of processing flow of design planning.

- Routability closure at the target chip size and routing layer
- Timing closure under the target sign-off condition

In this verification process, the steps of cell placement, signal routing, and timing optimization are repeated. For that reason, as the third measure, a new high-speed processing engine has been introduced for these three steps, thereby reducing the LSI feasibility verification test time.

By applying design planning including the features described above, design planning of LSIs integrating 110 million logic gates and 10 000 macros can be processed in 48 hours with 77 GB of memory.

In designing LSIs, TAT reduction by ensuring support for multi-CPU processing is also very effective. Reference Design Flow provides positive support for multi-CPU processing. Concerning layout design, almost all processes support multi-CPU processing and multi-CPU processing under a job scheduler such as Load Sharing Facility (LSF) is also supported.

Figure 3 shows the TAT reduction effects by using multi-CPU processing. It shows results of a layout with one CPU and four CPUs of a block on a scale of four million gates as the layout object. While the reduction effects vary depending on the process step, TAT reductions of 18.8% to 67.4% can be achieved.

3. Measures for addressing increase of sign-off corners

An LSI sign-off condition is composed of a combination of operation guaranteed ranges of "process," "temperature" and "voltage." A sign-off corner refers to an arbitrary corner point of the combination. For example, a sign-off condition of process slow, high temperature and lower limit voltage is defined as the worst corner and a sign-off condition of process fast, low temperature and upper limit voltage as the best corner.

With advanced technologies, process characteristics have increased in complexity and a characteristic

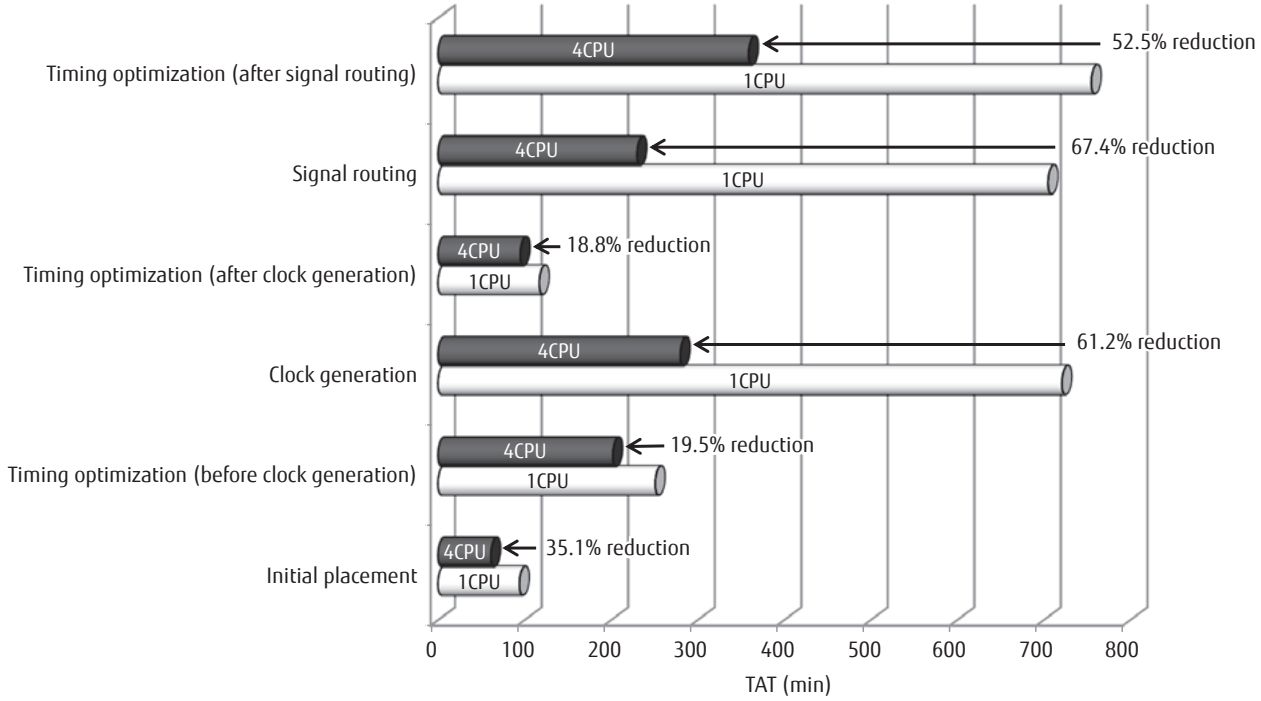

Figure 3
TAT reduction effects of multi-CPU processing.

may emerge in which the worst delay is generated in a low temperature condition—something that was unthinkable with the conventional processes. Similarly, a characteristic exists in which leakage power is inverted depending on the combination of V_{th} (transistor threshold voltage) and temperature.

To cover all of these advanced process characteristics, the number of sign-off corners unavoidably increases in advanced technologies as compared with the conventional technologies. Naturally, increased sign-off corners means there are more corners to be processed with a layout. To focus on optimizing setup timing, multiple corners must be considered. In addition, the power worst corner separate from the corner for setup timing optimization must be considered as well for leakage power optimization. Dealing with multiple corners, which may differ depending on the layout purpose, with high accuracy and a short TAT is an issue in the development of the LSI design environment.

Reference Design Flow resolves this issue by introducing two new features, which are described below.

1) Introduction of Multi-Corner Multi-Mode (MCMM) feature

As the first measure, the MCMM feature has now been introduced to layout design in addition to timing ECO design[1)], which has been previously supported. The following outlines the MCMM feature.

- Multiple corners (multiple modes can be specified as required) are specified for the layout tool
- Layout design is implemented while giving consideration to multiple corners specified at the same time

Traditionally, there was no way to handle this other than serially processing as many setup timing optimization steps as the number of corners, which had a risk of causing a local solution. By introducing this new feature, multiple corners can be collectively processed and the process can be completed with a short TAT without rework.

Furthermore, there was a limit of only one corner considered for clock generation. For this reason, a clock skew occurred at an unconsidered corner and hindered convergence of layout design in some cases. After introducing this feature, it has become possible to give consideration to multiple corners at the same time and the problem of clock skew at an unconsidered corner has been eliminated.

Introducing this feature has also allowed

simultaneous consideration of multiple corners required for setup timing calculation and leakage power calculation. This has significantly improved the accuracy of leakage power optimization, and thus helped disseminate this optimization method.

The benefits of introducing the MCMM feature are as described above, but there are also drawbacks. Generally, the TAT increases in proportion to the number of corners considered by the layout tool and measures to address this issue are also required in the development of the LSI design environment.

2) Introduction of auto scenario[note1)] reduction feature

As the second measure, the auto scenario reduction feature has been introduced. An outline is as follows.

- The layout tool itself calculates the timing of the specified scenario immediately before the start of layout design
- Unnecessary scenarios are automatically deleted from the memory according to the content of the process such as setup optimization, clock generation and leakage power optimization
- The processing time is reduced by keeping on the memory only the scenarios necessary for the relevant process
- After the process is completed, the deleted scenarios are automatically restored and the next layout step is started.

By introducing this feature, layout design can be completed within a TAT that meets the schedule even if multiple corners required by advanced technologies are specified for the layout tool.

Figure 4 shows the TAT reduction effects of the auto scenario reduction feature. It shows the results of a layout of a block on a scale of four million gates as the layout object before and after this feature has been introduced. While the reduction effects vary depending on the process step, TAT reductions of 21.4% to 28.3% can be achieved.

4. Improvement of layout tool accuracy

Along with the advancement of technologies, the impact of the following factors on delay analysis, which were conventionally negligible, has increased and new verification technologies and sign-off conditions are now required.

1) Increase of crosstalk delay
2) Increase of on-chip variation
3) Increase of variation of wiring resistance and wiring capacitance due to wiring density
4) Increase of wiring resistivity

note1) A combination of an arbitrary corner and arbitrary mode is called a scenario. A mode corresponds to the timing constraints describing the operation of an LSI.

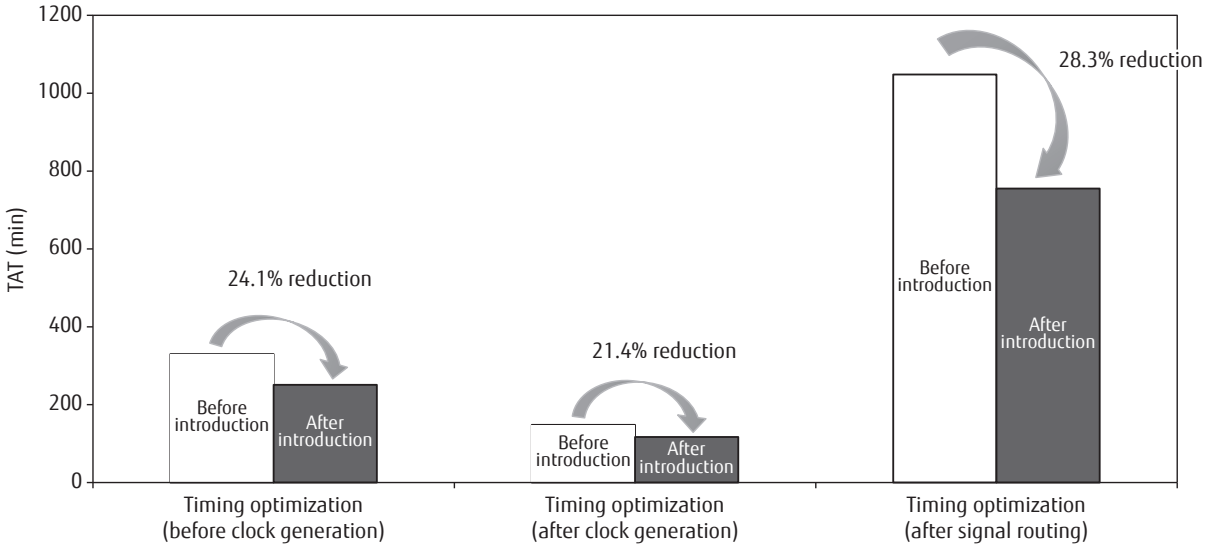

Figure 4
TAT reduction effects of auto scenario reduction feature.

For Reference Design Flow, we have quickly launched verification technologies and put the sign-off conditions in place.

Measures for the sign-off tool have been taken. For the layout tool, however, one problem was that there was no other choice but to address the error factors in delay analysis mentioned above by taking measures in the form of design margins for reasons including:

- Inadequate functionality of the layout tool
- Inability to be used in practical applications in terms of TAT even if adequate functionality is provided

Nevertheless, with advanced technologies such as 40 nm and 28 nm, the increased design complexity and process variation made convergence of calculation in layout design impossible with design margin, and there was an urgent need to improve the accuracy of the layout tool.

Accordingly, for Reference Design Flow, we have launched new features, accelerated enhancement and positively introduced a new version of the layout tool so as to accommodate advanced technologies, and thereby improved the accuracy of the layout tool. Specifically, the following new features and libraries have been introduced into the layout design environment.

1) Introduction of a delay calculation engine that takes crosstalk into consideration
2) Introduction of an on-chip variation (OCV) calculation engine
3) Introduction of an engine for wiring resistance and wiring capacitance extraction that takes wiring density into consideration
4) Introduction of Composite Current Source (CCS) libraries[note2)]

Introducing the new features and libraries mentioned above has improved the accuracy of layout tools and improved the correlation between the sign-off and layout tools. Further, the design margins, which were expected in the conventional LSI design environment, have been significantly reduced.

Figure 5 shows delay calculation errors between sign-off and layout tools in 28 nm technology. In 28 nm technology, in which correlation is difficult, delay calculation errors are within the range of ±10 ps with most of the timing paths. This points to the high accuracy of the layout tool that almost eliminates the need for design margins.

5. Measures for accommodating new mask design rules

Due to the miniaturization of processes, measures for new mask design rules, which did not exist in the conventional technologies, are essential to advanced technologies. For example, the 28 nm process requires twice as many mask design rules as the 90 nm one.

Meanwhile, when advanced technologies are launched, specifications of technology files[note3)] and features of layout tools are often unable to meet the requirements of new mask design rules. The LSI design environment must be developed so that the LSI design schedule can be met even in such a situation.

With Reference Design Flow, we have resolved this issue by independently developing routing technology files tuned to satisfy new mask design rules within the scope of the existing technology file specifications and layout tool features. In the 40 nm and 28 nm process generations, there are new mask design rules relating to routing as well as placement but we have successfully satisfied the new rules by making use of workarounds.

Even for a fabless company, techniques for tuning the LSI design environment including technology files are essential as differentiating techniques.

6. Conclusion

This paper has described issues such as measures for handling LSIs, measures for addressing increase of sign-off corners, improvement of layout tool accuracy, and measures for accommodating new mask design rules. These are essential to the development of the LSI design environment for advanced technologies. To resolve these issues, we have developed and introduced

note2) Non-linear delay model (NLDM) libraries were common in the past but they have a limitation in that they cannot handle the impact of wiring resistance with high accuracy. For that reason, CCS libraries, which are current source model-based, are the mainstream for advanced technologies.

note3) A technology file is a file representing mask design rules for each layout or sign-off tool. Multiple technology files exist such as those for placement and routing and for wiring resistance and wiring capacitance extraction.

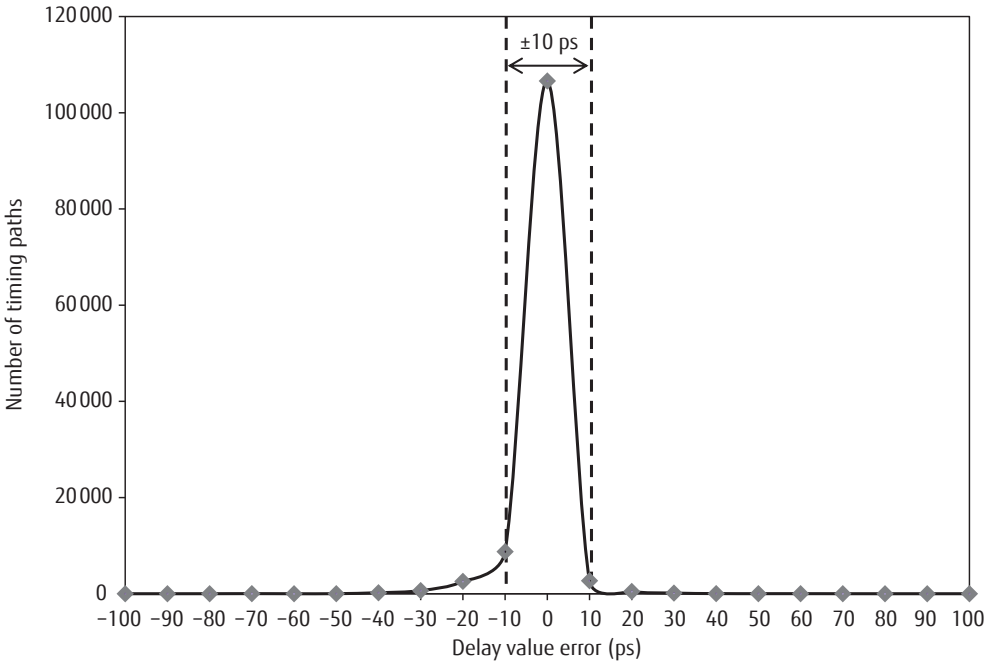

Figure 5
Delay calculation errors between sign-off and layout tools.

new features including the netlist reduction feature, automatic macro placement feature, high-speed processing engine for cell placement, signal routing and timing optimization, MCMM feature, auto scenario reduction feature, delay calculation engine that takes crosstalk into consideration, OCV calculation engine, an engine for wiring resistance and wiring capacitance extraction that takes wiring density into consideration, CCS libraries, and independent development of routing technology files. We have thereby managed to reduce TAT of LSI development adopting advanced technologies such as 40 nm and 28 nm processes.

For this LSI design environment, we also plan to conduct development in future so as to accommodate the 20 nm process.

References

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