

# H.264 Transcoder LSI Chip

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Extension of video recording times and further reduction in network traffic loads require that video data compressed with the MPEG-2 format used for digital terrestrial broadcasting and other types of broadcasting be converted to the H.264 format, which has a higher data compression rate. It is also desirable that H.264 video data itself be converted to an even lower bit rate. This paper introduces a transcoder implemented on an LSI chip for executing in real time the transcoding processing required for these applications. The transcoding method used is advantageous in terms of image quality. It first decompresses compressed video data and then recompresses it so as to minimize the image deterioration that normally accompanies cross-format conversion. This LSI has low power consumption and a small form factor, enabling it to operate with USB power (under 2.5 W) and be mounted in devices the size of a PCI Express Mini Card (30 × 50.95 mm). It is now being used mainly in PC-TVs and personal video recorders (PVRs) to achieve long recording times of digital-terrestrial, BS digital, and CS digital broadcast programs in Japan. However, with the recent proliferation of mobile terminals like smartphones and tablets and the increasing demand for video viewing and recording via the network, Fujitsu expects this transcoder to also be used for converting video to a compression format that can reduce network traffic loads and enable the playback of HD video on today's mobile terminals. Fujitsu Semiconductor is committed to creating new solutions to support these applications.

## 1. Introduction

Functions for making long-time video recordings in the H.264 format using a transcoder<sup>note1)</sup> are now becoming standard in hard disk recorders and television sets equipped with a recording function, and many types of devices are being equipped with transcoders implemented on LSI chips (hereafter "LSIs".) At the same time, there are increasing opportunities for viewing high-definition (HD) content with mobile devices such as smartphones and tablets, and the use of transcoding functions is spreading to enable data-intensive HD content to be highly compressed and transmitted on wireless transmission paths having narrow bandwidths.

In May 2007, Fujitsu announced the MB86H51

codec LSI for compressing and decompressing Full HD video in the H.264 format in real time.<sup>1)</sup> Then, using the video processing technology of this LSI as a foundation, it developed the MB86H52 first-generation transcoder LSI, which was announced in August 2007.<sup>2)</sup> This product was followed in May 2009 by the MB86H57 and MB86H58 second-generation transcoder LSIs providing enhanced functionality, a smaller form factor, and reduced power consumption.<sup>3)</sup>

Fujitsu Semiconductor has now developed the third-generation of these transcoder LSIs—the MB86M01, MB86M02, and MB86M03—referred to collectively as the MB86M0x. This LSI adds new functions to the MB86H57 and MB86H58, which have come to be widely used in stationary equipment such as hard disk recorders and in mobile accessories for notebook computers.

This paper first describes issues with current

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note1) A device for recompressing (transcoding) compressed data in MPEG-2 or another format into a format having a higher compression rate such as H.264.

transcoder products and provides an overview of the MB86M0x. It then presents examples of system configurations using this LSI and describes future development plans.

## 2. Issues with current products

The MB86H57 and MB86H58 second-generation transcoder LSI, while coming to be used in a variety of products as described above, are limited by the following issues that need to be resolved to expand the application of Fujitsu's transcoder LSIs.

- 1) Support of broadcast standards in other countries  
Support is provided only for MPEG-2-to-H.264 transcoding, which means that these chips cannot be used in products for coding digital broadcasts in the H.264 format.
- 2) Support of improved display resolution in mobile terminals  
In simultaneous transcoding (in which two streams of data from Full HD input data are generated, one at Full HD resolution and the other at less than Full HD), support for the stream at less than Full HD is limited to QVGA display resolution. These chips cannot, as a result, provide sufficient resolution for today's advanced mobile terminals like smartphones.
- 3) Support of dual transcoding under USB operation  
When a USB is used as the interface between the transcoder product and host system, no support is provided for a master/slave connection function, in which two transcoders interconnected by a special interface act as master/slave transcoders with the former controlling the latter, and in which both transcoders appear as one transcoder to the host CPU. These LSIs cannot, as a result, be used for dual transcoding.
- 4) Enhanced image quality  
Although these LSIs are highly praised by customers for their high image quality, further improvements must be made to maintain industry-leading image quality in the years to come.
- 5) Double tuner support  
Since support for only one tuner input is currently provided, one LSI by itself cannot support the two tuners that are needed if background program recording is desired.
- 6) Use of certified USB logo  
Since power consumption during USB suspend mode does not satisfy the standard, USB logo

certification cannot be obtained for USB bus-powered operation.

## 3. MB86M0x overview

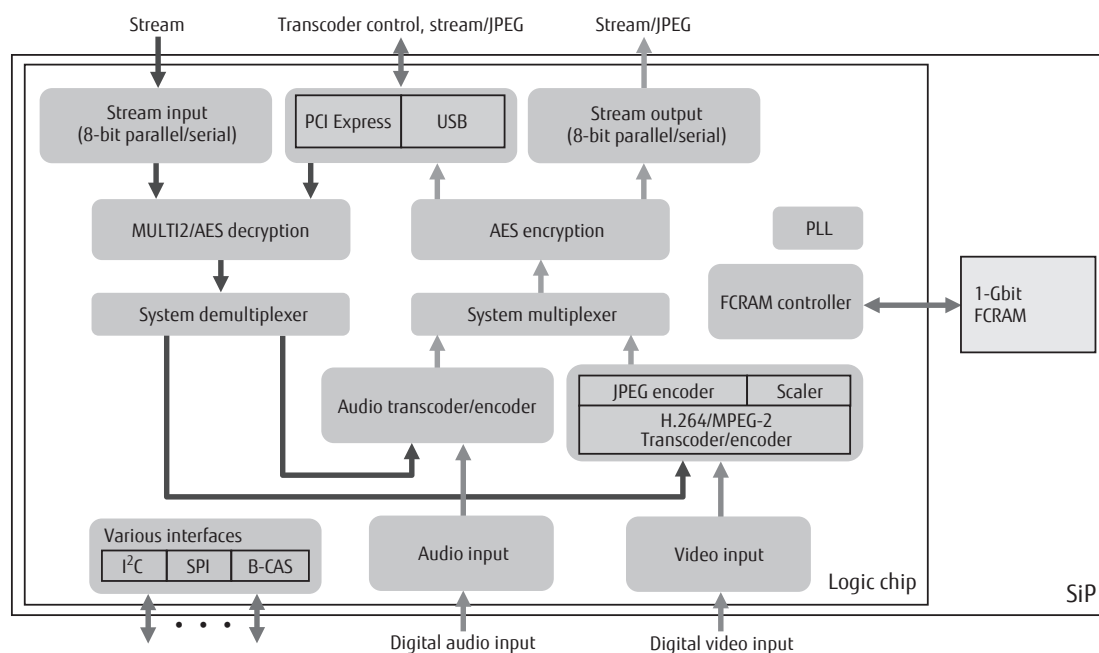
The MB86M0x was developed as a product to resolve the issues described in the previous section. A block diagram of this LSI is shown in **Figure 1**. The H.264/MPEG-2 transcoder/encoder block for converting video data is based on the encoder/decoder cores that have been successfully used in past codec/transcoder LSIs. In addition to low power consumption, it achieves high image quality and a reduction in processing load through proprietary algorithms developed by Fujitsu Laboratories. This block provides not only a transcoding function that converts Full HD data from MPEG-2 into H.264 format but also a transrating function that converts H.264 video data into H.264 formats with an even higher compression rate.

The audio transcoder/encoder block performs audio transcode/encode processing for a variety of formats while the system multiplexer block multiplexes video and audio data in a TS/MP4 container. The system demultiplexer block, meanwhile, separates video and audio data from the TS/MP4 container.

In addition to the above functional blocks, the MB86M0x comes equipped with a JPEG encoder for generating thumbnail images, a scaler for enlarging/reducing images, an AES encryption block and MULTI2/AES decryption block for providing security functions, and a fast cycle random access memory (FCRAM) controller for accessing a 1-Gbit FCRAM (Fujitsu Semiconductor's proprietary low-power memory technology).

The MB86M0x integrates the above functions with a video input section for inputting uncompressed digital video data in SMPTE 274M/296M-2001 and ITU-R BT.656 formats, an audio input section for inputting digital audio data in I<sup>2</sup>S format, a stream input section for inputting stream data, a stream output section for outputting stream data, a PCI Express/USB block for exchanging commands, stream data, and JPEG data with an external CPU host, a variety of interfaces including I<sup>2</sup>C, SPI, and B-CAS, and a phase locked loop (PLL) for generating the internal operating clock. This LSI with all of the above functions is packaged together with the 1-Gbit FCRAM.

The MB86M0x achieves industry-leading low



**Figure 1**  
Block diagram of MB86M0x LSI.

power consumption of 1.2 W (including memory) during Full HD H.264 transrating operation. Its lineup of packages consists of a 13-mm-square package targeting accessories for smartphones and tablets and mobile accessories for notebook computers and a 21-mm-square package with a ball pitch of 0.8 mm targeting home electronics equipment.

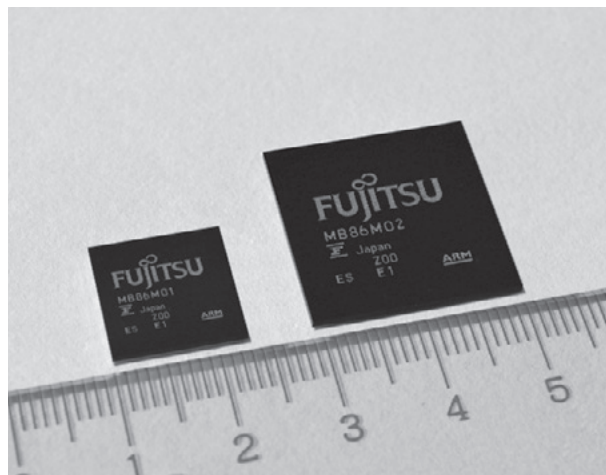
A photograph of two MB86M0x LSIs is shown in **Figure 2**, and the MB86M0x main specifications are listed in **Table 1**.

#### 4. Main features

The MB86M0x LSI has the following features, which can be used in a variety of applications.

- 1) Support of H.264 transrating and diverse audio transcoding

Fujitsu's past codec/transcoder LSIs supported products only for Japan and the United States, which lie in the MPEG-2 broadcast sphere. The addition of the H.264 transrating function to the MB86M0x means that it can now be used in products for Europe, South America, and Asia in the H.264 broadcast sphere as well as in equipment supporting "SKY PerfectTV! HD" H.264 broadcasts within Japan. This transrating function enables data to be recompressed even for H.264



**Figure 2**  
Photograph of MB86M0x.

broadcasts so that video recording time can be further extended. The MB86M0x also supports audio transcoding for a variety of formats (including MPEG-2/4 AAC-LC, HE-AAC, Dolby™ Digital (AC-3)<sup>note2)</sup>, and MPEG-1 Audio Layer 2) so that audio can be converted to fit the specifications of diverse playback devices.

note2) Dolby is a trademark of Dolby Laboratories.

**Table 1**  
Main specifications of MB86M0x LSI.

Function	Specifications	
Transcode	Video	MPEG-2HD → H.264HD/SD + H.264SD/QVGA H.264HD → H.264HD/SD + H.264SD/QVGA MPEG-2HD → MPEG-2SD H.264HD → MPEG-2SD *Transcode speed: 1.n – 2.0 x
	Audio	MPEG-2/4 AAC-LC, HE-AAC, MPEG-1 Audio Layer2, Dolby™ Digital (AC-3) Re-mux
	Data remux	ARIB Data, Closed Caption, Teletext
Encode	Video	H.264 HD/SD/QVGA, MPEG-2 SD
	Audio	MPEG-2/4 AAC-LC, HE-AAC, MPEG-1 Audio Layer2, Dolby™ Digital (AC-3)
Stream formats	MPEG-2 TS, MP4	
Interfaces	PCI Express, USB2.0 (Device), Stream-I/F (Serial or 8-bit Parallel) [2 input, 3 output streams], Video I/F (SMPTE 274M/SMPTE296M-2001, ITU-R BT.656), Audio I/F (I <sup>2</sup> S)	
Other functions	Security: AES (encryption/decryption), MULTI-2 (decryption only)	
	JPEG QVGA encoder (for thumbnails)	
	I <sup>2</sup> C, SPI-ROM (EEPROM) I/F, B-CAS I/F	
Power consumption	1.1 W (typ., MPEG-2 HD to H.264 HD transcoding) 1.2 W (typ., H.264 HD to H.264 HD transrating)	
Memory	1-Gbit FCRAM in-package	
Packages (SiP)	MB86M01: FBGA 490-pin 13-mm square (ball pitch: 0.5 mm) MB86M02: FBGA 490-pin 21-mm square (ball pitch: 0.8 mm) MB86M03: FBGA 289-pin 13-mm square (ball pitch: 0.65 mm) <sup>note)</sup>	

note) No PCI Express interface

## 2) Enhanced image quality

Support is now provided for reference B pictures, thereby increasing the compression rate and improving image quality at low bit rates.

## 3) Simultaneous control of two programs for viewing and recording

The MB86M0x chip features two tuner input terminals, which means that it can connect to two tuner modules and thereby simultaneously control a program for viewing and a program for recording.

## 4) USB dual transcoding function

In past transcoder LSIs, the master/slave transcoder-connection function could be applied only when using PCI Express. Now, with the MB86M0x, it can also be applied when using USB as a host interface. This function enables two MB86M0x to be interconnected and used as a dual transcoder.

## 5) Reduced power consumption in USB suspend mode

The power consumed by the MB86M0x in USB suspend mode has been reduced to meet standard specifications so that USB logo certification, which could not be obtained for past transcoder LSIs, can now be obtained for USB bus-powered operation.

## 6) Improved resolution in simultaneous transcoding

Past transcoder LSI supported only QVGA display resolution in simultaneous transcoding while the MB86M0x also supports standard definition (SD) display resolution.

# 5. Application examples

This section presents examples of configuring practical systems using the MB86M0x.

## 1) USB dongle TV tuner

This is a solution for adding a tuner capable of long-time video recording by simply connecting the dongle, a small USB device, to a device like a PC, a TV, or set-top box (STB) having a USB interface (**Figure 3**).

The dongle is powered by the USB bus, meaning that an AC adapter is not needed, resulting in a very simple system configuration.

## 2) Wi-Fi TV tuner

This is a solution that enables TV viewing on mobile terminals like smartphones and tablets. Since viewing Full HD broadcasts directly on a mobile terminal is problematic because of insufficient decoding performance and network bandwidth, a transcoder makes it possible to convert resolution and bit rate so that such broadcasts can be easily viewed (**Figure 4**).

## 3) Simultaneous multi-channel recording

The MB86M0x transcoder's two tuner inputs and master/slave connection function can be used to provide a four-tuner-module simultaneous viewing/recording solution (**Figure 5**). For a system that supports only digital terrestrial broadcasting, this configuration enables the number of B-CAS cards (conditional access cards for Japanese broadcasting) to be reduced from four to one, thereby reducing the bill-of-materials

(BOM) costs associated with these cards.

## 6. Future development plans

Constructing the systems for the Wi-Fi TV tuner and simultaneous multi-channel recording applications described above requires a host CPU for controlling the transcoder, which means a product that is less than optimal in terms of performance and cost. To address this issue, we are developing a companion LSI for existing transcoders. At the same time, the demand for high-resolution video beyond Full HD such as 4K2K ( $4096 \times 2160$  or  $3840 \times 2160$  pixels) is expected to increase. In response to this need, we are moving forward on the development of 4K2K codec technology for use in transcoders and other products. These development plans are summarized below.

### 1) Companion LSI

The current Wi-Fi TV tuner solution includes a host CPU as a multi-decoder and communications processor. To implement such a CPU, we could use a multi-decoder

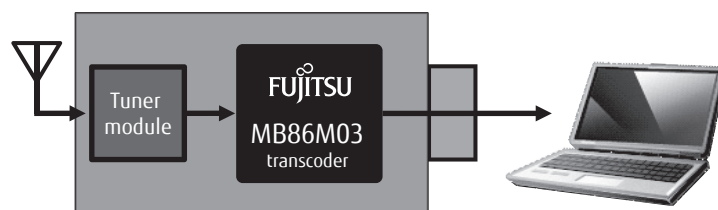


Figure 3  
USB dongle TV tuner.

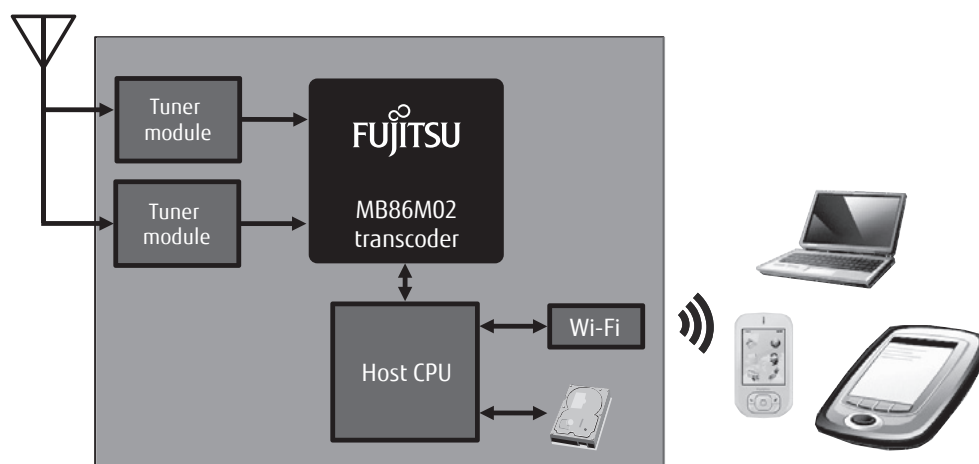
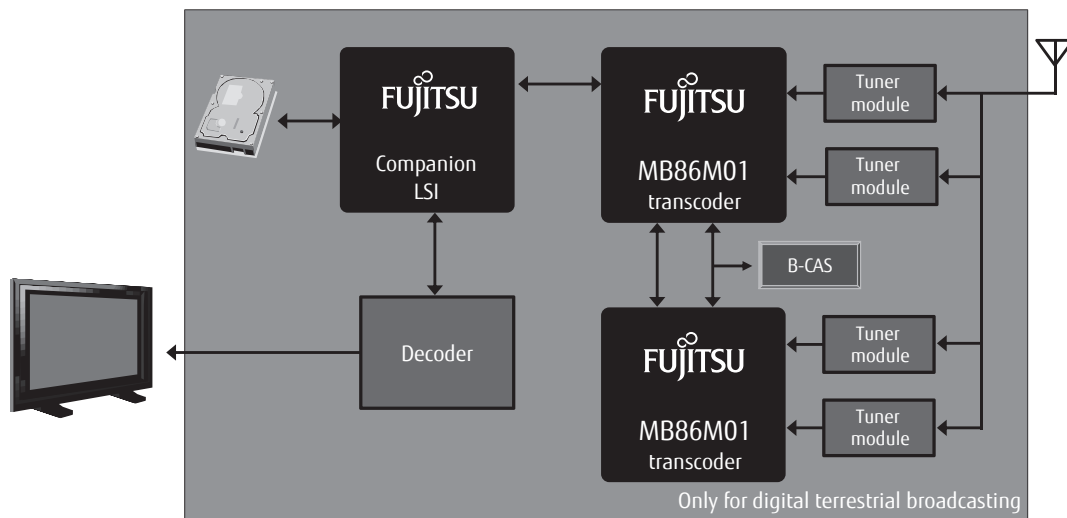


Figure 4  
Wi-Fi TV tuner.



**Figure 5**  
Simultaneous multi-channel recording.

LSI, but it would have no margin performance-wise for adding functions. Conversely, a communications processor has more than enough performance but is impractical from the viewpoint of power consumption and price. The simultaneous multi-channel recording solution, meanwhile, requires the control of multiple transcoders, but the need for connecting simultaneously to a hard disk drive (HDD), the network, etc. would require the use of multiple interfaces. Unfortunately, there is currently no LSI that can satisfy this requirement. We are currently in the process of developing a companion LSI exclusively for transcoders with just enough features to solve the above problems. This LSI will integrate an ARM Cortex™-A9 dual-core processor (operating at 500 MHz or less) and various interfaces (such as USB2.0/3.0, S-ATA, PCI Express, and Gigabit Ethernet MAC) as needed for different solutions. The plan is to optimize performance and functionality for each transcoder-based solution with the aim of reducing power consumption and price.

## 2) 4K2K/HEVC codec development

In many countries including Japan, analog terrestrial broadcasting has been discontinued, and the conversion to Full HD broadcasting has been completed. Moreover, efforts toward the development and deployment of 4K2K video have already begun in various countries. A number of consumer-electronics makers announced 4K2K-compatible TVs at the 2012

International CES show, and Intel's next-generation mainstream CPU (Ivy Bridge) launched in April 2012 supports playback of 4K2K video. In addition, a number of 4K2K camera products have already appeared, enabling the creation of 4K2K content. Since 4K2K video also consists of a huge amount of data, compression using some kind of format is needed, and since this amount of data is essentially four times that of Full HD video, an even higher compression rate is required. To meet this need, standardization of High Efficiency Video Coding (HEVC)—a new format having twice the compression rate of H.264—is underway at the Joint Collaborative Team on Video Coding (JCT-VC) established by the Moving Picture Experts Group (MPEG) of ISO/IEC and the Video Coding Experts Group (VCEG) of ITU-T. The plan is to complete this standardization work by January 2013. Fujitsu Laboratories is participating in these standardization activities and is conducting algorithm studies. Against the above background, the study of 4K2K/HEVC codec-core development at Fujitsu has begun.

## 7. Conclusion

This paper introduced a transcoder LSI for converting video in real time and presented future development plans. The development of Full HD codec LSIs and transcoder LSIs has been progressing steadily, and the MB86M0x LSI introduced here represents the

completion stage for a product using current codec technology. Looking forward, we plan to expand transcoder application by designing new solutions using a chipset consisting of a companion LSI and one or more transcoder LSIs. Additionally, we plan to exploit the codec-related technology that we have accumulated over many years to achieve early development of a 4K2K/HEVC codec with the aim of opening up a whole new world of video processing.



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Mr. Tanaka is engaged in the development of transcoder LSIs.

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