Simulation of Electrical Characteristics Using SignalAdviser Environment

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As the operating frequencies of the printed circuit boards (PCBs), multichip modules (MCMs), and systems in packages (SiPs) used in digital devices have increased while the operating voltage of the large-scale integration (LSI) chips in these devices has decreased, two problems regarding electrical devices have arisen: first, design time has become longer owing to noise problems such as signal integrity (i.e., signal noise), power integrity (power-supply noise), and electromagnetic compatibility (EMC); and second, costs have increased. These problems have been solved by establishing an electrical-characteristics simulation environment in which simulation is used to optimize the design of a broad range of digital devices. In this report, Fujitsu's efforts in establishing such an environment are described, and examples of using the latest environment, called SignalAdviser, for signal-integrity analysis and power-integrity analysis are presented.

1. Introduction

The operating frequencies of the printed circuit boards (PCBs), multichip modules (MCMs), and systems in packages (SiPs) used in digital equipment such as high-performance, high-end servers are steadily increasing. Moreover, to achieve higher performance and better functionality, the degree of integration of the large-scale integration (LSI) chips in these devices has been considerably increased by exploiting cutting-edge process-refinement technology. In step with these trends, the current consumed by the LSIs has increased substantially. To suppress the increase in power consumption resulting from the increased operating frequency and current consumption, the operating voltage of the LSIs has been steadily decreased. Consequently, it has become difficult to eliminate operation-related problems caused by, for example, power-source ground-bounce noise, simultaneous-switching noise, and return current (which are associated with temporal variation of current consumption during LSI operation) and to design equipment so that the electromagnetic interference (EMI) that it generates because of these noise sources satisfies electromagnetic compatibility (EMC) standards.[1),2)] Furthermore, the scaling down of LSI processes as well as the reduction in operating voltage and the increase in packaging density of devices are making it more difficult to ensure that equipment is resistant to electrostatic discharge (ESD). In addition, complex noise problems are becoming more prevalent. They result from the various noise sources described above and are a combination of spatially propagated and transmitted noises. Such complex noise problems, for example, degrade the antenna-reception sensitivity of mobile devices such as cellular phones. They can be grouped into four categories.

1) Signal integrity (signal noise)
- reflection noise/crosstalk noise
- skin effect/dielectric loss

- inter-symbol interference (ISI)

2) Power integrity (power-source noise)
- simultaneous switching noise
- power-source ground-bounce noise
- noise due to return current

3) EMC (EMI noise)
- EMI specifications (VCCI, FCC, EMC directives) are not satisfied.
- ESD level that the equipment can tolerate is too low.

4) Multiple-noise problems

Problems due to a combination of signal noise, power-source noise, and EMI noise (such as degradation of antenna-reception sensitivity)

Aiming to solve these noise problems, the Fujitsu Group has established a simulation-based environment for investigating electrical characteristics and optimizing designs through simulation. Using this design environment for developing a wide range of devices—ranging from the latest high-end servers to mobile phones—and eliminating the design rework necessitated by noise problems has had two significant effects: development times have been shortened, and development and equipment costs have been reduced.

This report describes electrical-characteristics simulation and reviews Fujitsu's efforts at constructing a simulation environment; the latest version is called SignalAdviser. It also presents application examples of signal-integrity analysis and power-integrity analysis. More details are given in the paper "Two Application Examples of Electromagnetic Field Analysis at Fujitsu" in this issue.

2. Construction of environment for simulating electrical characteristics

Before the 1990s, the Fujitsu Group focused on applying "Design Rule Check" (DRC), which incorporates design-rule documents and the rules they contain into the computer-aided design (CAD) systems used for designing PCBs, as a method for devising noise countermeasures. As process-refinement technology evolved, however, the limits on design methods that rely on only these design rules became more obvious.

More specifically, with generalized design rules, prevention of noise problems under the worst imaginable conditions was exceedingly difficult. It was thus often the case that design was difficult when attempts were made to follow the design rules. As a result, cases in which designs did not follow the design rules and cases in which extensive re-design work to solve noise problems was required became more noticeable. To handle such cases, it could be considered sufficient to draw up and apply design rules that combine the design requirements for individual devices; however, that would be unrealistic because it would take a huge amount of work by specialists in noise problems to draw up the design rules. As a result, we basically design products by complying with design rules or by using DRC; however, in difficult cases, the designers themselves perform a high-precision simulation and verify the presence or absence of noise problems. Moreover, a simulation-based design method that obtains optimum design conditions by exploiting simulation only when problems occur is being utilized. Since the beginning of the 1990s, the Fujitsu Group has developed and applied various types of simulators and solvers that make it possible to devise countermeasures against the above-described noise problems by using simulation-based design methods (**Figure 1**). A line noise analysis system called SIGAL[3] was released in 1996. It was superseded by SignalAdviser, the current system, in 2001. SignalAdviser is a family of sub-systems (simulators and solvers), including SignalAdviser-SI (SI: signal integrity), SignalAdviser-PI (PI: power integrity), and SignalAdviser-EMC.

By combining a DRC system with these simulators and solvers as needed, one can establish an environment in which noise

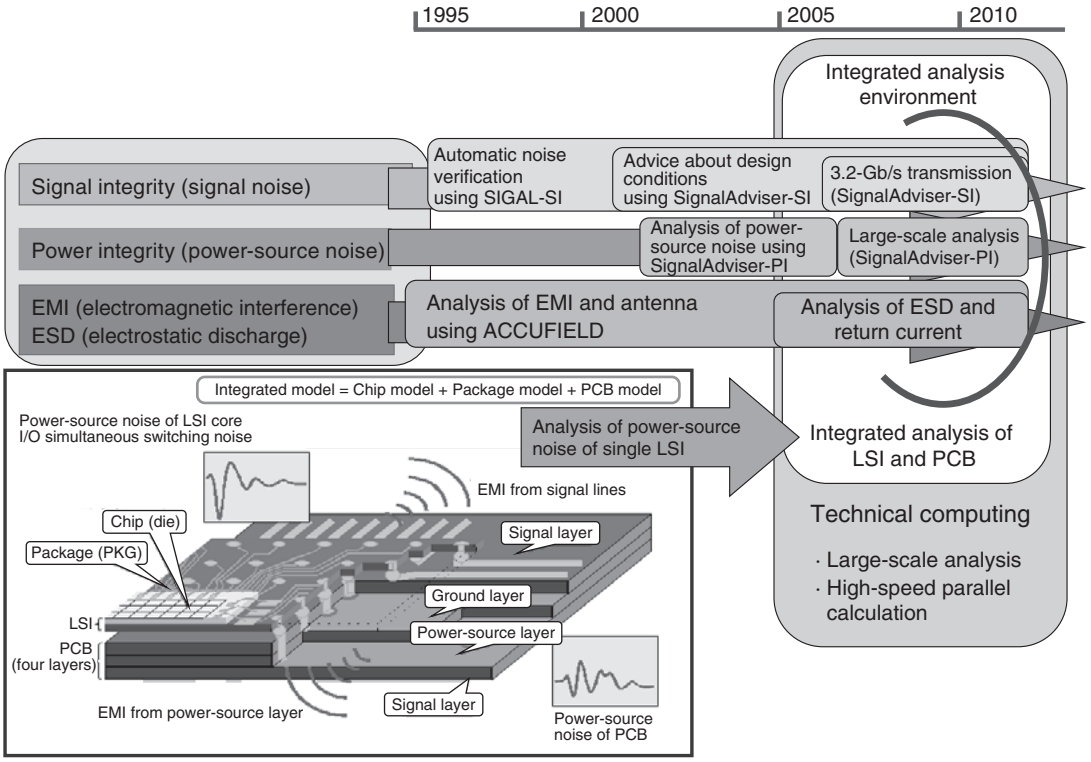
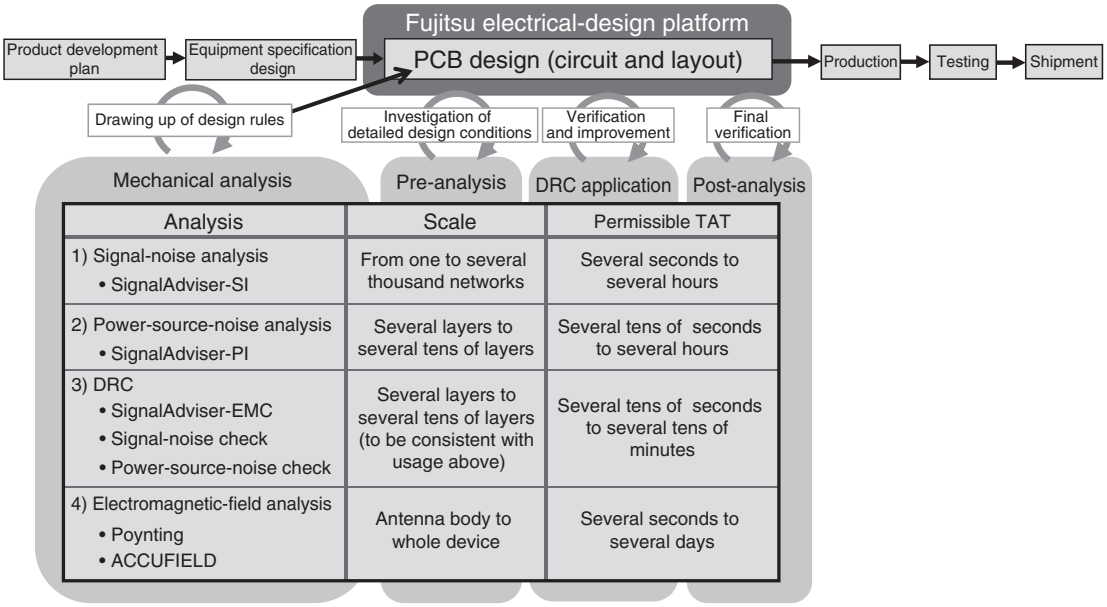


Figure 1
Development of simulation-based design method.

countermeasures can be efficiently devised. To eliminate rework necessitated by noise problems, the simulator and solver must be incorporated into the design process in such a manner that they can be utilized effectively. In other words, they must not only ensure high precision but also produce analysis results in a sufficiently short turnaround time (TAT). The TATs required for analysis by the four simulator/solver functions in SignalAdviser are listed in **Figure 2**. For example, in the case of signal-noise analysis (using SignalAdviser-SI), investigating the transmission line conditions in an upper-stream design stage requires finding optimal solutions for a representative network by trial and error while analysis is continuously repeated. The permissible TAT for analysis in that case is at most a few seconds. However, if the analysis after PCB design is comprehensive, covering up to several thousand circuit networks across all PCBs, the permissible TAT is up to a few hours. Thus, the permissible TAT for analysis varies greatly in accordance with the analysis target and scale.

The electrical-characteristics simulation environment developed by Fujitsu satisfies the permissible TATs for the analyses listed in Figure 2 in all fields (ranging from signal-integrity analysis of PCBs to electromagnetic-field analysis of whole devices). Normally, there is a trade-off between analysis precision and analysis time, and shortening the processing time while maintaining precision requires specialist knowledge and know-how concerning simulation methods and electronic circuits. In contrast, simultaneously performing design and simulation requires an environment that is accurate and can be easily used by not only certain technical experts with specialist knowledge but also general designers.

The SignalAdviser system developed by Fujitsu for creating simulation models has



Analysis	Scale	Permissible TAT
1) Signal-noise analysis • SignalAdviser-SI	From one to several thousand networks	Several seconds to several hours
2) Power-source-noise analysis • SignalAdviser-PI	Several layers to several tens of layers	Several tens of seconds to several hours
3) DRC • SignalAdviser-EMC • Signal-noise check • Power-source-noise check	Several layers to several tens of layers (to be consistent with usage above)	Several tens of seconds to several tens of minutes
4) Electromagnetic-field analysis • Poynting • ACCUFIELD	Antenna body to whole device	Several seconds to several days

Figure 2
Analysis TATs required by simulator.

made it possible to automate and simplify tasks such as selecting a modeling method and setting a partition pitch and to automatically optimize analysis precision and time. On top of providing these features, it can automatically judge whether simulation results are satisfactory or not and present advice concerning noise countermeasures.

Accordingly, it creates an environment in which high-precision simulations can be quickly performed without the need for design experience. Furthermore, because the system not only has enhanced simulation functions but also enables seamless connection to CAD tools used in various design stages and provides a component database for analysis use, it makes design tasks easier by utilizing simulation.[4] This electrical-characteristics simulation environment has made possible combined signal-integrity analysis and power-integrity analysis, which has encouraged many people to use SignalAdviser: indeed, more than 3000 licenses—an exceptionally high number for the electrical design industry—for it are granted annually across the entire Fujitsu Group.

3. Signal-integrity analysis

Signal-integrity analysis can be divided into two categories: "pre-layout analysis" (performed before layout design) and "post-layout analysis" (performed after layout design). Moreover, to enable analysis to be performed accurately in a short time, it is important to maintain information for analysis in a components database ("analysis library" hereinafter). These two types of analysis are described in detail in sections 3.1 and 3.2. For signal integrity analysis, Fujitsu has developed and is using SignalAdviser-SI, which replaces the older discontinued analysis system, SIGAL-SI.

3.1 Pre-layout analysis

Pre-layout analysis is simulation performed in the planning-design stage and in the circuit-design stage. In addition to linking LSI floor planning CAD and circuit CAD, it provides a topology-editing function for checking the arrangement and interconnection of components from a clean slate (namely, without CAD data).

Pre-layout analysis involves tasks such as verifying component characteristics, determining

transmission line topology, verifying the effects of manufacturing variations in components and substrates, investigating terminal processing and electrical-resistance constants, and investigating transmission line constraints during layout design. Implementing "sweep analysis" (namely, varying parameters such as transmission line length and resistance to determine their effects) and "variation analysis" (namely, arbitrarily combining manufacturing variations in components and substrates) makes it easy to perform the abovementioned investigations.

3.2 Post-layout analysis

Post-layout analysis is simulation performed midway through or after the layout-design stage and is linked to layout CAD. This analysis uses actual component layouts and transmission line-pattern conditions. As well as selecting and analyzing arbitrary components and networks during layout CAD, it provides a function for performing batch simulation for comprehensive verifications after layout design.

This simulation may be omitted for components, parts, and circuits on the basis of design data from previously manufactured products. It is performed only for the newly designed components, parts, and circuits; during this simulation, operating margins and so on are validated accordingly. In such cases, the batch-analysis function of post-layout analysis is effective.

3.3 Analysis library

Signal-integrity analysis requires an "input/output buffer information specification" (IBIS) model, in which the characteristics of the LSI input/output buffers are defined. Although IBIS models are provided by many semiconductor-device manufacturers, they present problems such as syntax errors and/or inconsistent characteristics. As a result, it is necessary to check the quality of such models before using them in a simulation. Furthermore, their contents are sometimes changed, information is added, and so on, making it necessary to confirm the presence or absence of changes at fixed intervals. Through unified processing using an analysis library in a cloud, as shown in **Figure 3**, Fujitsu Group companies are working to improve the efficiency of work involving manual inputting, checking, and updating of models. Moreover, the feedback received via measurement and analysis results from designers is used to determine whether the characteristics of an IBIS model fit the actual products. When an IBIS model is found to be anomalous, it is withdrawn from the library, and a request for revision is sent to the vendor. In this way, the quality of the analysis library is continuously improved.

3.4 Example signal-integrity analysis

An example of applying signal-integrity analysis when designing PCBs for the FLASHWAVE7500 optical-transmission system and investigating transmission line constraints is shown in **Figure 4**. If a chip-select (CS) signal is transmitted between CPU-DDR2 memories, this circuit network receives a signal output from one pin of the CPU at nine DDR2 memories. This causes a waveform disturbance due to reverberation and a deficient driving-force capability on the output side. Analysis results for the minimum possible total transmission line length are presented in Figure 4 (a). Although the driving force is sufficient, the waveform is significantly disturbed by reverberation. In contrast, as shown in Figure 4 (b), it is possible to avoid this noise problem by restricting the transmission line-length difference and by reflecting the restriction in the design constraint conditions for CAD.

Another example from PCB design for the FLASHWAVE9500 system is shown in **Figure 5**. The 1700 networks (out of approximately 4800) carrying signals that were causing concern about noise problems (regarding, for example, clock and high-speed memory interfaces)

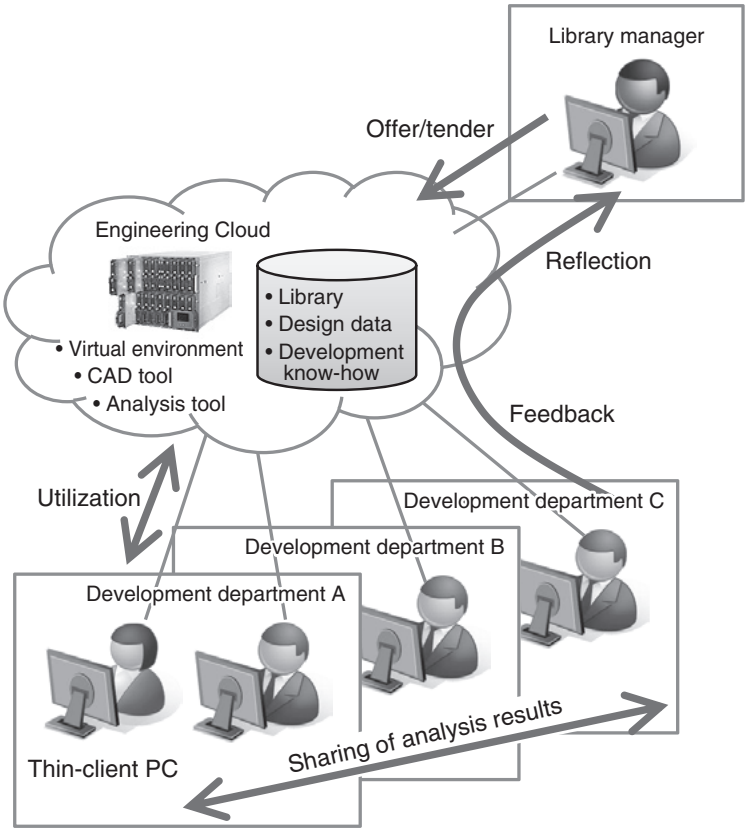
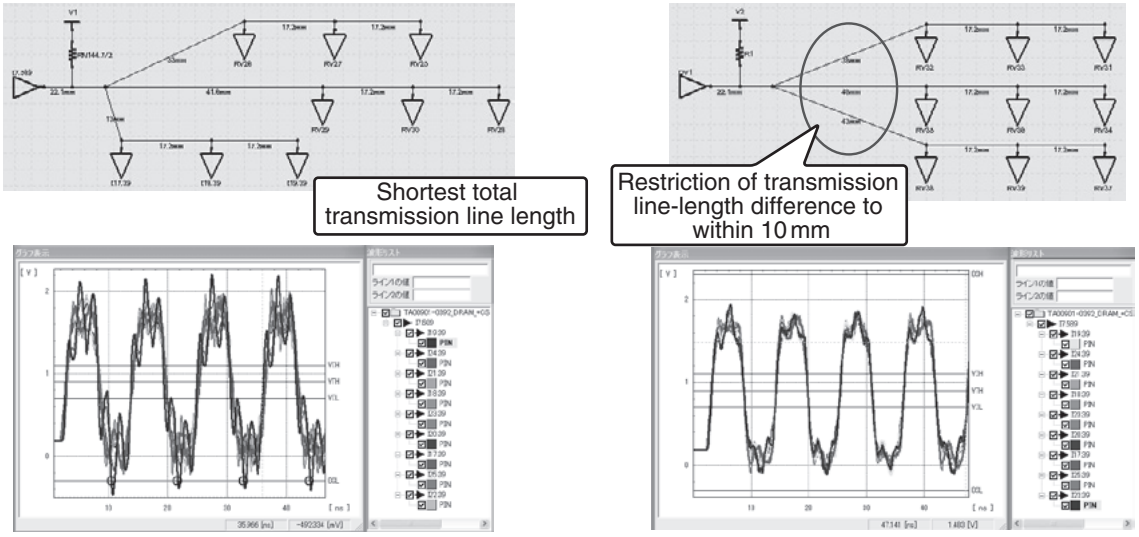


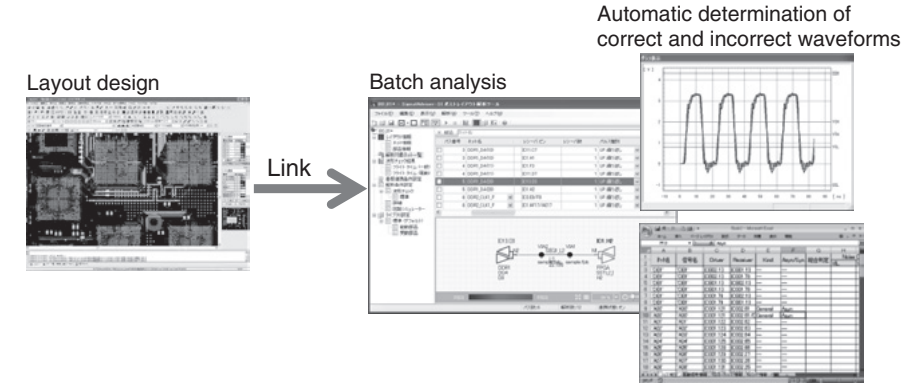
Figure 3
Simulation in cloud environment.



(a) Before implementing restriction

(b) After implementing restriction

Figure 4
Example implementation of design constraint on basis of signal-integrity analysis.



Example analysis-target list

Net name	Analysis target	Measurement point	Determination result	Details of circuit measurement
GTXCLK1	Yes	I6.748	OK	None
GTXCLK2	Yes	I6.745	OK	None
L2SW_CLK125	Yes	I44.7	OK	None
MC_CLK125M	Yes	I6.275	OK	None
RXC1	Yes	I9.222	Failure (steps)	Resistance change R868 (39 Ω→18 Ω)
RXC2	Yes	I9.125	OK	None

125 (CLK) 400 (DDR_W) 400 (DDR_R)

Figure 5
Example post-layout analysis.

were comprehensively analyzed after layout design. After the network targeted for analysis was selected in accordance with the layout-design data, analysis-model creation and simulation were lumped together with waveform determination and executed. The results are shown in Figure 5 in the form of a spreadsheet showing a list of analysis target examples. Changing the transmission line patterns or changing the resistance of the damping resistor or adjusting the driving force of the drivers on the basis of the problems revealed by this analysis makes it possible to build quality into products during the design stage and to develop devices without having to rely on previous ones. If a huge number of networks are analyzed (as in the example described here), the results of the comprehensive analysis are checked by several designers. Establishing an analysis environment in the cloud, as shown in Figure 3, makes it possible to share the results without having to duplicate and transfer data between designers. This is an important advantage of cloud technology.

4. Power-integrity analysis

Devices designed by the Fujitsu Group contain large-scale PCBs (i.e., PCBs with over 20 layers) for applications such as high-end servers and optical-transmission devices. The SignalAdviser-PI power-integrity analysis system (formerly "SIGAL-PI"[1),5),6)]) developed and supported by Fujitsu enables quick-turnaround simulation even for such large-scale PCBs.

4.1 Efforts aimed at large-scale analysis

SignalAdviser-PI uses the "partial-element equivalent-circuit" (PEEC) method in the manner of a resistance-inductance-capacitance (RLC) mesh model to replace a PCB's power source

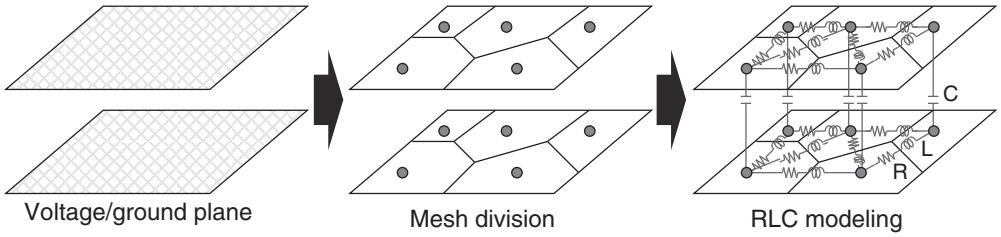


Figure 6
PEEC method.

and its ground-pattern sections with equivalent circuits composed of resistors, inductors, and capacitors connected in a network-like fashion (**Figure 6**). A simulation model is created by connecting equivalent circuits of power-supply components, capacitors, and LSIs, which serve as noise sources for the PCB model. Analyzing the models created in this manner with a circuit simulator makes it possible to analyze power source impedance and DC voltage drop. With simulation using this method, using an approximate method for RLC mesh modeling of the PCB power source and ground-pattern sections reduces analysis precision. Although precision increases with the fineness of the model's mesh, the analysis time also increases. Methods for reducing model size, improving circuit simulation, and so on targeted at PCBs with over 20 layers have led to an environment in which analysis can be completed in about one hour.

4.2 Example of DC voltage drop analysis

An example of applying DC voltage-drop analysis to the main PCB of the SPARC Enterprise UNIX server is shown in **Figure 7**. In this example, a reduction in the number of layers in the PCB (from 26 to 24) to reduce cost was investigated. In particular, since the DC voltage drop becomes worse as the number of layers is reduced, DC-voltage-drop analysis was carried out. The results for a +1.0-V power-source system (which has the lowest voltage-drop margin) are shown for the case in which

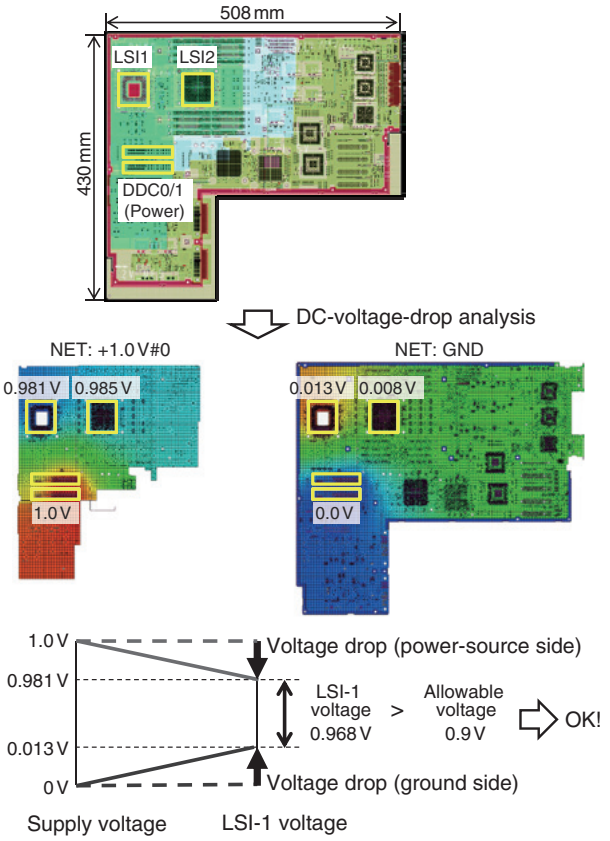


Figure 7
Example analysis of DC voltage drop.

two LSIs using this power source are operating simultaneously. The results demonstrate that the power-source voltages at the LSIs drop while the ground voltage rises. The DC voltage drops below the permissible value as a result of the reduction in the number of PCB layers. Thus, the analysis enabled us to advise against the proposed design change because reducing the number of PCB layers from 26 to 24 would have

led to low-voltage problems after production.

4.3 Example of power-source impedance analysis

An example of applying power-source impedance analysis to the same PCB as that used in the voltage-drop analysis is given in **Figure 8**. This PCB (508 mm × 430 mm) would conventionally have been designed on the basis of the required capacitance and number of capacitors estimated by calculation. As a result, it was difficult for the PCB designers to grasp the difference in impedance characteristics of the PCB for different capacitor layouts. Use of the power-integrity analysis (which is applicable to large-scale PCBs) enabled simulation using actual PCB data and made it possible to quantitatively understand the impedance characteristics of the PCB and thus optimize its design. For reference, the time required for the analysis (including all steps from creating the analysis model used in this example to performing the simulation) and other simulation conditions were as follows: the analysis frequency was from 1 Hz to 1 GHz; the required analysis time was 58 minutes; the memory used was approximately 640 MB; and the CPU was an Intel Core2Duo 6700 (2.66 GHz).

5. Conclusion

An electrical-characteristics simulation process established by Fujitsu was described in this report. Creating a simulation environment in which high-precision quick-turnaround simulation can be performed has enabled a broad range of designers to use simulation in practice without the need for design experience. By continuing to improve the convenience and information-sharing capability of this environment by utilizing cloud computing, Fujitsu will continue to improve product quality while shortening development times.

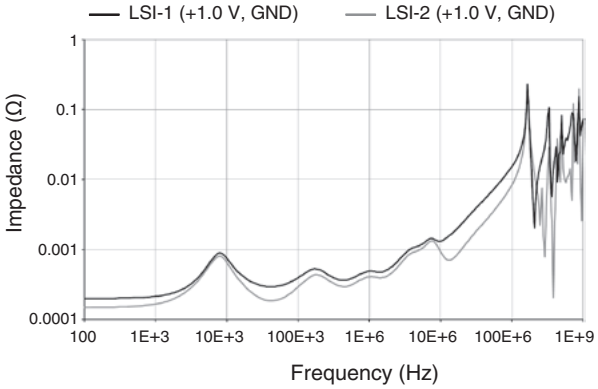


Figure 8
Example analysis of power-source impedance.

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