High-Speed Interconnect Technology for Servers

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We are developing high-speed interconnect technology for servers to meet customers' needs for transmitting huge amounts of data as quickly as possible. High-speed interconnect technology consists of high-speed I/O circuits and high-speed printed circuit boards (PCBs), and these technologies are optimized to achieve the target performance. This paper describes the architecture of I/O circuits that are part of efforts to develop high-speed transmission circuits. It also introduces the results of testing a prototype chip that was built to evaluate 20 Gb/s transmission. It goes on to describe efforts for improving PCB's simulation accuracy so that high-speed signals can be sent stably. For accurate simulations, we think it is important to accurately evaluate each part that makes up the transmission line and reflect the results in a simulation model.

1. Introduction

Multiple LSIs centered on processors are integrated in a server and signals are transmitted among these LSIs at the speed of several Gb/s. This speed has doubled in two years and high-speed interconnect technology serves to significantly differentiate a particular product from its competitors.

To achieve high-speed transmission, it is essential to have I/O circuits integrated in each LSI, developed by using the latest semiconductor technologies, and a high-speed printed circuit board (PCB) to transmit its signals. The authors develop these I/O circuits, determine the specifications of the PCB and combine them optimally to achieve the target performance for customers. Besides achieving high-speed transmission, stable operation is also an important requirement to be considered in the development phase.

This paper describes the trends in the development of the latest high-speed I/O circuit to support high-speed interconnect technology, as well as the technological development to enable the stable operation necessary to achieve high-speed transmission on a PCB.

2. High-speed I/O circuit

2.1 Technical challenges

In the conventional servers, a system called a "parallel interface" has been used where 1 Gb/s class signals are used in parallel for high-speed transmission inside the system. With the enhanced performance of CPUs for servers in recent years, there are needs to improve the comprehensive signal throughput in the whole CPU chip. However, because a circuit system called a "single-end" system has been adopted for conventional signal transmission circuits, where one channel is involved in transmitting one bit, it is hard to increase the transmission speed particularly due to the impact of noise caused through simultaneous changes of multiple signals.

To address this issue, the authors have been engaged in developing high-speed I/O circuit technology to support 10 to 20 Gb/s backplane transmission optimized for high-performance, highly reliable servers of the next generation. As a part of this effort, we adopted a new differential serial interface to achieve high-speed signal transmission. While the differential signal transmission requires two signal lines per bit, the occurrence of noise is minimized in comparison with the single-end transmission. This allows the impact of extraneous noises to be eliminated, which is an advantage for high-speed transmission. Nevertheless, we need to find a solution to comply with the requirements for sophisticated analogue circuit design technology in terms of signal waveform restoration and highly accurate timing control.

Furthermore, it is imperative to install a CPU requiring high integration in this high-speed I/O circuit. Therefore, another challenge is to develop the circuit in the design phase based on an advanced semiconductor manufacturing process where the characteristics of circuits are highly susceptible to fluctuations.

Moreover, in response to society's recent awareness about reducing environmental impact, we set low power consumption and space saving as a part of our development objectives. By saving the space on a chip, more I/O circuits can be integrated on a semiconductor chip, which results in better comprehensive signal throughput and enhanced system performance. However, because advanced semiconductor devices tend to indicate a higher leakage current, it is known to be difficult to reduce consumption power and achieve a compact analog circuit section.

To find solutions to the technical challenges associated with the above-mentioned new technologies and development objectives, our efforts are centered on optimizing the circuit configuration through simulations and developing and evaluating test chips.

Further, aiming to satisfy the product requirement of integration in high-reliability servers, we set up policies to adopt an α-ray resistant latch at significant points inside the high-speed I/O circuit and to add parity error detection circuits.

2.2 Application technologies

The configuration of a high-speed I/O circuit is indicated in **Figure 1**. Signals are

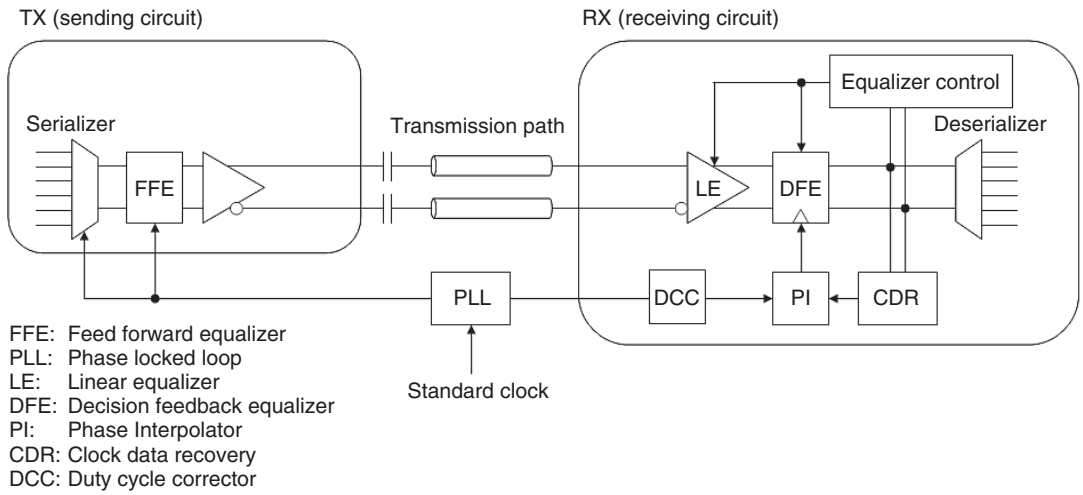


Figure 1
Block diagram of high-speed transceiver circuit.

transmitted from a sending circuit (TX) on the left to a receiving circuit (RX) on the right via a transmission path such as board wiring based on the differential transmission method. A serializer is a circuit used to transfer parallel data driven by a relatively slow clock inside a chip into serial data driven by a quick clock. A feed forward equalizer (FFE) is a circuit used to compensate for the loss of high-frequency signals at the transmission path (by generating signals on which high frequency is emphasized in advance). It outputs its signals to the transmission path via a differential output path. Normally, a capacitor to eliminate any direct current element is connected to the transmission path in a serial connection. A linear equalizer (LE) integrated in the differential input circuit will improve the quality of signals transferred to RX via the transmission path by amplifying the attenuated high-frequency element. In the next step, application to a circuit called a decision feedback equalizer (DFE) is conducted. DFE is a circuit to improve signal quality by changing the current value of the logic decision based on the logic information of past signals. This feature is effective when transmitting signals via a transmission path with a significantly high frequency loss. A mechanism is adopted for the LE and DFE inside RX that allows an equalizer control circuit to set the optimal value automatically.[1] The logic data received by the DFE are transformed into relatively slow parallel data via a deserializer and output to the chip internal circuit. At a duty cycle corrector (DCC), the clock edge relationship is adjusted at both the rising and falling waveforms of the high-speed clock generated in a phase locked loop (PLL). Then regarding data receiving timing at the DFE, fine adjustment of the clock edge phase at a phase interpolator (PI) is conducted to enable a highly accurate data strobe. With regard to the PI phase setting, data edge information is filtered digitally at clock data recovery (CDR) so that a clock phase should be adjusted to be automatically positioned on the center of an effective data window.

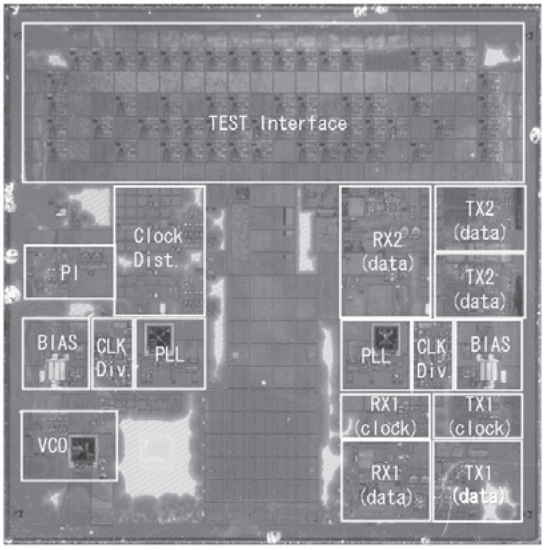


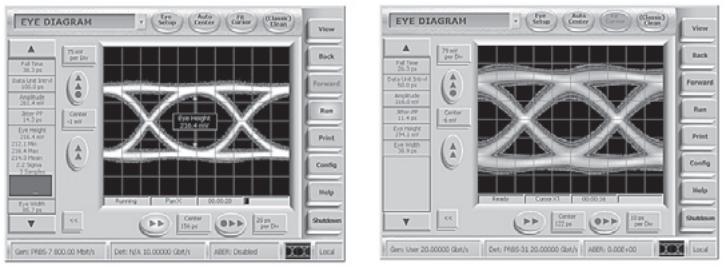
Figure 2
Outline of test chip.

An overview of a test chip is indicated in **Figure 2**. This test chip was designed to evaluate a whole element circuit.

The results of measuring a waveform output from the sending side of the test chip in Figure 2 are indicated in **Figure 3**. A high-quality waveform of the target range (10 to 20 Gb/s) could be obtained. Operation of the signal receiving side was also checked and judged to be at a level close to its completion as an element technology.

We have developed multiple types of test chips so far, and technological development is being promoted using both real devices and simulations by, for instance, improving the accuracy of simulation models based on the results of evaluating those test chips.

We will start working on advanced technologies to further improve performance, while redoubling our efforts for detailed product designs targeting commercialization.



10 Gb/s 20 Gb/s

Application data: PRBS31 (Pseudo Random Bit Sequence 31)

Figure 3
Waveform of test chip's output.

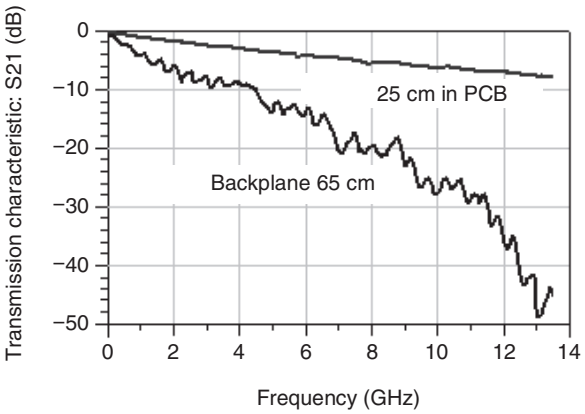


Figure 4
Comparison of transmission path conditions.

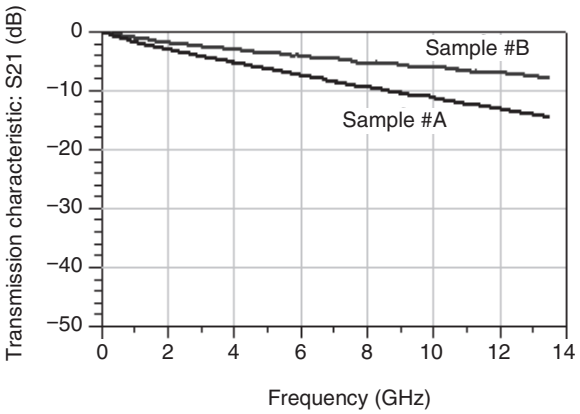


Figure 5
Comparison of PCB material characteristics.

3. High-speed printed circuit boards

3.1 Characteristics of transmission path and PCB

Attenuation of signals on a transmission path and degradation of signal waveform due to reflection noise are factors that hinder high-speed transmission. Because the wiring of a PCB is long and the transmission path is constructed across multiple PCBs in backplane transmission particularly, these factors cause serious problems. **Figure 4** indicates the actual measurements of transmission characteristics (S21) of a 25 cm transmission path in a PCB and a transmission path (65 cm in total) comprised of three PCBs including a backplane. Comparing the transmission loss at 10 GHz, the former path indicated –7 dB while the latter path indicated –28 dB. These values can be interpreted as meaning that the signal size (amplitude) output from the sending circuit will become 19.95% and 0.16% respectively, when they arrive at the receiving circuit. This shows the significant difficulty of achieving high-speed transmission in backplane transmission.

Attenuation of electric signals occurred during the transit of the transmission path because of the conductor loss caused by the skin effect of signal conductors and a phenomenon called dielectric loss, which arises because of the dielectric tangent (tan δ) of the insulation material. Losses related to the conductor can be improved by minimizing the surface roughness of single conductors, and dielectric loss can be improved by using materials with a low tan δ (low dielectric material). **Figure 5** indicates

the actual measurements of transmission characteristics (S21) for different PCB materials. Sample #A used a conductor with a standard surface roughness and dielectric material, while Sample #B used a conductor with a reduced surface roughness and low dielectric material. Although the width and length of the wiring on the PCB between both samples were the same, a significant difference was observed in their transmission loss.

The reflection noises generated in a transmission path are attributable to the inconsistency (disturbance) of characteristic impedance at connections of elements (via, footprint of components etc.) comprising a transmission path. For this reason, it essential to design a PCB (packaging design) with impedance matching that helps to decrease the impact of reflection noise. **Figure 6** shows an example of impedance matching achieved by optimizing the footprint geometry for the connector components of surface implementation that comprises a transmission path. The quality of a transmission waveform can be drastically improved through impedance matching, achieved by changing the GND pad geometry and GND via layout.

3.2 Measurement, verification and evaluation

An effective way to precisely verify the phenomena generated in these transmission paths is to obtain measurement data of transmission path characteristics by using pilot devices. However, it is impossible to make and evaluate all transmission paths because there are more than 1000 pieces of wiring on a server PCB. Therefore, verification based on simulations is essential. We will report our approaches for evaluating the transmission path characteristics in the below.

To verify a transmission path based on a simulation, a high degree of consistency between the simulation and measurement results is necessary. In this case, however, matching the result extracted from measuring characteristics of a comprehensive transmission path with the simulation result is not an essential requirement. Because a transmission path is comprised of

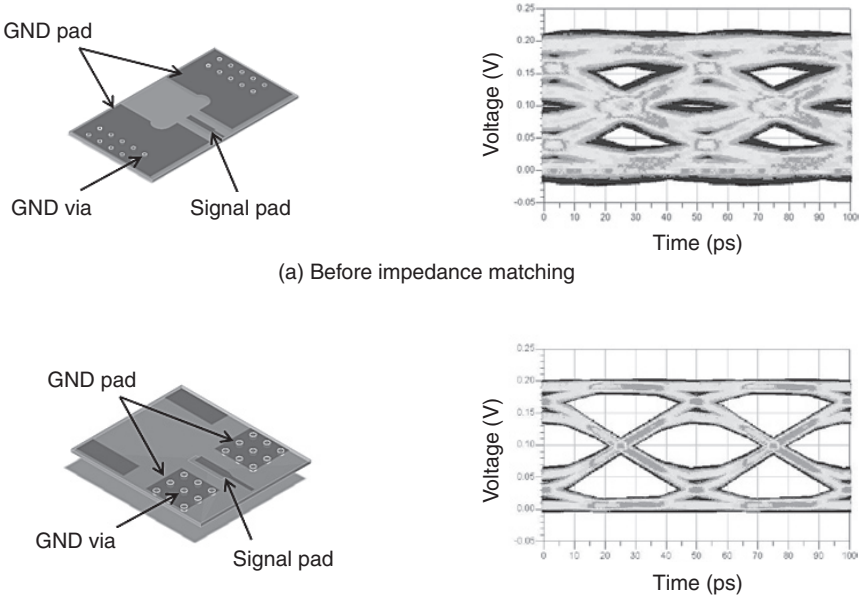
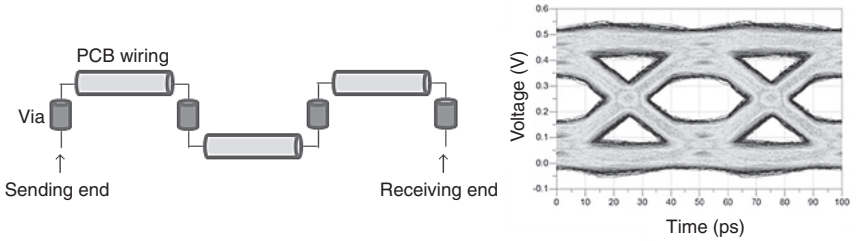
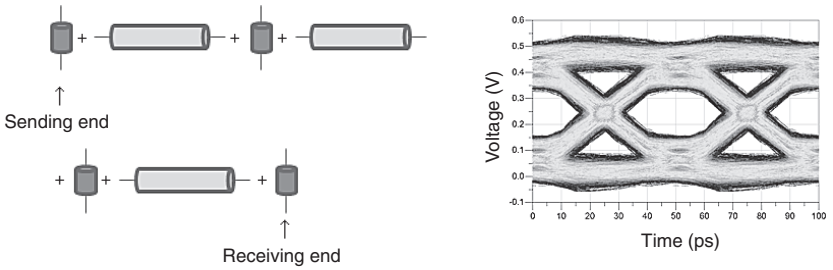


Figure 6
Implementation of impedance matching.



(a) Comprehensive transmission path characteristics



(b) Extract and add up individual elements of transmission path

Figure 7
Comparison of measured and extracted transmission path models.

multiple elements such as PCB wiring, connectors and vias, it is impossible to identify which element contributes to a discrepancy or which transmission path component is generating an error, if any inconsistency is observed between both data. Further, even if both data matched, it may be impossible to ignore errors if there is any difference in the transmission path conditions. Therefore, the key to evaluating transmission path characteristics is the precise extraction and evaluation of characteristics in an individual transmission path component instead of those of the comprehensive transmission path. **Figure 7** and **Figure 8** indicate the results of verifying the measurement accuracy and validity of our approach to evaluate a given transmission path in this process.

Figure 7 is a comparison of measured and extracted transmission path models, where path characteristics were measured and analyzed as S parameters for the same PCB wiring and signal waveforms for transmission simulation using S parameter as a model were developed. Figure 7 (a) represents the characteristics of a comprehensive transmission path, while Figure 7 (b) represents the sum of extracted and added-up data for an individual component of the transmission path. A high level of agreement is observed between both data. This demonstrates the following facts: precise measurement of an individual component of the transmission path could be achieved, and verification of any given transmission path is possible by combining its individual components.

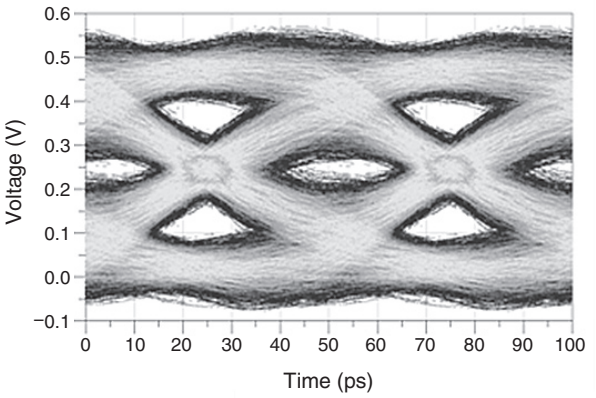


Figure 8
Effect of measurement system.

When separately measuring and extracting individual transmission path components, in the case of a transmission path component such as a via for instance, it is impossible to ignore the impact that the measurement system has on the measurement results, as it may degrade the measurement accuracy. Accordingly, it is essential to have calibration technology to eliminate the impact of the measurement system to establish this evaluation approach.[2] While the graph shown in Figure 7 (b) indicates the state in which the impact of the measurement system is eliminated, the graph in Figure 8 indicates the state before eliminating the impact of the measurement system. This result demonstrates the importance of calibration technique.

It is possible to generate a highly accurate model for the transmission path based on the feedback of highly accurate measurement results and the observation data of a cross section for the measured transmission path to electromagnetic simulations. With this approach, it is possible to more quickly assess manufacturing dispersions and evaluate combinations for comprehensive transmission path conditions, while the scope of evaluation would be limited if real pilot models were used.

Figure 9 is a graph where a waveform of the transmission simulation using the above-mentioned verification technique is superimposed on the waveform based on actual measurement of signals transmitted from the measurement unit. While the simulation result does not include source-related noise or jitter element associated with the oscillator inside the measurement unit, both waveforms overlap completely, demonstrating the high degree of consistency.

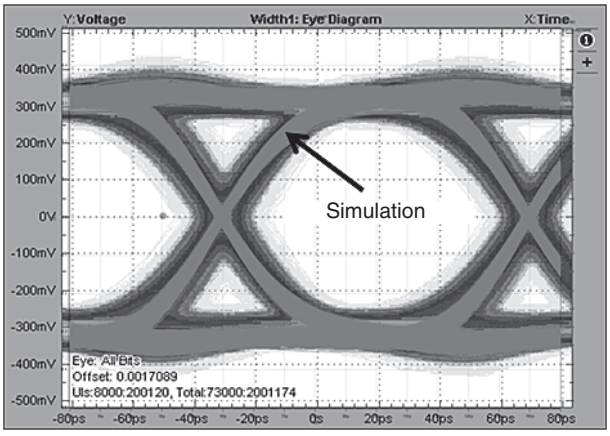


Figure 9
Comparison between simulated and measured transmission waveforms.

Through the above-mentioned approaches, the method of verifying a transmission path at 20 Gb/s transmission has been established. These approaches are considered to be technologies that can optimize the characteristics of high-speed PCBs.

Precise verification of transmission path characteristics not only helps to improve PCB design but also is beneficial in the pilot production and design verification of I/O circuits. We will remain committed to enhancing measurement accuracy and simulation accuracy to be ready for transmission at a speed higher than 20 Gb/s, where even a small impact of transmission path components would be difficult to ignore.

4. Conclusion

This paper reported on some high-speed interconnect technology for server applications.

The demand for greater server performance will become more intense and technological development to address high-speed transmission will become more important in future.

While the currently dominant transmission method uses electric signals, the progress of silicon photonics will soon bring the age of the optical server, where optical signals from an LSI will be transmitted within PCBs. We are determined to continue working on technological development to enhance high-speed performance while giving consideration to these advanced technologies. Our aim is to meet customers' request for improved server performance. Meanwhile, we want to offer value to customers also in the area of stable operation as another important issue to be tackled.

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