

Analysis of Insulating Materials and Deep Interfaces by Auger Electron Spectroscopy

● Michiko Sato ● Shiori Shirai ● Yoshihiko Seyama ● Toru Itakura

(Manuscript received December 28, 2009)

Auger electron spectroscopy (AES) is a powerful tool for investigating the composition of minute particles and thin films as well as the compositional distribution of elements in the depth direction of multilayered films and metallic-bonded interfaces. However, non-conductive materials are generally difficult to analyze because of the charge-up phenomenon generated by the exciting electron beam. Furthermore, in a “depth profiling” analysis performed simultaneously with sputter etching, if the target analysis site is deep beneath the sample surface, the depth resolution is degraded by effects such as surface roughness and mixing, so precise evaluation is difficult. To solve these problems, we have investigated an AES analysis technique that uses a thin sample processed by a focused ion beam. It enables measurement free from charge-up even if the sample is composed of insulating material and achieves depth profiling with outstanding resolution even at analysis sites (such as interfaces) deep within the sample.

1. Introduction

Auger electron spectroscopy (AES)¹⁾ is a method of analyzing the type and amount of elements on a solid surface to a depth of several nanometers by measuring the energy and signal intensity of Auger electrons generated when a finely focused beam of electrons irradiates the surface. In simultaneous use with secondary-electron microscopy and ion-sputter etching, AES can provide compositional analysis of localized regions and measure compositional changes in the depth direction from the surface (hereinafter, “depth profiling”) with high positional resolution.

Since the excitation source is a beam of electrons, some of the electrons in non-conductive materials pile up. This phenomenon, which is called “charge-up”, makes the analysis of such materials difficult. Measurement without charge-up is possible if the insulating regions are minute or a thin film on a conductive substrate. In other words, if most of the incident electrons

penetrate so that they do not stop above the measurement region, charge-up does not occur and AES analysis is possible. Even though a desired analysis (such as element distribution in sample cross sections including insulating materials) is feasible after suitable processing, AES analysis should sometimes be done after the sample has been further processed to reduce its thickness enough to allow the electron beam to penetrate the sample.

The maximum depth from the sample surface that can currently be depth-profiled at the same time as ion-sputter etching is 1–2 μm . However, interfaces between joints (such as solder) and multiple layers are normally located deeper, where measurement time becomes excessively long and depth resolution decreases owing to the influence of surface roughness and mixing. Given those circumstances, we have performed AES depth profiling after processing a sample (containing interface regions targeted for

analysis) into a thin section with a thickness of 1–2 μm.

In this paper, we overview our sample processing method and then present examples of successful AES analyses of an insulating material and of a deep interface. Until now, such deep interface analysis has been impossible.

2. Thin sample preparation

If the sample for analysis is less than a micrometer (i.e., several hundred nanometers) thick, a large portion of the 10-keV electron beam normally used for AES analysis penetrates into the sample interior (although the amount of penetration depends on the material in question). Data about the etching depth achieved during depth-profiling analysis should ideally be obtained with good depth resolution in the shallowest direction possible, which for all practical purposes, is no more than 1 μm. Accordingly, a small, thin analysis sample—in the form of a section several hundred nanometers long containing the target interface—should be cut out from a large, thick sample.

To achieve such precise processing, we use

a focused ion beam (FIB). An accelerated beam of gallium ions is focused by an electrostatic lens and scanned over the sample surface. This method can shave target sites of a sample with high positional accuracy (i.e., a few tens of nanometers) by detecting the generated secondary electrons as images.²⁾ Moreover, FIB can deposit an electrically conductive film (such as tungsten) on an arbitrary region of the sample surface by irradiation under a flow of coating material source gas.

Schematic diagrams showing examples of the processing for cross-sectional surfaces of materials including insulating ones are shown in **Figure 1**. Figure 1 (a) shows a method called “lift out” (or “pick up”), which is widely used to make transmission electron microscope samples made by applying FIB processing to the sample and taking out a small, thin section. Figure 1 (b) shows a method that avoids charge-up in the case of observing and analyzing a box-shaped hole (formed by FIB) from an oblique angle. In this method, another hole is opened up behind the first one, and the site to be analyzed is thinned to a few hundred nanometers. After that, tungsten,

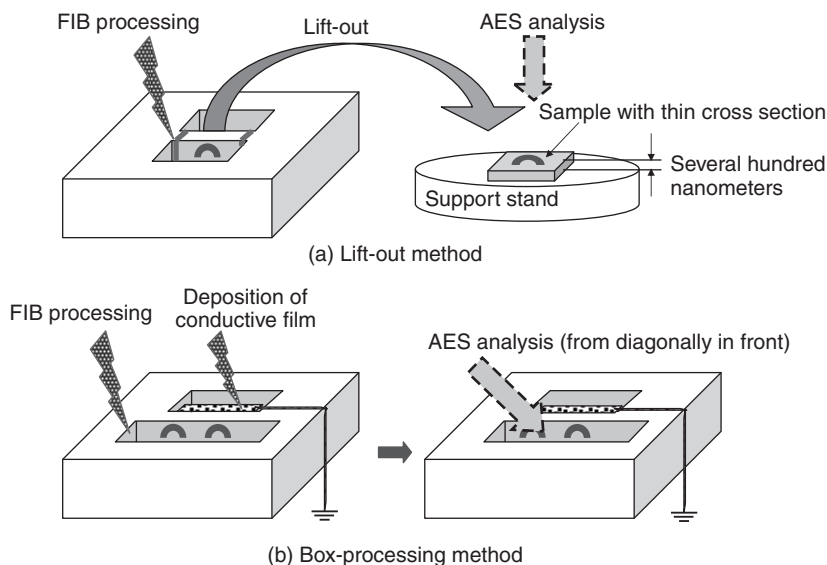


Figure 1
Two methods of preparing thin cross-sectional samples.

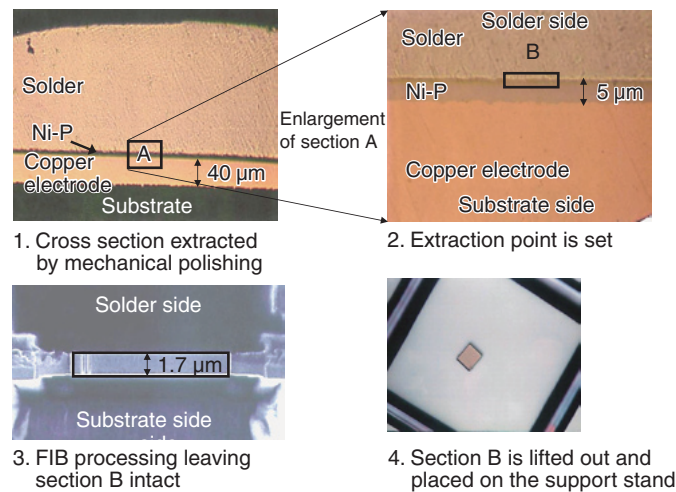


Figure 2
Sample preparation process for depth-profiling analysis of deep interfaces.

for example, is deposited on the rear of the thin film to form an escape route for the primary beam electrons. Compared with the lift-out method, the box-processing method has three advantages: there is no risk of the processed sample being lost, a wide region can be processed, and processing is simple.

On the other hand, the lift-out method enables depth-profiling analysis in conjunction with sputter etching of insulating materials and deep interfaces. Thin-section processing to form a sample for depth-profile analysis of an interface formed by soldering a terminal to a substrate is shown in the micrographs of an observed sample in **Figure 2**. Standard resin embedding and mechanical polishing were performed, and the bonded interface was first observed from the cross-sectional direction (images 1 and 2). Holes were opened up by FIB above and below the region of the bonded interface to be analyzed (region B in image 2) in a manner that left that region after the FIB processing (image 3). The interface region to form the thin section (i.e., sample) was lifted out and set on a suitable support stand (image 4). The extracted section was then sputter etched and depth-profiling analysis was performed.

3. AES analysis of cross section including insulating material

For cross-sectional analysis, a typical method is to form a box-shaped hole by FIB and then observe and analyze the cross section from an oblique angle. However, charge-up in sections of insulating film often prevents secondary-electron-microscopy observation and AES analysis. As shown in the example in **Figure 3 (a)**, part of the conventional secondary-electron image is abnormally bright, the AES spectrum is distorted, and noise is generated. On the other hand, as shown in **Figure 3 (b)**, for the thin-film cross section made by the box-processing method, charge-up was suppressed and the region with the insulation film lost its shine, enabling a normal AES spectrum without distortion or shift to be obtained.³⁾

4. AES depth profiling of insulating materials

In the depth profiling of thin films and insulating thick films on insulating substrates, if the thickness of the whole sample is less than 1 μm, charge-up does not occur and AES analysis is possible. For a sample consisting of silicon-dioxide (SiO₂) film deposited on an insulating

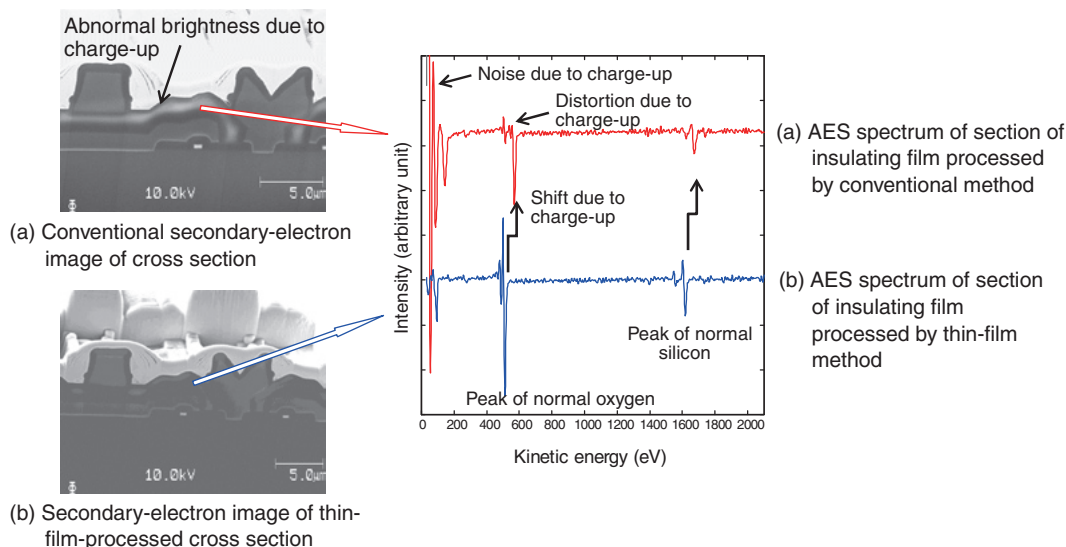


Figure 3 Secondary-electron images and AES spectra of cross-sectional sample including insulating film.

substrate like lithium niobate (LiNbO_3), to ensure that pre-deposition contamination (from carbon, for example) does not remain at the film-substrate interface, a thin sample is prepared and depth-profile analysis is performed by AES.

The results of an AES depth-profile analysis are shown in **Figure 4**. For depth-profile analysis, etching by argon-ion-beam bombardment and AES spectra measurement were performed alternately, and the distributions of elements in the depth direction were profiled as a graph with distance in the depth direction (calculated from the etching rate and etching time) plotted on the horizontal axis and element concentrations (calculated from peak intensities) on the vertical axis. Although predicted AES spectra for carbon and other elements have also been measured, such spectra were not obtained from the $\text{SiO}_2/\text{LiNbO}_3$ interface though titanium was detected in the SiO_2 film.

In the above manner, a previous study ascertained that if the sample was made as thin as possible, then even if it consisted of an insulating layer on an insulating substrate, charge-up did not occur and AES depth profiling was possible.⁴⁾

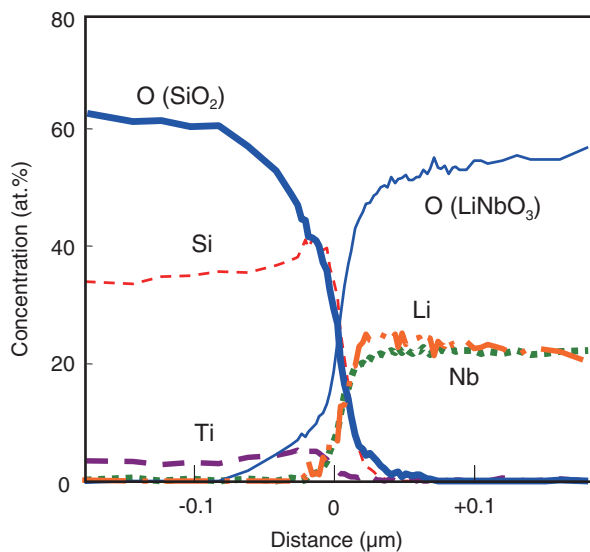


Figure 4 Results of AES depth-profiling analysis of $\text{SiO}_2/\text{LiNbO}_3$ interface.

5. AES depth profiling of deep interfaces

In an effort to solve the problem of solder peeling away from an interface, we analyzed a peeling surface by AES with an advanced depth-profiling capability (profiling with depth resolution of about 10 nm), which can provide

valuable information that lets us, for example, identify an interface with peeling solder or determine whether there are inclusions in that interface. And considering the problem of high-temperature detachment of products with components (such as tin-coated copper terminals) attached to printed circuit boards by lead-tin solder (as manufactured, i.e., before use), we performed AES analysis of a detached surface. The results showed the presence of a layer of palladium-tin alloy coated on the substrate-side electrode on the component-side of the peeling surface; on its substrate side, a nickel-phosphorus (Ni-P) layer appeared below the palladium, and at the Ni-P/Pd interface, there was a lead-tin (Pb-Sn) layer. We found that solder detachment occurred at the Pb-Sn layer.

To determine the conditions under which this detachment occurs, we prepared reference samples under different soldering conditions that had bonded interfaces with no detachment at a depth of several tens of micrometers from the sample surface. Since conventional AES depth profiling would have been impossible, we made thin samples by the lift-out method (Figure 2) and analyzed them. The results of AES depth

profiling near interfaces in the thin lifted-out reference samples (with soldering times of 2 s and 5 s) are shown in **Figure 5**, where the substrate side is on the right. Since each sample was measured with the substrate side up, the etching time for the right side was shorter, and the increased carbon concentration at the left edge of the figure originates from the electrically conductive adhesive tape used to support the sample. In other words, when the left edge of the figure was reached, the thin sample was being etched completely.

For soldering time of 2 s, a primary structure consisting of lead-tin solder/palladium-tin alloy/palladium/nickel-phosphorous layers was maintained. In contrast, for soldering time of 5 s, lead was detected between the palladium-tin alloy and the nickel-phosphorous layer. That is to say, as soldering time was increased, the palladium layer blended completely into the lead-tin solder. After that, a lead-containing layer could form between the palladium-tin and nickel-phosphorous layers by a solidification process. We think that that layer is probably the cause of the solder detachment.⁴⁾

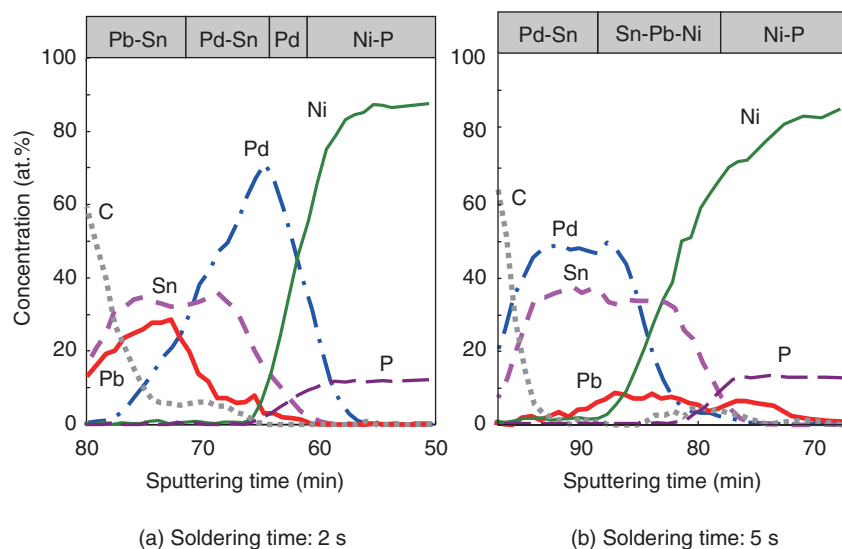


Figure 5
Results of AES depth-profiling analysis of solder-joint interface.

6. Conclusion

In this paper, we showed that by processing a sample into a thin section for AES analysis, we can analyze the cross-section of an insulator (hitherto impossible) and analyze the depth profile of insulating materials and deep interfaces. While most of the improvements in conventional analysis technologies have resulted from the efforts of analysis instrument manufacturers, from the user's standpoint, improvements also come through solutions found by devising methods for sample fabrication, data analysis, and so on. From now on, in response to the needs of customers who depend on materials analysis, we will strive to advance analysis technology to the best of our ability.



Michiko Sato

Fujitsu Quality Laboratory Ltd.

Ms. Sato received a B.S. degree in Physics from Aoyama Gakuin University, Tokyo, Japan in 1975. She joined Fujitsu Laboratories Ltd., Kawasaki, Japan in 1975 and studied surface analysis. In 1994 she moved to Fujitsu Analysis Laboratory Ltd., which was renamed Fujitsu Quality Laboratory Ltd., Kawasaki, Japan in 2006 and has

been engaged in surface analytical services. She is a member of the Surface Analysis Society of Japan.



Shiori Shirai

Fujitsu Quality Laboratory Ltd.

Ms. Shirai received a B.E. degree in Applied Science from Tokyo Denki University, Japan in 1992. She joined Fujitsu Laboratories Ltd., Atsugi, Japan in 1992 and has been engaged in research and development of analytical techniques for electrical materials. She is currently engaged in analytical services using FIB, SEM, AFM, and LSM in Fujitsu Quality Laboratory Ltd., Kawasaki, Japan.

References

- 1) Surface Science Society of Japan: Anthology of Surface Analysis Technology, Auger Electron Spectroscopy. (in Japanese), Maruzen Co., Ltd., 2001.
- 2) T. Adachi: FIB Unit and its Application. (in Japanese), *Electron Microscopes*, Vol. 30, No. 3, pp. 237–244 (1996).
- 3) S. Shirai, et al.: Deposition Technique with FIB for Observation and AES Analysis of Cross-section Samples Containing Insulating Materials. (in Japanese), *Journal of Surface Analysis*, Vol. 9, No. 4, 2002, Summary of Meeting on Application of Surface Analysis, A-1, (2002).
- 4) M. Sato, et al.: Application of Focused Ion Beam Technique to Thin-Film Sample Preparation for Auger Electron Spectroscopy-Sputter Depth Profiling of Deep Interfaces. (in Japanese), *Journal of Surface Analysis*, Vol. 15, No. 1, pp. 40–49 (2008).



Yoshihiko Seyama

Fujitsu Quality Laboratory Ltd.

Mr. Seyama received a B.S. degree in Physics from Chiba University, Japan in 1986. He joined Fujitsu Laboratories Ltd., Atsugi, Japan in 1986. Until 2003, he studied magnetic materials, particularly current-perpendicular-to-plane giant-magnetoresistance (CPP-GMR) multilayer films. He is now engaged in TEM analysis work in Fujitsu Quality Laboratory Ltd., Kawasaki, Japan.



Toru Itakura

Fujitsu Quality Laboratory Ltd.

Mr. Itakura received B.S. and M.S. degrees in Applied Physics Engineering from the University of Tokyo, Japan in 1979 and 1981, respectively. He joined Fujitsu Laboratories Ltd., Kawasaki, Japan in 1981 and studied focused ion beam technology and reliability engineering for semiconductor devices.

He moved to Fujitsu Quality Laboratory Ltd., Japan in 2006 and he is now engaged in surface analysis work. He is a member of the Japan Society of Applied Physics.