Two-Dimensional Carrier Profiling by Scanning Tunneling Microscopy and Its Application to Advanced Device Development

● Hidenobu Fukutome

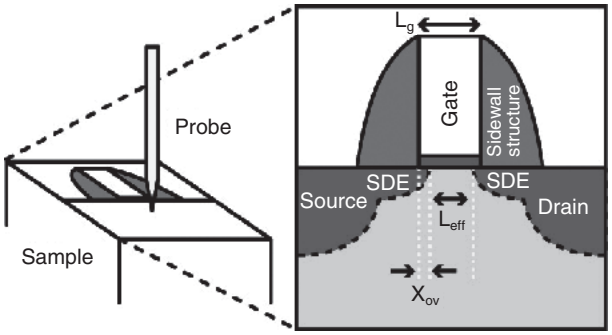
(Manuscript received December 28, 2009)

A high-resolution two-dimensional (2D) carrier profiling technique has been desired to optimize the dopant profile around the source/drain and extension region in transistors to enhance electrical characteristics when scaling the gate length down to less than 50 nm. At Fujitsu Semiconductor Ltd., high spatial resolution of about 1 nm has been achieved by scanning tunneling microscopy to enable the 2D carrier profiling technique to be applied to the development of scaled transistors beyond the 90-nm technology node. The dependence of the 2D carrier profile on process conditions was found to agree well with that of electrical characteristics. On the basis of such profiles, the dopant profile in scaled transistors has been optimized. The technique also enables an evaluation of dopant distribution fluctuations that cause variability in transistor performance. The dopant profile around the extension region was found to depend on the gate line edge roughness. On the basis of the measured results, various methodologies for suppressing transistor performance variability have been proposed.

1. Introduction

The scaling down of transistors—the basic building blocks of large-scale integrated circuits (LSIs)—is being actively pursued to increase the performance and integration of LSIs, which have found widespread use in all sorts of equipment including hand-held devices, digital appliances, and mainframe computers. As shown in **Figure 1**, a transistor consists of a gate electrode plus source and drain electrodes that are formed by a dopant profile in the silicon substrate below the gate. The transistor functions as a switch between its on-state and off-state by adjusting the current that flows between the source and drain at the gate. To scale down gate dimensions to less than 50 nm without degrading transistor performance, we must optimize the dopant profile formed below the gate. For example, if the distance between the source and drain (effective channel length) is short, the leakage current in the off-state is high, so the power consumed by the LSI in standby mode is high, which is undesirable.

There has thus been a need for a measurement technique that can visualize the



SDE: Source/drain extension region
X_{ov}: Lateral overlap length

Figure 1
Schematics of cross-sectional carrier profile in scaled transistor and its measurement method.

nanoscale dopant profile in the lateral direction (L_g direction in Figure 1). In this paper, I describe the results of applying a two-dimensional (2D) dopant profiling technique that my coworkers and I have developed using scanning tunneling microscopy (STM)[1] to the research and development of scaled transistors.

2. STM-based 2D dopant profiling technique

Dopant profiling techniques can be divided into two groups according to the object of measurement. That is, there are techniques that measure the total number of impurity atoms and those that measure electrically active dopants. A typical example of the former is secondary ion mass spectrometry, which corresponds to one-dimensional dopant profiling. STM-based dopant measurement is an example of the latter type. Both types of techniques are important in achieving efficient fabrication of scaled transistors. At the same time, various types of dopant profiling equipment based on a microscope and probe configuration have been researched and developed. Each of these reflects the features of this mainstay configuration. In general-purpose scanning capacitance microscopy, the probe tip has a large diameter, which has made it difficult to achieve the nanoscale spatial resolution needed for evaluating scaled transistors beyond the 90-nm node. In contrast, STM can achieve high-resolution 2D profiling of dopants in the silicon substrate, as described below.

2.1 Basic principle of STM

STM is a surface-measurement technology that uses the tunneling current flowing between the metallic probe and the surface of a sample. This tunneling current flows when the probe is brought sufficiently close to the sample to which a fixed voltage has been applied. Here, a 2D topographic image, of atomic steps for example, can be obtained by scanning the sample surface with the probe while keeping the tunneling current fixed by controlling it through a feedback loop. Since the tunneling current changes exponentially with respect to the tip-sample distance, excellent spatial resolution in the vertical direction can be achieved. In addition, the use of tunneling phenomena via an atom at the tip of the probe leads to extremely high resolution in the horizontal direction as well. In short, STM has atomic-scale resolution that can visualize individual surface atoms.

The tunneling current is a physical quantity that reflects the local carrier concentration near the sample surface, and since it attenuates exponentially with tip-sample distance, as long as there is no local Fermi-level pinning on the surface, the local carrier concentration reflected by the dopant concentration in the silicon substrate can be measured by STM. Appropriate application of hydrogen termination to the surface of a silicon sample can eliminate Fermi-level pinning on the surface, and this has made it possible to experimentally confirm the dependence of the tunneling current on sample voltage according to conduction type and carrier concentration.[2),3)] Moreover, measurements can be made in a high vacuum to reduce the effects of surface-adsorbed material and to maintain a hydrogen-terminated surface, thereby enabling measurements to be repeated a sufficient number of times at the same location.[4)]

2.2 Acquisition of 2D carrier profile images by CITS

As described above, a topographic image of a sample's surface can be obtained by STM. Since the sample-voltage (V_s) dependence of the tunneling current (I_t) reflects the local carrier concentration in the silicon substrate, current imaging tunneling spectroscopy (CITS),[5)] which can provide both a topographic image of the sample surface and the 2D distribution of the local I_t-V_s characteristic simultaneously, can be used in conjunction with a measurement location identification technique to obtain 2D carrier

profile images. A tunneling current image of a nanoscale pn junction as a specific example of how a 2D carrier profile can be obtained by CITS is shown in **Figure 2**. As shown on the left, the probe is scanned above the pn junction while the tip-sample distance is kept roughly constant. This enables the p-type and n-type regions, which exist as alternate strips with widths of about 100 nm, to be visualized because the tunneling current flowing between the tip and sample fluctuates as conduction type and carrier concentration change. In this way, a 2D carrier profile can be measured by CITS as a tunneling current profile.

2.3 Resolution of STM-based 2D carrier profiling

Here, I describe the resolution of STM-based 2D carrier profiling. Although STM itself has atomic resolution, there are other factors that determine the spatial resolution in carrier concentration measurement. In particular, energy band bending, which occurs as the probe approaches the sample surface, can be considered to be a primary factor, which sets a fundamental resolution limit that is estimated to be 1–2 nm. The carrier concentration measurement range, meanwhile, is about 10^{17}–10^{20} cm^{-3}, and the concentration resolution when expressed in scientific notation is one significant digit.[3] Thus, STM can achieve the level of resolution required for developing devices beyond the 90-nm node.

3. Better performance for scaled transistors

The results of observing a cross section of a scaled transistor as an example of STM-based 2D carrier profiling are shown in **Figure 3**. This is a 2D carrier profile of a p-type metal-oxide-semiconductor field-effect transistor (MOSFET) with a gate length of 38 nm.

To enable STM measurements, the sample cross section was first polished to obtain a flat observation surface with unevenness of less than 1 nm. Next, the sample was immersed in a hydrofluoric acid solution to selectively remove silicon dioxide film. This treatment resulted in hydrogen termination of the silicon surface to be measured by STM.[6] After the hydrogen termination was completed, the sample was transported to an ultrahigh vacuum and STM measurements were performed.

As described above, the outer geometric shape of the MOSFET, such as the gate electrode, was measured from a surface topographic image, and the 2D carrier profile was simultaneously obtained as a tunneling current profile image. By combining these two, we could successfully visualize the state of the source/drain extension (SDE) regions of the source/drain electrodes under the gate electrode. The obtained 2D carrier profile can be used to determine the nanoscale lateral overlap length of the SDE under the gate, X_{ov} (shown in Figure 1).

Using this evaluation method, we measured

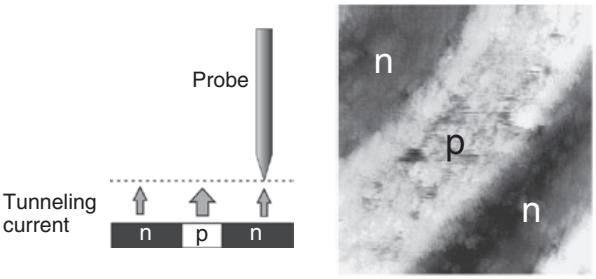


Figure 2
Tunneling current image of nanoscale pn junction.

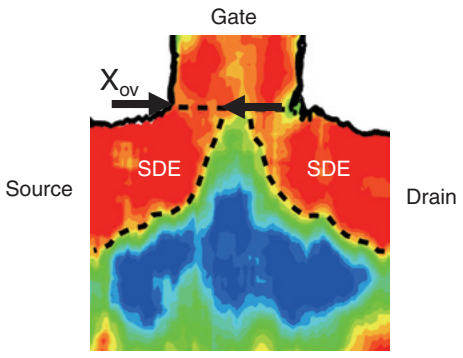


Figure 3
2D cross-sectional carrier profile of 38-nm p-MOSFET.

various transistor cross sections fabricated under different conditions and clarified that a difference in those conditions could change the average value of X_{ov} by 2 nm.[7] We also found that the STM measurement results agreed well with the device threshold voltage roll-off characteristics (threshold voltage gate-length dependence). In other words, we found that STM-based 2D carrier profiling technology has a spatial resolution of better than 2 nm, which makes it capable of contributing to the optimization of transistor process conditions.

Thus, by using STM technology to deepen our understanding and knowledge of the mechanisms behind dopant diffusion suppression techniques,[8] such as fluorine co-implantation, we were able to achieve dopant profile optimization in a relatively short time, which accelerated the development of advanced high-performance devices beyond the 90-nm node. By using STM, we were also able to directly evaluate the effects of small changes in the shape of the sidewall spacer[9] on the dopant profile and directly examine lateral anomalous diffusion of dopants along the interface of the sidewall spacer.[10] By correlating these findings with device performance, we were able to contribute to the optimization of 2D dopant profiles in the SDE regions.

4. Reduced variability in transistor performance

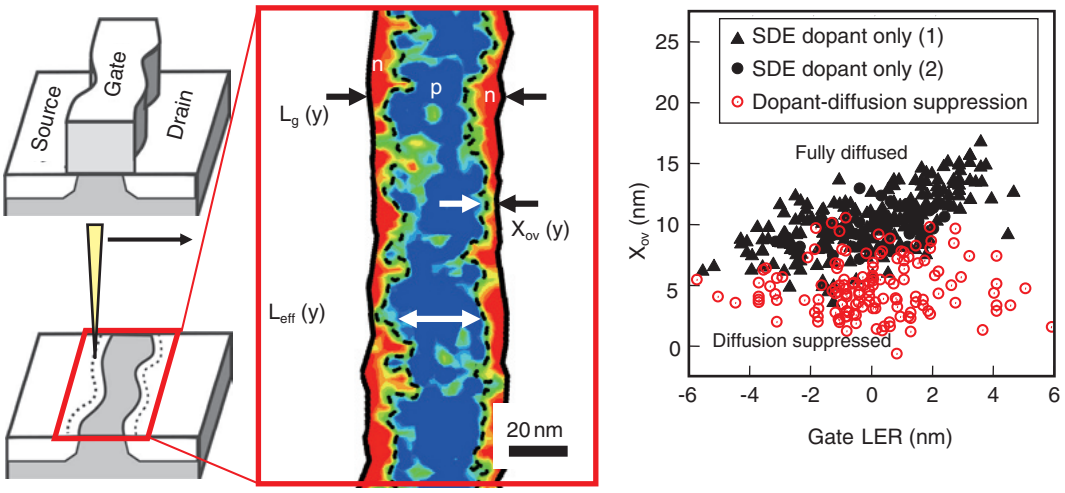
In addition to observing transistor cross sections, we also measured surface carrier profiles directly under the gate electrode. In scaled transistors, the threshold voltage is often determined by the leakage current between the source and drain, so the effective channel length (L_{eff}) is an important evaluation item. We therefore measured, for the first time in the world, the correlation between the gate line edge roughness (LER) and SDE profile.[4] There have been concerns that gate LER variability can affect the performance of scaled transistors. In the past, there was no way other than computer simulation[11] to check this, but now such phenomena can be evaluated directly by STM.

4.1 Evaluation of correlation between gate LER and SDE profile

Here, I outline a method for evaluating the correlation between gate LER and SDE profile. First, the gate is selectively removed to expose the active regions to be observed. Next, the same processing as in the cross-section measurements is applied to remove the sidewall structure and gate insulation film, and the active-region surface is hydrogen terminated. As a result, at the time of gate processing, the silicon substrate in the transistor fabrication process is dug away by several nanometers, which transfers the gate shape to the active-region surface. Consequently, the position of the gate edge can be extracted from a topographic image, and at the same time, the 2D carrier profile of the active-region surface can be obtained by measuring the tunneling current profile. By combining these two pieces of information, we can evaluate the correlation between gate LER and L_{eff} fluctuation or X_{ov} fluctuation.

4.2 Evaluation results

A typical 2D carrier profile of the SDE and the channel region directly underneath the gate electrode in an n-MOS transistor with sub-50-nm gate lengths is shown in **Figure 4**. As shown in Figure 4 (a), gate length L_g (y), lateral overlap length X_{ov} (y), and effective gate length L_{eff} (y) can be locally determined. In addition, we can see from the results in Figure 4 (b) that there is a correlation between gate LER and X_{ov}. Moreover, the SDE-edge fluctuation increases or decreases according to this correlation. Thus, if we suppress dopant diffusion in order to operate a transistor with a relatively short L_g, the SDE lateral edge will fluctuate, reflecting the gate LER, and L_{eff} fluctuation will increase. We also confirmed that if L_{eff} fluctuation increases as predicted from STM measurements, V_{th} (threshold voltage) fluctuation



(a) 2D carrier profile in active-region surface under gate

(b) Relationship between X_{ov} in extension under gate and gate LER

Figure 4
Relationship between gate LER and carrier profile around extension region.

will likewise increase.

4.3 Improved transistor fabrication

From the above discussion, we can expect performance variability, which hinders the normal operation of circuits, to become a serious problem when we scale down transistors to raise LSI performance and integration. By utilizing the STM measurement results, we developed transistor fabrication methods that reduce dopant profile fluctuation. For example, we developed an amorphous gate as a fabrication method for improving dopant profile fluctuation.[12] We also devised an ion implantation method for forming the SDE regions and showed that it could reduce a scaled transistor's L_{eff} fluctuation by 15% and V_{th} fluctuation by 15%.[13] Techniques like these for reducing transistor performance variability are one of the most important ways to make possible advanced devices of the 40-nm process generation and beyond, and 2D carrier profiling has played an important role in their development.

5. Fault analysis

2D carrier profiling of active-region surfaces can also be used to evaluate the dopant profile of the active region modulated near the shallow trench isolation region. For example, we have clarified that X_{ov} gradually decreases at points closer to the shallow trench isolation region.[14] It is also possible to apply 2D carrier profiling to active-region surfaces of narrow-channel MOSFETs typical of static random access memory (SRAM), and we have shown that the dopant profile of scaled transistors in SRAM can significantly change from the ideal state through the effects of gate LER and shallow trench isolation.[14] These results suggest that an STM system with auxiliary equipment for identifying the probe position could be used to analyze SRAM defect locations.

6. Conclusion

This paper described STM-based 2D carrier profiling and presented examples of its application to semiconductor device development. This technique, which enables 2D dopant profiles to be actually observed, has contributed to the efficient development of advanced semiconductor devices. Looking forward, we foresee new application methods that exploit the advantages of STM as a surface-sensitive measurement technology

(having high 2D resolution on the measurement surface) as in the evaluation of dopant profile fluctuation, and we envision combinations of STM with other measurement technologies and technology computer aided design (TCAD).

References

1) G. Binnig et al.: Surface Studies by Scanning Tunneling Microscopy. *Phys. Rev. Lett*., Vol. 49, Issue 1, pp. 57–61(1982).
2) M. B. Johnson et al.: Scanning tunneling microscopy and spectroscopy for studying cross-sectioned Si (100). *J. Vac. Sci. Technol*., B, Vol. 10, Issue 1, pp. 508–514 (1992).
3) H. Fukutome et al.: Two-dimensional characterization of carrier concentration in metal-oxide-semiconductor field-effect transistors with the use of scanning tunneling microscopy. *J. Vac. Sci. Technol*., B, Vol. 22, Issue 1, pp. 358–363 (2004).
4) H. Fukutome et al.: Direct Evaluation of Gate Line Edge Roughness Impact on Extension Profiles in Sub-50-nm n-MOSFETs. *IEEE Transactions on Electron Devices*, Vol. 53, No. 11, pp. 2755–2763 (2006).
5) R. J. Hamers et al.: Surface Electronic Structure of Si(111)-(7×7) Resolved in Real Space. *Phys. Rev. Lett*., Vol. 56, Issue 18, pp. 1972–1975 (1986).
6) Y. Morita et al.: Ideal hydrogen termination of Si (001) surface by wet-chemical preparation. *Appl. Phys. Lett*., Vol. 67, Issue 18, pp. 2654–2656 (1995).
7) H. Fukutome et al.: Gate insulating layer impact on the extension profile of the sub-50 nm p-MOSFET. Ext. Abstr. International Workshop on Junction Technology 2002, 2002, pp. 43–46.
8) H. Fukutome et al.: Fluorine Implantation Impact in Extension Region on the Electrical Performance of Sub-50 nm p-MOSFETs. International Electron Devices Meeting Tech. Digs., 2003, pp. 485–488.
9) H. Fukutome et al.: Direct Measurement of Offset Spacer Effect on Carrier Profiles in Sub-50 nm p-Metal Oxide Semiconductor Field-Effect Transistors. *J. Jpn. Appl*. Phys, Vol. 45, No. 4B, pp. 3133–3136 (2006).
10) H. Fukutome et al.: Anomalous diffusion in the extension region of nanoscale MOSFETs. International Electron Devices Meeting Tech. Digs., 2001, pp. 67–70.
11) A. Asenov et al.: Intrinsic Parameter Fluctuations in Decananometer MOSFETs Introduced by Gate Line Edge Roughness. *IEEE Transactions on Electron Devices*, Vol. 50, No. 5, pp. 1254–1260 (2003).
12) H. Fukutome et al.: Suppression of Poly-Gate-induced Fluctuation in Carrier Profiles of Sub-50 nm MOSFETs. International Electron Devices Meeting Tech. Digs., 2006, pp. 281–284.
13) H. Fukutome et al.: Comprehensive Design Methodology of Dopant Profile to Suppress Gate-LER-induced Threshold Voltage Variability in 20 nm NMOSFETs. Tech. Digs. of Symposia on VLSI technology, 2009, pp. 146–147.
14) H. Fukutome et al.: Direct Measurement of Effects of Shallow-Trench Isolation on Carrier Profiles in Sub-50 nm N-MOSFETs. Tech. Digs. of Symposia on VLSI Technology, 2005, pp. 140–141.

Hidenobu Fukutome
Fujitsu Semiconductor Ltd.

Dr. Fukutome received B.S., M.S., and Ph.D. degrees in Solid State Physics from Osaka University, Osaka, Japan in 1994, 1996, and 1999, respectively. In 1999, he joined Fujitsu Laboratories Ltd., Atsugi, Japan, where he has been engaged in research and development of a two-dimensional carrier profiling technique and development of the 90-, 65-, 45-, and 32-nm-node CMOS devices using this technique. He moved to Fujitsu Semiconductor Ltd. in 2008. He was a visiting researcher at ETH Zurich (Swiss Federal Institute of Technology) in 2007. He received the Young Scientists Prize from the Ministry of Education, Culture, Sports, Science and Technology in 2008. He left Fujitsu Semiconductor Ltd. in April 2010.