Multilevel Interconnect Technology for 45-nm Node CMOS LSIs

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We have developed a novel porous low-k material called nano-clustering silica (NCS) which has a low dielectric constant (k = 2.25) and high mechanical strength (Young's modulus E = 10 GPa), and established manufacturing technology for 45-nm node multilevel Cu/Full-NCS interconnects which use NCS in trench layers and via layers to reduce the resistance-capacitance (RC) delay. Our Cu/Full-NCS interconnects are reliable enough to prevent damage to Cu interconnects by the mechanical stress that occurs in wire bonding, packaging, and other processes. This paper describes the characteristics of NCS and problems due to applying porous low-k material in multilevel interconnects. In addition, the performances and reliability of 45-nm node CMOS LSIs which use NCS are also explained.

1. Introduction

LSI speed has been accelerated by reducing the size of LSIs based on Moore's Law (scaling rule). In high-performance LSIs, such as microprocessor units (MPUs) which are applied in high-end servers and primary devices of mobile equipment, their size has been reduced to the nano-technology level with a design rule of a 45-nm node.

The relationship between LSI size and actuation speed (delay time) is shown in **Figure 1**. By reducing the size of LSIs, the delay time of transistors will decrease, indicating that CMOS node shrinkage directly contributes to transistor acceleration. On the other hand, reducing the size of interconnects will increase the delay time. This is explained by the fact that, the effect of electric charge accumulating in the condenser structure (parasitic capacity) between adjacent interconnects grows beyond the negligible level. Namely, the time required for charging and discharging an electric charge on the parasitic capacity between interconnects will increase the delay in signal transmission. Particularly, when the minimum interconnect distance is shorter than 100 nm, an increase in the RC delay due to this parasitic capacity offsets the transistor acceleration, resulting in a drop in LSI actuation speed.[1)-3)] In this case, the capacity between interconnects is proportional to the permittivity of the insulation film. Permittivity represents a physical quantity that indicates the level of electric charge deviation (dielectric polarization) in molecules or atoms in an electric field. In this paper, it is expressed as a relative value versus permittivity in a vacuum (dielectric constant). To decrease parasitic capacity, it is essential to decrease dielectric constant.

In the midst of an increasing trend for smaller size, the permittivity-related requirements requested for each design rule are described in the International Technology Roadmap for Semiconductors (ITRS) issued by the International Roadmap Committee. The trend of decreasing dielectric constant (Low-k) in the ITRS issued from 1999 to 2006 is shown

in **Figure 2**. This figure indicates the low dielectric constant of insulation film necessary to maintain an interconnect delay at a certain level based on the interconnect structures listed in the roadmaps. When the dielectric constant is lower than 2.5, the insulation film is susceptible to damage caused by mechanical stress with the reduction of dielectric constant. Because this configuration is susceptible to film damage during the interconnecting process, there is a significant hurdle to be overcome for commercialization. Because of this, the dielectric constant is reviewed in each roadmap revision, prolonging the time after a dielectric constant smaller than 2.5 is required.

The insulation film used for interconnects requires high mechanical strength in addition to sufficient insulation performance. Because a high level of stress is applied on the fine interconnect structure during the wafer flattening and wire bonding processes, insulation films must have a good mechanical strength. However, lowering the dielectric constant of the insulation film leads to degraded mechanical strength. Because of this, it is extremely difficult to form fine interconnects by using low-k insulation films.

Fujitsu has developed a novel porous low-k material called nano-clustering silica (NCS) which has a low dielectric constant (k = 2.25) and high mechanical strength (Young's Modulus E = 10 GPa) and applied this material to CMOS LSI interconnects after 65-nm node.

In this report, the challenges in producing low-k insulation film (hereafter "Low-k film") and the characteristics of NCS are explained first. Then, challenges for developing LSI multilevel interconnect manufacturing technology are described. Finally, the performances and reliability of 45-nm node CMOS LSI interconnects which use NCS are discussed.

2. Challenges in producing Low-k film

To produce a Low-k film with a dielectric constant smaller than 2.5, it is necessary to form pores (dielectric constant = 1) inside the insulation film. In the initial stage of development, many institutes reported research on a template type of porous insulation film. In this method, the template material is dispersed inside the insulation film in advance and the template is decomposed and removed to generate the pores after the film is formed. Based on this template approach, it is possible to produce material with a dielectric constant even smaller than 2.5 by increasing the pore percentage. However, Low-k films made in this way have a weak mechanical strength and there is the fatal problem that they are susceptible to having degraded insulation film characteristics. This problem is caused by

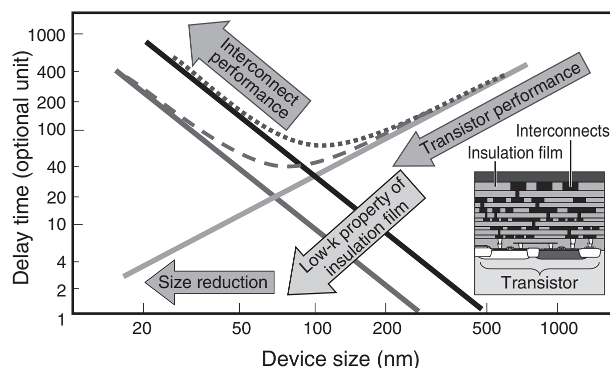

Figure 1
Relationship between LSI size and delay time.

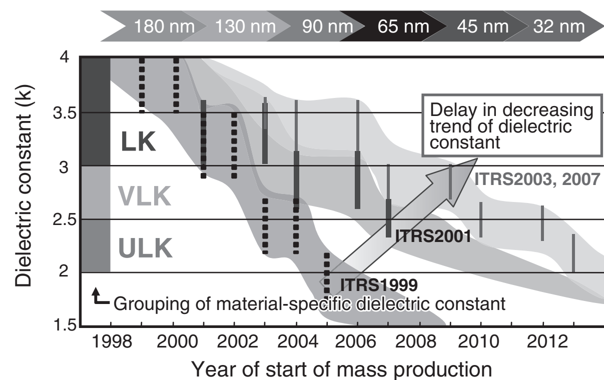

Figure 2
Trend of decreasing dielectric constant.

chemicals penetrating into the pores during the formation of the interconnect structure. The main factors behind the poor mechanical strength and penetration of chemicals are attributable to the pore generation process associated with the decomposition and evaporation of the template. In this method, channels of the gas generated during the process of template decomposition may become tunnel-like pores with a length longer than 20 nm (huge connected pores) or open pores, and this makes it difficult to control the core geometry, size and distribution.

3. Development concept and characteristics of NCS

In this section the pore formation technology and characteristics of NCS are explained in comparison with the conventional template-type porous insulation film.

In the development of NCS, a Low-k characteristic was achieved using the material design and concept shown below so as to address the issues associated with template-type porous materials (**Figure 3**).

1) To prevent generation of huge connected pores and open pores, nano-clusters with a basket-like molecular structure are formed, in which pores are generated in advance. The nano-clusters are dispersed in a medium and films are formed by applying this medium in a rotating manner.
2) Because the nano-clusters also include a potent catalyst to cause a chemical reaction, nano-clusters bond securely to each other upon being heated after the film formation process.

Different from the conventional template approach, this technology allows the formation of pores without involving elements that are decomposed and evaporated by heating. Therefore, NCS has a number of excellent characteristics as shown below.

1) Pore size

Because NCS enables a structure with a uniform dispersion of nano-pores, no huge connected pores are observed, unlike in the template-type porous insulation films to which pores with a dielectric constant of 2.25 are

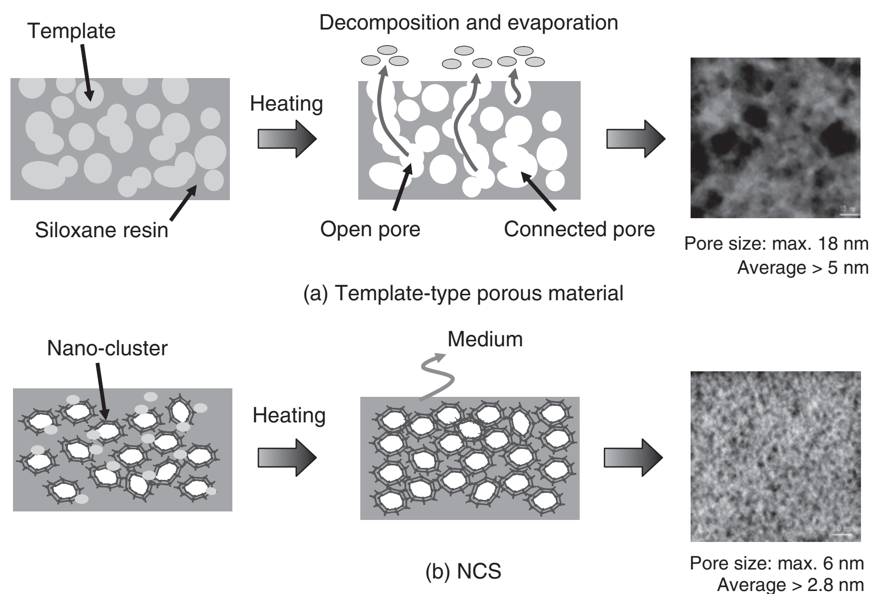

Figure 3
Challenges of template-type porous materials and material design concept of NCS.

introduced. The pore size obtained by the NCS approach is 2.8 nm on average based on the small angle X-ray scattering method, indicating that the pore size could be reduced to about one-fourth versus the pore size in the template-type porous insulation film (11.2 nm).

2) Mechanical strength

With conventional template-type porous insulation films, it is difficult to achieve both high mechanical strength and Low-k features at the same time, because the mechanical strength drops significantly with the decrease of dielectric constant (namely, with the increase of pore percentage). This is due to the fact that the generation of huge connected pores leads to a degradation of mechanical strength, as already mentioned.

With NCS, on the other hand, a Young's modulus of 10 GPa was achieved for a dielectric constant of 2.25, which is smaller than the FY2003 ITRS requirement for 45-nm CMOS LSI interconnects and the following generations. It represents a mechanical strength more than twice that of template-type porous insulation film (4.8 GPa). This result was achieved through reducing the pore size by using nano-clusters and having a secure chemical bonding through a potent catalyst.

3) Insulation performance

NCS indicates an insulation performance in the order of four digits higher than that of the template-type porous insulation film, where the leakage current is 4.6×10^{-11} A/cm^2 in a surge field of 0.2 MV/cm, a sufficient insulation performance as a CMOS LSI multilevel interconnect material.

4. Cu/NCS multilevel interconnect manufacturing technology

In this section, challenges in applying Low-k films to multilevel interconnects and 45-nm multilevel interconnect manufacturing technology which uses NCS are described.

The multilevel interconnect manufacturing process is shown in **Figure 4**. In this figure, the interconnect manufacturing process for the first

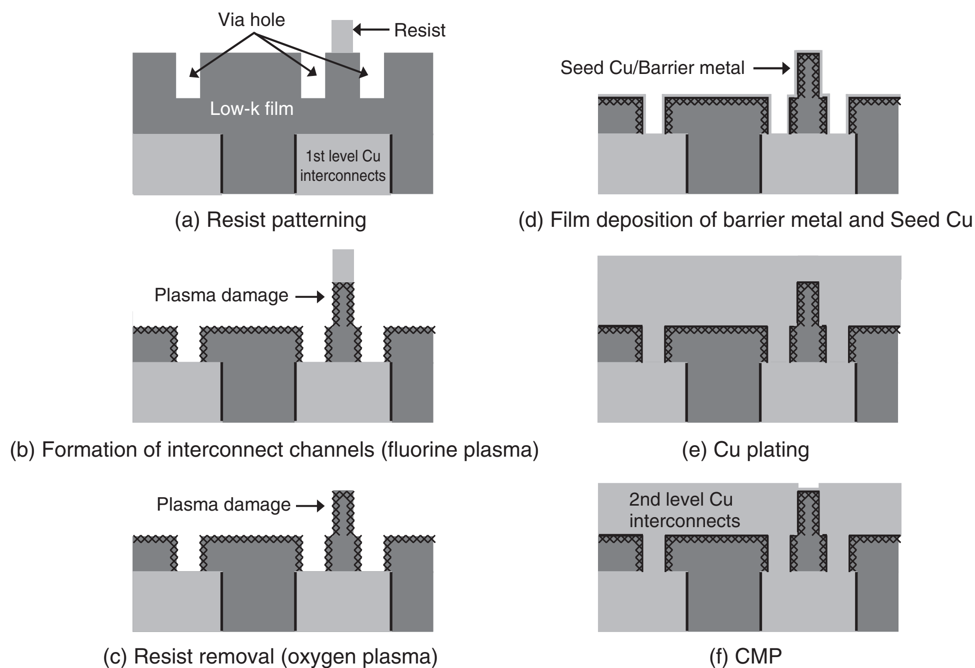

Figure 4
Manufacturing process of multilevel interconnects.

layer and via hole forming process to establish connection with the first layer are omitted, because the purpose of the figure is to explain the challenges of the multilevel interconnect manufacturing process.

The first step is to pattern the resist to make interconnect channels on the substrate on which via holes are formed. [Figure 4 (a)]. Then, using this resist pattern as masking, a Low-k film is etched using fluorine plasma and interconnect channels are processed to form interconnects [Figure 4 (b)]. In the next step, resist patterns are removed by using oxygen plasma [Figure 4 (c)], and then a film is made while using a spattering barrier metal to prevent copper from intruding into the Low-k film and Seed Cu, which is an essential factor as an electrode for copper plating [Figure 4 (d)]. Further, copper is stuffed into the interconnect channels by plating [Figure 4 (e)]. Finally, surplus copper is removed by polishing by chemical mechanical polishing (CMP) to separate the connects [Figure 4 (f)].

In the general multilevel interconnect manufacturing process as mentioned above, two types of damage are observed when applying a Low-k film. The first problem is that the film is destroyed during the CMP process due to its fragility, as mentioned before. The second major problem is the degradation of the film characteristics due to damage caused by the plasma during the dry etching process.

We will now describe this dry etching process in more detail at a molecular level. Siloxane bonding as a framework of the Low-k film is removed by decomposition and gasification with ions and radials that are generated when fluorine and oxygen turn into plasma. In this process, chemical damage occurs to the Low-k film to make it easier for the film to absorb atmospheric humidity. Because the dielectric constant of water is very high (80), the permittivity will elevate beyond the required value if the Low-k film absorbs even a tiny amount of water. In addition, the absorption of water will cause a current leakage inside the Low-k film, and lead to a serious drop in insulation performance. Therefore, to use a Low-k film for multilevel interconnects, the etching conditions need to be optimized and the plasma-related damage on the Low-k film should be reduced.

Fujitsu has attempted to optimize the etching conditions to control plasma-related damage during the etching process, when NCS is used as an inter-layer insulation film for CMOS LSI multilevel interconnects. To achieve this, the relationship between the film characteristics and various other parameters, such as the type of gas used for plasma generation, the pressure of the etching chamber, the gas flow rate, the composition of the gas mixture and the power conditions in plasma generation were studied in detail. To be specific, regarding the gas mixture of CF_4 and oxygen used for etching, the amount of oxygen was reduced as much as possible to minimize the chemical damage to the Low-k film. To raise the plasma power and complete the etching process in the shortest time, the duration of the film's exposure to the plasma was minimized.

As a consequence, the elevation of the dielectric constant due to plasma-related damage during the NCS etching was suppressed to within 0.1. Also, the elevation of the leakage current due to plasma-related damage could be drastically reduced.[4)]

5. Performances of Cu/NCS multilevel interconnects

In this section, the interconnect performances of Cu/NCS multilevel interconnects are described when they are used as 45-nm node CMOS LSI multilevel interconnects.

5.1 Multilevel interconnect structure

As mentioned before, the parasitic capacity generated among the interconnects will change depending on the permittivity of the insulation film that encloses those interconnects. Fujitsu

has applied NCS to 65-nm CMOS LSIs and commercialized the resultant products. With a 65-nm CMOS LSI, a hybrid structure was employed where NCS was used for only those interconnects that were on the same level. This structure was employed because using NCS on the same level was sufficient to obtain the targeted device performance. However, a circuit simulation of its application in 45-nm nodes revealed that the distance between the interconnects was reduced by 70%, which leads to a greater parasitic capacity in relation to the distance between interconnects, the volume of the insulation film, and the prolongation of the RC delay. Therefore, in applying NCS to 45-nm node CMOS LSI multilevel interconnects, Full-NCS structure was employed, where the range of introducing the NCS was extended to the via layer.

As a result, 45-nm node CMOS LSI multilevel interconnects were established by introducing the aforementioned NCS material and LSI multilevel interconnect technology. **Figure 5** shows a cross section of the LSI multilevel interconnects that we developed, as taken by a transmission electron microscope (TEM).

The CMOS LSI multilevel interconnects are comprised of three interconnect levels: a lower level for which the minimum interconnect distance is applied for inter-device signal transmission, a middle level, and an upper level for extracting signals to the outside. NCS is introduced to the lower interconnect level (Line/Space = 65 nm/65 nm) where the effect of parasitic capacity on delay is most significant.

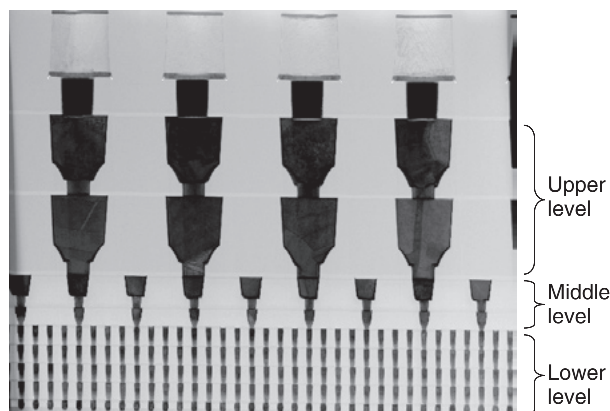

Figure 5
45-nm node multilevel Cu/Full-NCS interconnects.

5.2 Interconnect leakage current

When an electric field of 0.7 MV/cm is applied to the lower level interconnects of Line/Space = 65 nm/65 nm, the leakage current is 1×10^{-12}A, demonstrating a sufficient level of insulation performance. This performance is possible thanks to the NCS material, characterized by a uniform dispersion of fine pores, as well as the optimization of conditions for NCS dry etching, as previously mentioned.

5.3 Parasitic capacity

When comparing the total amount of parasitic capacity among interconnects and between different levels in Full-NCS structure with those of multilevel interconnects in a hybrid structure to demonstrate the significance of the development of Full-NCS structure, we confirmed that the parasitic capacity could be reduced by 20% in Full-NCS structure versus the parasitic capacity in the hybrid structure.

5.4 Interconnect performance

The RC delay in the Full-NCS structure in the current innovation was compared with the RC delay in a general insulation film based on FY2006 ITRS, and those delays in a hybrid structure. The comparison results are shown in **Figure 6**.

Compared with the general RC delay of 682 ps/mm with the 45-nm node stipulated by ITRS, the hybrid structure increases the delay up to 729 ps/mm. On the other hand, when using the 45-nm node Full-NCS structure developed by Fujitsu, the delay could be reduced to 584 ps/mm. We demonstrated that performance was successfully improved by 14% versus the

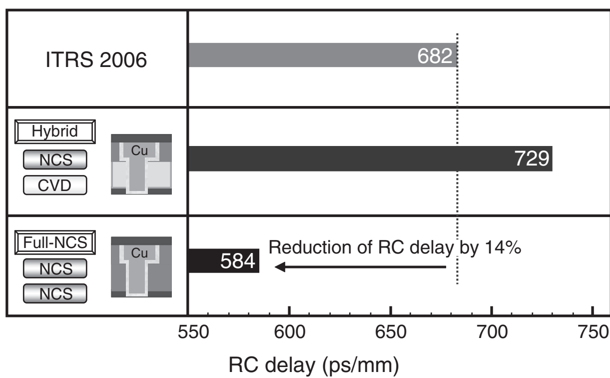

Figure 6
Comparison of RC delay.

interconnect performance stipulated by ITRS.[5)]

6. Reliability of Cu/NCS multilevel interconnects

In this section, the reliability of CMOS LSI multilevel interconnects is described, as it is one of the most important points for commercialization.

6.1 Stress migration

An LSI generates heat of about 100°C at the most at actuation. This heat generation will cause stress inside the LSI multilevel interconnects due to a difference in heat expansion among the various component materials. Failures such as disconnection of interconnects caused by this stress are called “stress migration”.

When using Low-k film for Cu interconnects, a degradation of the resistance to stress migration has been reported frequently.[6)-8)] This phenomenon may be attributable to the mechanism where humidity absorbed by the Low-k film surface causes oxidation of the barrier metal under the impact of plasma-related damage during the etching process. This could lead to changes in the adhesive performance and stress property at the interface of the Cu or Low-k film. However, because a residue of fluorine contamination which is generated in the etching process adheres to the etched surface of the Low-k film in addition to the above-mentioned humidity, it is essential to examine the influence of this residual fluorine contamination when analyzing the oxidization mechanism of barrier metals. Therefore, we analyzed the mechanism of barrier metal oxidization at the barrier metal-NCS interface. The analysis results revealed that the fluorine contamination reacts with the water inside the NCS and generates hydrogen fluoride (HF). HF works as a catalyst to promote oxidization of the barrier metal.[9)] Based on these analysis results, we developed a treatment process to remove the residue of fluoride contamination during the interconnect formation and verified that there was no disconnection associated with stress migration in an acceleration test of 1008 hours at 200°C. Thus, excellent resistance to stress migration of Cu/Full-NCS multilevel interconnects was demonstrated.

6.2 Wire bonding test result

Wire bonding was conducted on the Cu/Full-NCS multilevel interconnects. Even though a tensile force was applied to the wire in the tension test, the only destruction mode observed was a wire disconnection. No disconnection or destruction of the interconnects or inside vias was observed. This result demonstrated the high mechanical strength of NCS and its high adhesion performance between different levels.

7. Conclusion

In this paper, NCS, a novel porous Low-k material that enables a reduction in the value of interconnect capacity used for 45-nm node CMOS LSI multilevel interconnect technology, was reported. In addition, 45-nm node CMOS LSI multilevel interconnect technology and its performance and reliability were described. NCS has successfully overcome the challenges of a template-type porous insulation film by adopting a unique material design called “nano-cluster”, demonstrating an excellent reduction of dielectric constant and superb mechanical strength as a pioneered approach in the global arena. Also,

45-nm node CMOS LSI multilevel interconnects with a Full-NCS structure demonstrated an excellent ability to drastically suppress the RC delay compared with the general insulation film stipulated in FY2006 ITRS. The reliability of these interconnects has been verified after establishing a manufacturing process in the mass production line at Fujitsu Micro-Electronics. The first shipment of these products started in 2008.

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