Wide-Range Low-Noise Fast-Hopping Fractional-ΣΔ Synthesizer in 1.2-V 90-nm CMOS

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A 90-nm CMOS wide-band low-noise fast-hopping synthesizer for 1.2-V supply and integration into a WiMAX front-end is described. The synthesizer's voltage controlled oscillator (VCO) is designed for a wide spread of process parameters and a guaranteed frequency range from 2.766 to 3.253 GHz. This target performance is achieved by using a highly sophisticated digital control unit, invoking fast automatic calibration of up to 24 fixed frequencies after power-on, and featuring fast digital calibration correction of approximately 20 µs upon a frequency change. A further feature that allows stable operation in widely varying environmental conditions (e.g., a temperature change of 140°C) is a second control loop of the phase-locked loop, using the frequency correction signal to a second VCO control input. An improved digital algorithm for fast frequency tracking is used, and this speeds up the digital tracking decision by a factor of 13 or more. In the final phase of the locking procedure, the same algorithm delivers multilevel phase measurement, enabling faster locking and improved (in terms of noise, linearity, and reference leakage) phase detection.

1. Introduction

The performance of today's front-end architectures for wireless communication depends to an increasing degree on the performance of the synthesizer. This is because new wireless communication standards that aim for high data efficiency, like IEEE 802.16e (Mobile WiMAX), set tight requirements on the purity and agility of the carrier generation. At the same time, increased market pressure for highly integrated solutions with growing digital complexity is moving the target technologies for such front-ends below 100 nm, which adds additional limitations to the analog design approach for synthesizer integration. As a result, it is a challenging task to implement competitive high-performance analog blocks in a technology optimized for high-density digital design, including the following demands:

- a large (487 MHz) required voltage controlled oscillator (VCO) range at a frequency (3 GHz) where parasitic effects significantly reduce the usable control range;
- a 1.2-V power supply voltage, which limits the usable VCO control range to 300 mV (when considering saturation margins), which is in conflict with the requirement for low VCO gain and extended frequency control range; and
- the need for low power consumption, which dictates higher power-related impedances (such as VCO tank impedance and loop filter impedance), but which conflicts with the requirement for lower impedance to give low noise (–95 dBc @ 100-kHz offset).

An initial synthesizer architecture using five sub-ranges, with 100-MHz bandwidth per sub-range, was evaluated. However, simulations showed that with the 480-MHz frequency drift

over process and temperature variations, only a limited frequency control range of 35 MHz could be obtained. Therefore, calibration would have been needed to meet the required performance. And since non-volatile memory was not available, autonomous calibration would have been necessary. Because the simulated maximum temperature drift was about 30 MHz (approaching the available control range), the compensation of process and temperature deviations became of critical importance, and the classical synthesizer concept needed to be completely revised.

To solve these problems, firstly the VCO was built with its frequency control range set by an 8-bit capacitor matrix. This enabled the compensation of process deviations and the achievement of the target frequency range. For the optimum area and to minimize parasitic capacitances, 8-bit control was implemented using two 4-bit binary weighted matrices (a coarse matrix and a fine matrix).

Without the possibility of using non-volatile memory or external calibration data, a lookup-table must be calculated automatically in a very limited time slot after power-on. However, calibration of all 256 sub-ranges would require huge digital complexity and greatly exceed the available time. Therefore, a subset of calibration frequencies was chosen, which includes all integer reference frequency multiples within the specified frequency range. This gave manageable complexity of the calibration control unit at the cost of a maximum possible frequency calibration error of Fref/2 (reference frequency) in fractional mode while the number of calibration steps was limited to at most 24.

In addition to this, a maximum of 30 MHz for a further frequency offset due to drift over the specified temperature range needed to be considered. To deal with this, a recalibration of the capacitor matrix is implemented in the initial phase of every frequency change to reduce the possible error. The recalibration applies to the fine capacitor matrix and allows the synthesizer to approach within about 0.1% of the target frequency in the initial phase of the hopping procedure. This capability of fast dynamic recalibration to compensate for the initial error and frequency drift caused by temperature is considered to be a unique feature of our calibration system.

However, even this solution cannot cover all possible operating requirements — the synthesizer must also allow continuous operation for hours without any hopping, which implies a maximum possible temperature drift without even partial recalibration because of the resulting unacceptable carrier disturbance.

The fact that temperature changes are much slower than the anticipated response of the phase locked loop (PLL) suggested a solution to this problem as well — a second analog control loop was implemented in the synthesizer to track any slow changes such as those caused by temperature.

Implementing all of the above techniques made the developed VCO into a complex circuit with various new functions.

2. VCO

The VCO consists of four main analog blocks, as shown in **Figure 1**. Because their complex functionality requires sophisticated digital logic, interfaces were implemented to allow the blocks to be controlled by state machines in a central digital unit.

2.1 VCO core

The noise performance of the VCO is mainly defined by its core circuit. Until recently, bipolar devices have been assumed to be superior in terms of flicker noise, but the latest design techniques have been developed to compensate for the up-conversion of flicker noise in pure CMOS technologies[1)-4)] A low noise design is achieved firstly by using low-noise components and secondly by designing them to avoid frequency conversion to the output target frequency.

Therefore, the VCO core consists of PMOS cross-coupled transistors and a low-flicker-noise programmable resistive current source.

The differentially driven LC-tank comprises a center tapped 3-metal inductor, varactors, and the 2 × 4 bit matrixes of switchable capacitances for digitally controlled tuning.

Using NMOS-switches to short or open the differentially placed high-Q metal-insulator-metal (MIM) capacitors between both oscillating nodes was found to be the most effective way to balance the digital frequency trimming.

Because the wide tuning range capability gives rise to a corresponding variation of the tank circuit impedance, a fast oscillation startup might be not guaranteed for the worst process conditions and lowest frequency settings. To avoid this risk, the VCO is always started at its highest frequency, and an amplitude level control circuit then calibrates the output signal level.

2.2 VCO amplitude control

An amplitude level detection circuit was implemented. This circuit and a counter-based state machine (located inside the digital block) form an output voltage magnitude control loop. The level detection consists of a rectifier plus low-pass filter and a hysteresis-comparator, which outputs a logic level corresponding to the comparison result of the VCO output magnitude and a preset (desired) amplitude value. Since it is sampled digitally within several subsequent steps, this output applies negative feedback to the amplitude settings so that after seven itera-

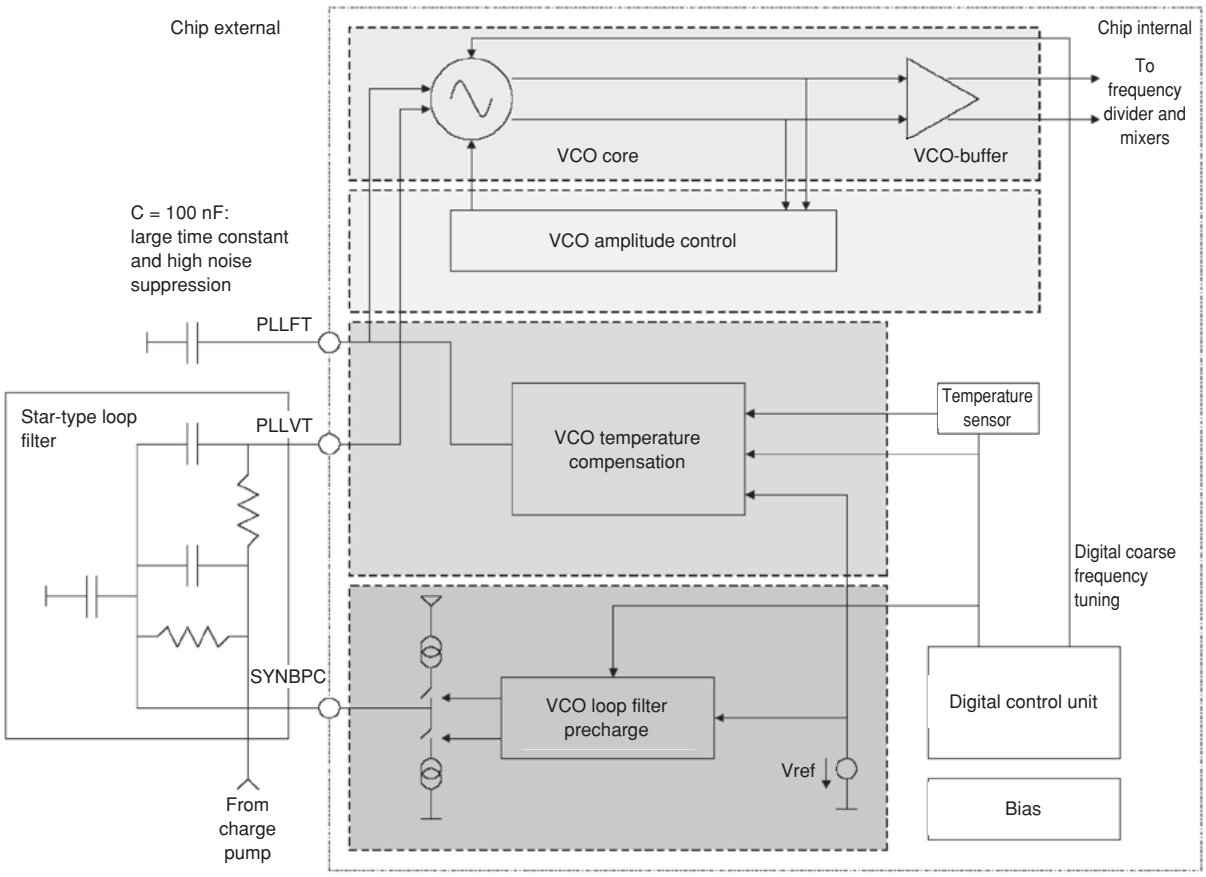


Figure 1
Block diagram of VCO.

tive steps the amplitude level is guaranteed to settle close to the predefined value.

The proper amplitude level control settings are calibrated for every (integer) frequency value to track the impedance change of the LC-tank, and they are restored after frequency reprogramming.

2.3 VCO temperature compensation

In contrast to conventional VCOs, the circuit implemented in the present development includes a second varicap, forming an additional analog tuning input used for temperature compensation. During the calibration phase, the newly developed temperature compensation circuit pre-charges an external capacitor to a voltage corresponding to the absolute temperature during initialization.

The initial temperature information is derived from an on-chip digital temperature sensing circuit. A reference voltage depending on the temperature information is fed to an external capacitor to pre-charge a reproducible starting value corresponding to the junction temperature.

After the operation of the synthesizer has started, its main control voltage is monitored continuously by a low-output-current operational transconductance amplifier, which compares the predefined mid-voltage (0.55 V in this case) with the actual control voltage.

Any changes, which cause a drift of this voltage (assumed to be mainly frequency changes due to temperature drift), cause a small corresponding current to flow into the external capacitor. The resulting voltage change on the second VCO input (solid curve in **Figure 2**) is completed when the output of the operational transconductance amplifier comes back into balance, which is the case when the main synthesizer control voltage (dotted curve in Figure 2)

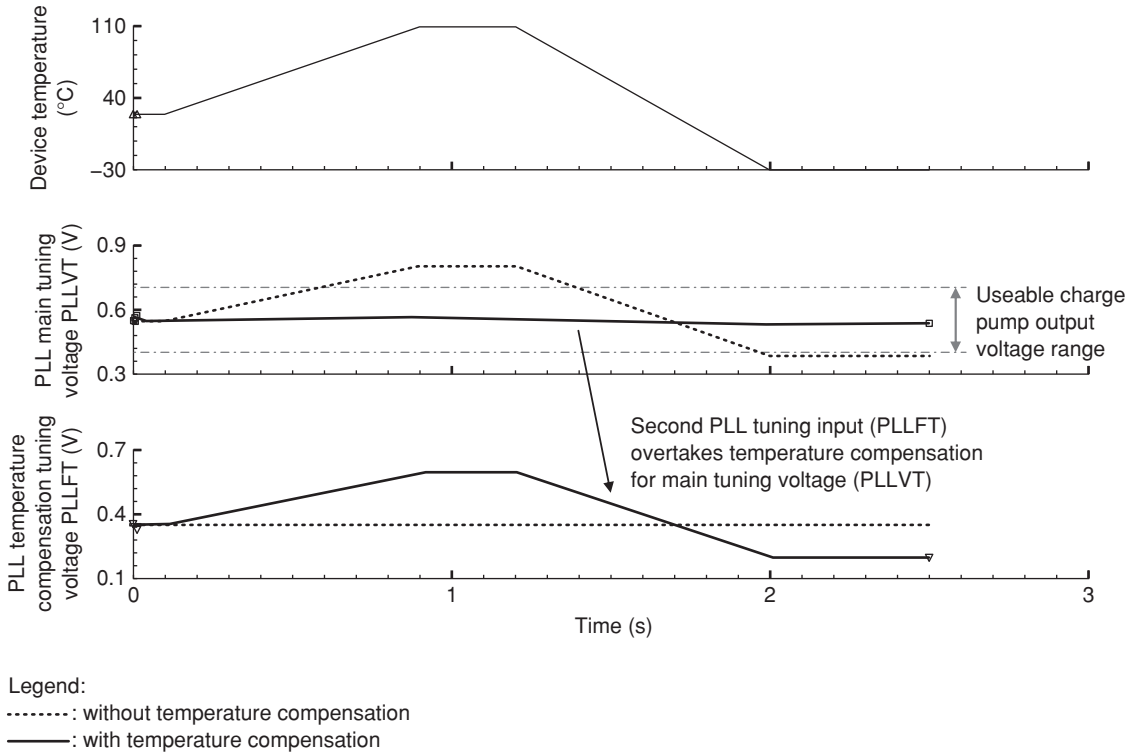


Figure 2
Simulated behavior of PLL temperature compensation loop.

reaches 0.55 V.

The additional VCO input used for this function is also a noise contributor. The wider voltage control range increases the risk of excessive noise generation because of the greater steepness of the varicaps at low voltages, which converts low-frequency voltage noise into carrier phase noise.

A suitable compromise was found by using a high capacitance value (100 nF), which forms a low impedance even at frequencies below 10 kHz, reducing noise voltage generation via the temperature compensation input.

The second analog control loop is then formed by the operational transconductance amplifier, the external 100-nF capacitor and the second VCO control input. This could cause instability due to interaction between the two analog control loops.

The large 100-nF blocking capacitor results in very low bandwidth of the second control loop, which prevents interaction between the two loops.

2.4 VCO loop filter precharge

Since this synthesizer is a sophisticated system with analog and digital frequency control, its behavior during calibration and recalibration (in the initial state of the hopping phase) is determined by a virtual third digital control loop (this is a feedback loop formed by the digital control function).

To ensure system stability, at least the fast analog loop must be opened during digital recalibration. This is done by forcing a predefined voltage (0.55 V) onto the loop filter capacitors so that after the forcing circuit has been released the analog control loop will start at the middle of the varicap control range. Of course, the time needed to pre-charge the capacitors becomes part of the hopping time, which reduces the hopping speed. To minimize the impact of this as much as possible, the voltage forcing circuit must be designed with high drivability, but minimal influences such as leakage current and substrate noise coupling while inactive.

To satisfy this requirement, the fourth part of the VCO-block is a combination of a fast comparator and a high-current up/down switchable source intended to precharge the loop filter main capacitor with the 0.55-V reference voltage for less than 7 µs.

3. Digital control unit and synthesizer architecture

Much of the functionality of our synthesizer concept lies in the digitally synthesized block, which allows the implementation of sophisticated high-speed algorithms for fast locking and phase noise improvement.

A simplified functional block diagram of the synthesizer architecture is shown in **Figure 3**. The only obvious difference from the classical ∑Δ (sigma-delta) synthesizer circuit is the divider chain main divider (MDiv) + integer divider (IDiv), which are both controlled by the serial peripheral interface instead of a single multi-modulus divider stage being used. A more detailed view of the synthesizer architecture with emphasis on the analog units is shown in **Figure 4**.

The MDiv is a dual modulus divider

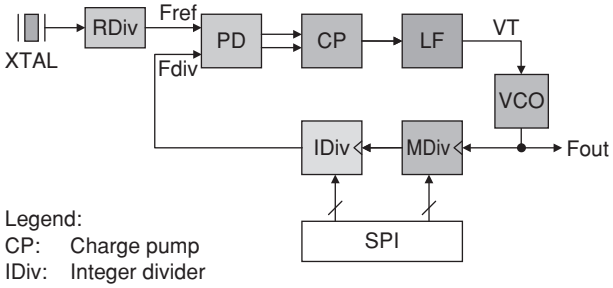


Figure 3
Simplified functional block diagram of the PLL synthesizer.

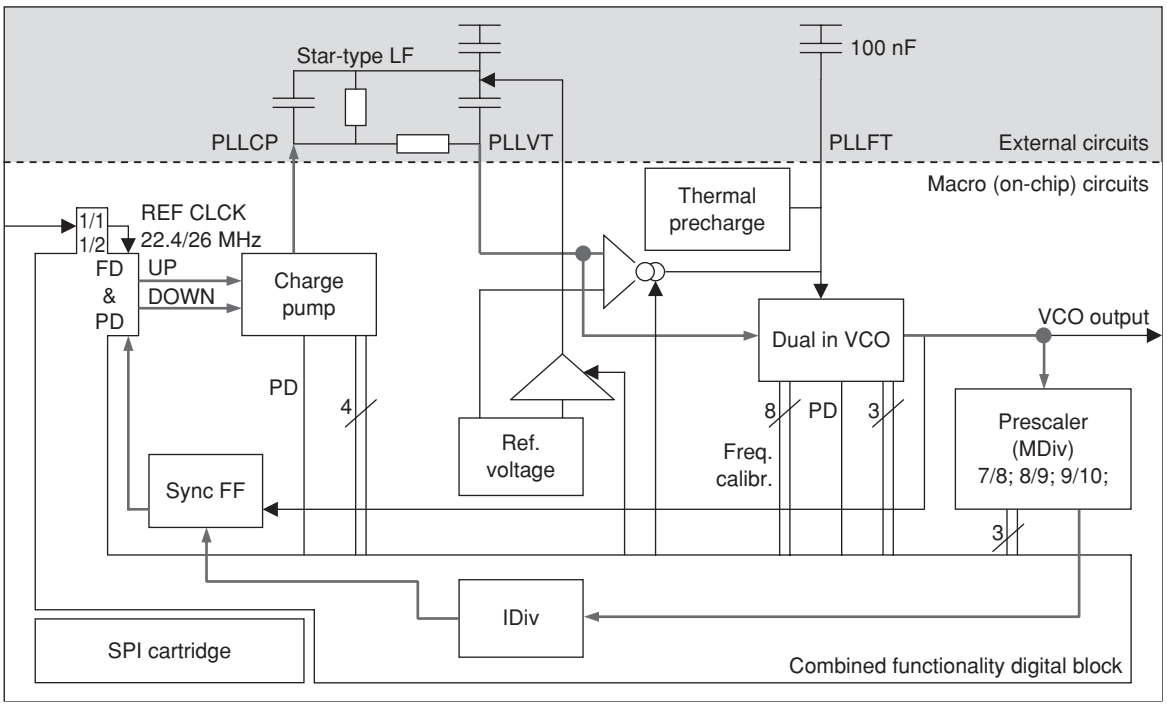
(prescaler), which can be programmed for three sets of dual modulus division ratios. The selected frequency generation scheme is decoded into one of the above three sets of division ratios and rounded out by the matching division ratio of the IDiv (13, 14, 15, or 16). The control within the selected set ($n/n + 1$) is done by a third-order sigma delta pseudorandom generator, where the 7-level output is mapped into the first of seven subsequent $n/n + 1$ cycles, counted by the IDiv.

This architecture has the advantage of using a small subset of fast division ratios (total of 4), while matching the higher dynamic range of the third-order sigma delta (7 levels) and achieving, together with the programmable IDiv, a continuous range of total division ratios from 95 to 154. This is required to cope with the frequency range from 2.766 to 3.253 GHz including a choice of reference frequencies between 22.4 and 26.0 MHz. Six additional cycles are needed to guarantee a continuous divider ratio range. This results in a total minimum IDiv ratio of 13, which is a limitation on the flexibility of the concept presented here.

The digital control unit also includes the state machines for the described control functions (e.g., VCO amplitude control, loop filter precharge, and frequency calibration and recalibration).

3.1 Digital frequency calibration and recalibration

As described in Section 2.1, as a result of a digitally controlled VCO concept being used, successful frequency locking is possible only



Legend:
FD: Frequency detector
IDiv: Integer divider
MDiv: Main divider
PD: Phase detector
Sync FF: Synchronisation flip-flop

Figure 4
Block diagram of the PLL synthesizer (external parts are in grey area).

with proper calibration setting of its capacitor matrix. During the sequential calibration flow, the calibration state machine automatically targets 24 fixed integer calibration frequencies for a reference setting of 22.4 MHz or 21 integer frequencies for a 26-MHz reference setting (both covering the specified frequency range). Reference frequencies such as 52 or 44.8 MHz are divided by two to match the PLL reference frequencies of 26 or 22.4 MHz.

Fast and precise frequency acquisition is accomplished by controlling (counting) the pulses on the input of the IDiv, which enables the maximum possible speed (or precision) of the measurement. In the present design, this is at least 13 times faster than the used reference frequency. The proper capacitor matrix settings are estimated in a successive approximation algorithm starting from the highest frequency. The algorithm estimates the most significant bit (MSB) setting first and all matrix bits are subsequently set/reset until the synthesizer frequency becomes within 1/2 of the least significant bit (LSB) of the calibration target (actual LSB frequency resolution varies over the frequency range because of the nonlinear dependence between capacitance and frequency).

The modification of the digital control value in the capacitor matrix (as a frequency value over time) is shown in **Figure 5** for a typical (simulated) successive approximation calibration flow for the frequency of 3.1808 GHz.

The calibration sequence ends with the setting of a preprogrammed frequency 2.912 GHz, which is needed for further calibration of the front-end.

After the programming of a fractional divider value during frequency hopping, the calibration data might differ by more than 50% of the reference frequency from the final target, mainly because of the fractional value. To avoid locking problems, the initial phase of the lock-up procedure repeats the last four steps of the calibration flow, readjusting the capacitor matrix. To ensure the maximum possible frequency acquisition precision (or minimum jitter) when a fractional divider ratio is used, the ΣΔ generator is forced to the first order during this phase. A further speed increase is achieved by skipping subsequent comparisons after eventually achieving the target locking precision (50% LSB) after any intermediate stage as shown in **Figure 6** (frequency value over time). With all the described techniques, this phase takes less than 20 µs to set the VCO frequency over the capacitor matrix to within 5 MHz of the target frequency.

3.2 Frequency/phase acquisition control

During the frequency acquisition phase (first part of the sequence in Figure 6), the ΣΔ generator is also forced to the first order to enable precise digital frequency comparison. The increased spurious generation with the

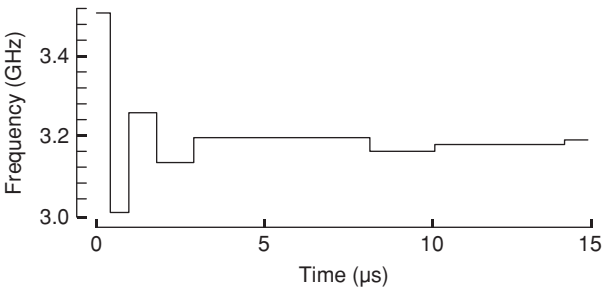


Figure 5
Frequency calibration sequence (VCO output frequency over time).

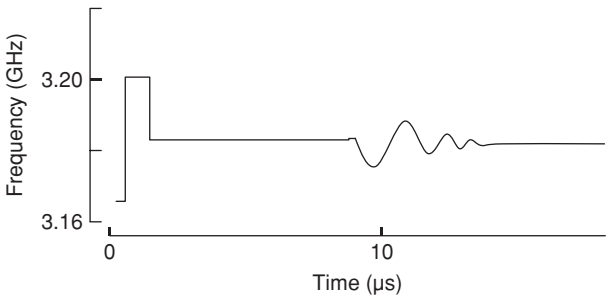


Figure 6
Output frequency during recalibration (shortened sequence) and final analog locking.

first-order ∑Δ is not relevant during frequency hopping because the carrier is not used at this time. Furthermore, the digital control unit forces the edge of the output divider pulses to a position very close to the target reference clock phase (see also ref. clock edges in **Figure 7**), avoiding a phase jump and resulting potential cycle slip and preventing any corresponding increase in the lock-up time.

3.3 Improved phase detector concept

The exclusive-OR (ExOr) phase detector principle, chosen for its linearity (inherently superior to phase frequency detectors) also has a disadvantage: The resulting output pulse duration, which is about 50% of the period for every pulse, causes 100% noise transfer for both output pulses from the current sources of the charge pump to the VCO. Further disadvantages are (i) the resulting high reference leakage power (the spectral power in the VCO output, placed at ± the reference frequency from the carrier), which increases the required loop filter order and (ii) the need for a precise 50% duty cycle reference.

A comparison with the most advanced phase frequency detector linearity and noise improvement techniques, reported in Reference 5), revealed a solution that avoids this problem. Using some of the additional six IDiv-cycles to define a precisely fixed length time-slot (a fixed position fraction of the reference clock cycle) for the charge pump output allows noise and reference leakage power reduction at least as efficiently as can be done with a phase frequency detector according to Figure 2.9 in Reference 6), while still keeping the superior linearity of the ExOr phase detector.

Three different possibilities (time slots) for masking the ExOr phase detector input are shown in Figure 7. They feature fixed lengths of 6, 4, or 2 IDiv pulses within a 13 pulse-cycle (first 7 cycles are controlled by the ∑Δ output which is a random integer between 0 and 7), so they reduce the effective output duty-cycle to 23%, 16%, or 7.7%, respectively. In the development described here, the second possibility was chosen with four pulses and a total output pulse duty cycle of 16%. The expected inherent static noise and reference leakage reduction is 3.25 times, or 10.2 dB. Further improvement up to 6.5 times (16.2 dB) should be possible if a very precise and fast charge pump is developed in the future.

3.4 Digital unit implementation

Because of the high complexity of the digital control unit (**Figure 8**) and synthesis difficulties resulting from the use of two asynchronous clock domains, care was taken to prevent noise coupling. Split supply domains were used to avoid an increase in jitter in the most critical clock paths (dark grey domain). The digital layout was also placed in a triple well region to isolate potential substrate noise from the sensitive area. Due to the high complexity, good testability is important and test features are

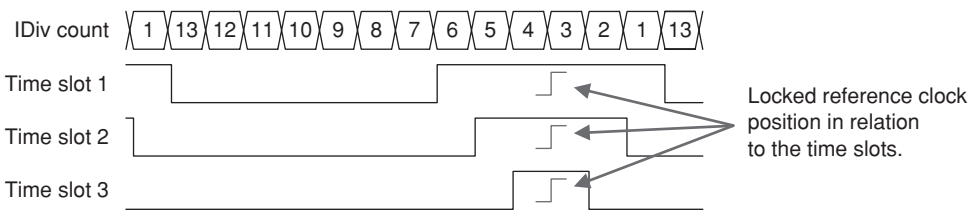


Figure 7
Three possible phase detector time slots derived from IDiv setting 13.

implemented in the synthesizer macro. Several internal signals can be routed to outputs and external signals can be forced to specific internal nodes.

4. Charge pump

The charge pump circuit is often a critical noise contributor in a frequency synthesizer. The challenge of improving it comes from the two conflicting mechanisms of in-band noise generation:

1) By direct noise generation of the output current sources, where a larger device size is the way to lower noise and
2) Non-linearity due to switching speed limitations, resulting in nonlinear ∑Δ-value-to-charge dependence. This nonlinear dependence folds the wideband sigma delta noise close to the carrier, increasing the in-band phase noise. A smaller device size enables a higher switching speed and results in less noise folding in that case, which conflicts with the first dependency.

While the amount of noise generated in the output current sources can be predicted quite well by simulation (though with considerable effort), a precise estimation of the folding of ∑Δ-noise over the charge pump (and phase detector) non-linearity to synthesizer noise is still too complex to be computable by simulation. The only possible approach with the existing development tools is to thoroughly evaluate the first silicon and then improve the balance in a subsequent design phase. A good performance balance is achieved when the difference between the integer and fractional performances approaches 3 dB.

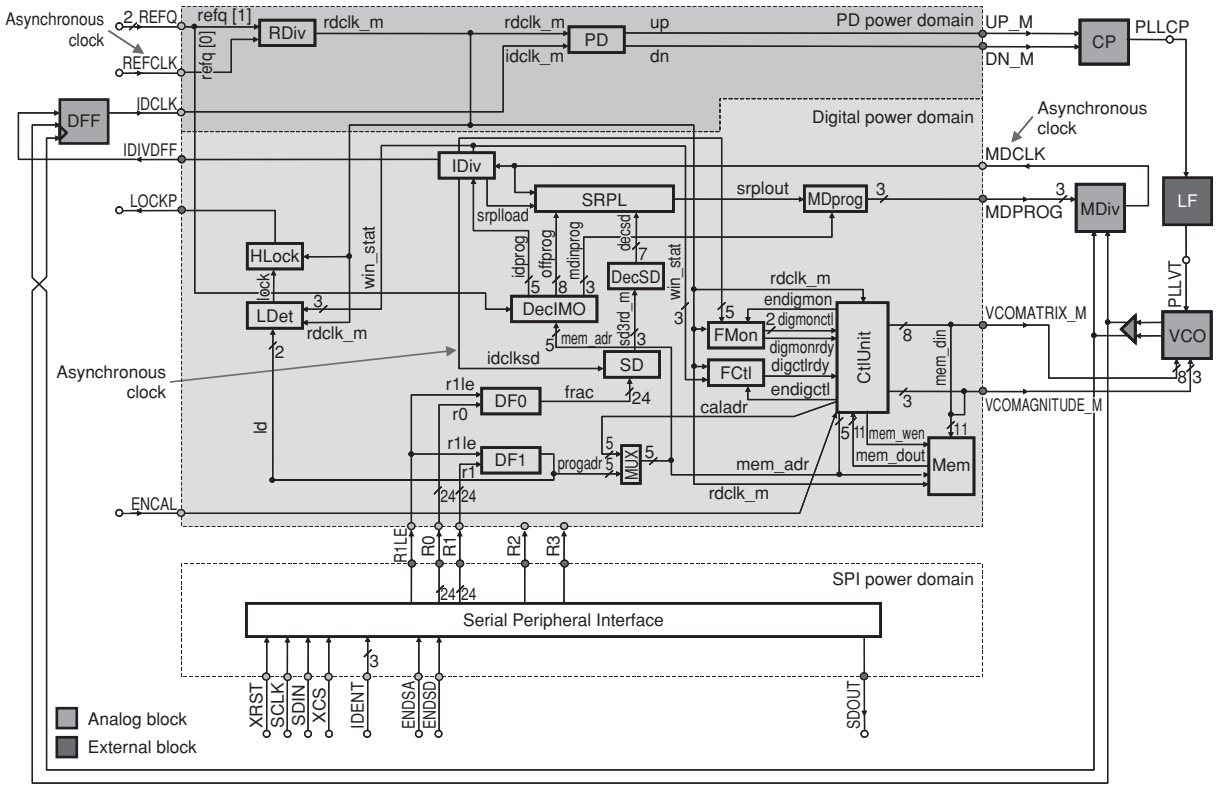


Figure 8
Block level diagram of the digital control unit and connectivity to other blocks.

The requirement for 1.2-V supply voltage operation (compared with 3-V for previous synthesizers) further increases the design difficulty because of the unfavorable ratio between the control value (2.4 times lower for a 1.2-V supply compared with a 3-V one) and input noise voltage of the biasing circuit (unchanged). Careful circuit improvement in this area and many iterative simulations were the key to reducing the impact of noise from the output current sources.

The use of 1.2-V devices and a modification of the output current switching for the PMOS current sources (from common source cascade type to transmission gate with a dummy load) was crucial to enable the output duty-cycle reduction (discussed in Section 3.3).

5. Measurement results

Measurement result at 3.01 GHz, presented in **Figure 9**, show that silicon PN-performance was close to what was expected. As shown by marker #7, the in-band noise level was –94.8 dBc/sqrHz.

A low PN level is the key to allowing the setting of sufficient synthesizer bandwidth to achieve a fast lock-up time. The bandwidth set for Figure 9 was about 200 kHz and this resulted in (integrated) RMS noise of 0.92° rms.

The measured lock-up time is shown in **Figure 10**, still with 200-kHz bandwidth and 0.92° RMS PN. It shows the output frequency error from the target (3.01 GHz) (vertical scale) against time (horizontal scale) after a new frequency was programmed. The specified final precision of <130 Hz was achieved after 130.8 µs.

6. Conclusion

We described the concept of a wide-frequency-range synthesizer capable of very low phase noise and fast hopping and suitable for integration in deep-submicrometer CMOS technology. The limitations on the analog performance (typical for this kind of technology) have been solved by choosing optimized circuit topologies and using sophisticated digital control algorithms. The required performance, which is not feasible with a completely analog design approach, was achieved by increasing the design complexity and using autonomous built-in state machines for continuous tracking and optimization of the analog operating points. This approach was also the key to compensating for the huge process variation range, which is a consequence of the reduced structure size in these state-of-the-art technologies. Measurement

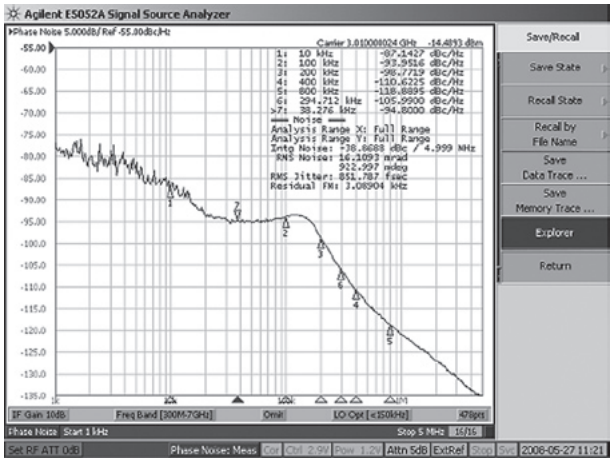


Figure 9
Synthesizer PN performance at 3.01 GHz.

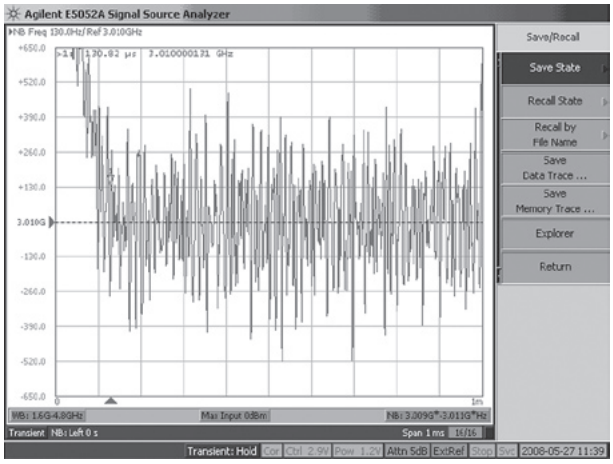


Figure 10
Synthesizer lock-up time at 3.01 GHz.

results showed phase noise of –94.8 dBc/sqrHz and a lock-up time of 130.8 µs, which are very close to the expected values. Three novel techniques were successfully implemented within the synthesizer design, allowing a simplified prescaler and extremely good phase detector linearity. The phase detector concept used in this development has potential for future phase noise improvement. This potential must be weighted carefully against the increasing effort and risk due to accumulated design complexity.

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