Novel Compact RF Module for Mobile WiMAX Terminal Equipment

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This paper describes a radio frequency (RF) module for Mobile WiMAX, where low cost, low power consumption, and small size are needed. To satisfy these requirements, we developed a new micro-size RF module and a new RF CMOS LSI using 90-nm CMOS technology. The RF module supports downlink multiple-input multiple-output (MIMO) technology and includes RF-LSIs, a power amplifier, a voltage-controlled temperature compensated crystal oscillator, and band-pass filters. Its size is 15 mm × 15 mm × 1.5 mm. This new RF module is the smallest in the world and includes all of the RF circuits necessary for Mobile WiMAX. The 2.5-GHz frequency band is supported and the RF bandwidths are 5 and 10 MHz. (WiMAX Forum profile: 3A.) This paper presents the RF architecture and high-frequency circuit technology used for the RF-LSI and RF module. The advantage of the RF module is that design engineers can easily get high-quality RF performance without special RF knowledge.

1. Introduction

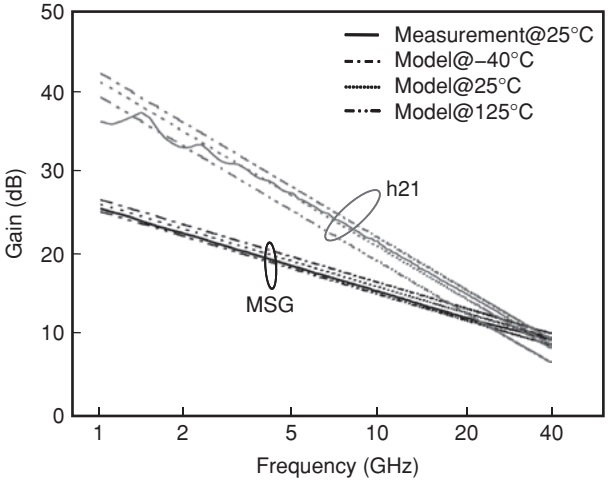
Wireless broadband access technology is used for high-speed Internet access, and the market for the latest wireless system demands ever higher speeds for data communications. As a system that meets these demands, Mobile WiMAX enables high-speed mobile Internet access. In particular, Mobile WiMAX best meets the requirements for mobile broadband Internet access and gives flexibility in the design of networks. This system is based on the IEEE 802.16e-2005 standard (released December 2005).[1] Therefore, this system is different from conventional cellular phone systems. Its basic performance gives a maximum data rate of about 37 Mb/s with a 10-MHz bandwidth.[2),3] This is the fastest among current mobile wireless systems. The modulation technique used for Mobile WiMAX is orthogonal frequency division multiple access (OFDMA), which is also under consideration for 4G systems.[4] Consequently, this system has the potential to become the main technology for the next-generation wireless systems.

During the design of the RF-LSI for Mobile WiMAX systems, the key issues are low power consumption, linearity, and wideband performance for the RF analog circuits. Although there is a tradeoff between low power consumption and linearity for a wideband system, both requirements must be satisfied for mobile terminals.

In this paper, we first describe Fujitsu's 90-nm CMOS process technology for RF-LSIs. We then discuss the RF architecture,[5),6] the receiver, transmitter, and synthesizer circuit design, and the RF module composition and performance. In addition, we describe a method of calibrating each block by process variation.

2. Fujitsu's 90-nm CMOS process technology

This technology is fully compatible with digital processes and consists of nine copper



MSG: Maximum Stable Gain
h21: h-parameter

Figure 1
Comparison of measurement data for various temperature models.

layers and one aluminum layer with standard components, including metal-insulator-metal capacitors giving up to 1 fF/μm^2 and low-leakage MOSFETs.

For good performance, for certain layouts, the N-MOSFET gives an fT of up to 120 GHz and the P-MOSFET up to 65 GHz. Comparison data for the 1.2-V N-MOSFET for various temperatures are shown in **Figure 1**. The technology supports varactors without the use of any additional process steps. The varactors allow wide tuning with a capacitance ratio of up to 3.4. A quality factor of 160 is achieved at 5 GHz.

Inductors are indispensable for RF circuits and these use three-layer stacking to give reduced resistance. As a result, quality factors as high as 20 have been achieved for a low-frequency inductance of 1 nH. This design is complemented by the use of ground shields specifically designed to reduce eddy currents and an electric field that penetrates the conductive silicon substrate.

3. RF architecture

The RF architecture for the LSI is shown in **Figure 2**. This LSI uses two stages of conversion for low power consumption and easily meets the specifications for relative constellation error (RCE). The receiver uses two down-conversion stages using a first local oscillator (LO1) frequency and a second local oscillator (LO2) frequency, translating the input spectrum from the 2.5-GHz-band WiMAX signals to an intermediate frequency (IF) and subsequently to zero with a quadrature demodulator (QDEM). The baseband signals are then applied to low-pass filters (LPFs) and variable gain amplifiers (VGAs). The transmitter uses two up-conversion stages. The WiMAX quadrature signal output from an analog-to-digital converter (ADC) is input to a quadrature modulator (QMOD) through LPFs and variable attenuators (VATTs). The modulated transmitter signal is converted to IF by the QMOD (mixed with LO2) and subsequently to the 2.5-GHz band by an up-mixer (mixed with LO1) through IF-VGAs. The synthesizer uses a fractional-N phase locked loop (PLL) to get fine tuning steps with fast hopping.

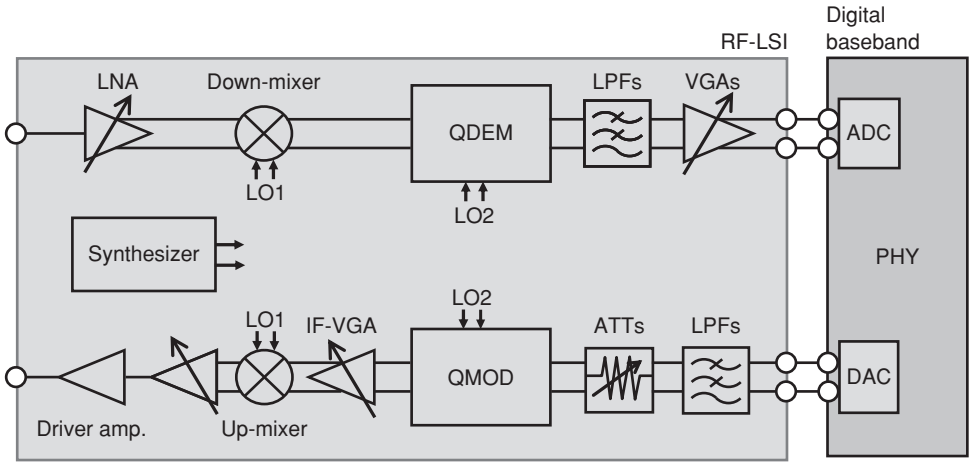
Considering the number of external surface-mounted components, we used single-ended ports for the RF input/output port. However, on the RF LSI side, the circuits were designed by applying differential circuits for noise isolation. The supply voltages are 1.2 and 2.9 V. Details of each block are given in Section 4.

4. RF-LSI circuit design

In this section, we give details of the receiver, transmitter, and synthesizer circuit designs.[7] A die microphotograph of the RF-LSI is shown in **Figure 3**. The chip size is 5 mm × 5 mm.

4.1 Receiver block

A detailed block diagram of the receiver is shown in **Figure 4**. The RF front-end consists of a variable gain low-noise amplifier (LNA) with an on-chip matching network (input impedance: 50 ohms). The down-conversion mixer (down-MIX) with a single-to-differential converter is shown in **Figure 5**. The LNA uses a well-known inductive source degeneration



ADC: Analog-to-digital converter
DAC: Digital-to-analog converter
LNA: Low-noise amplifier
PHY: Physical layer

Figure 2
RF architecture.

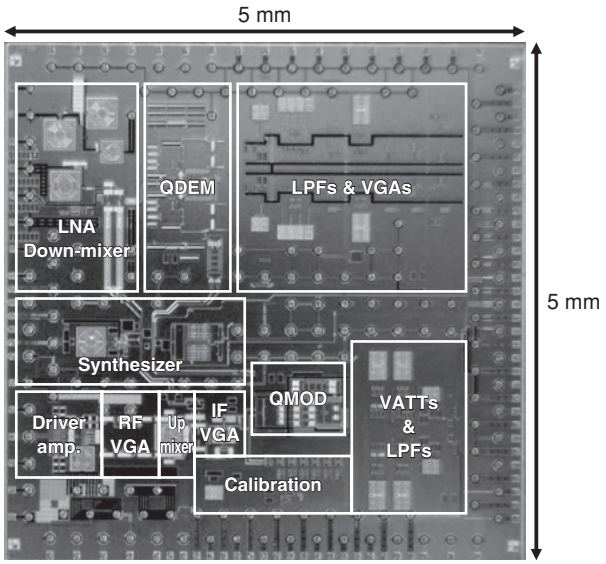
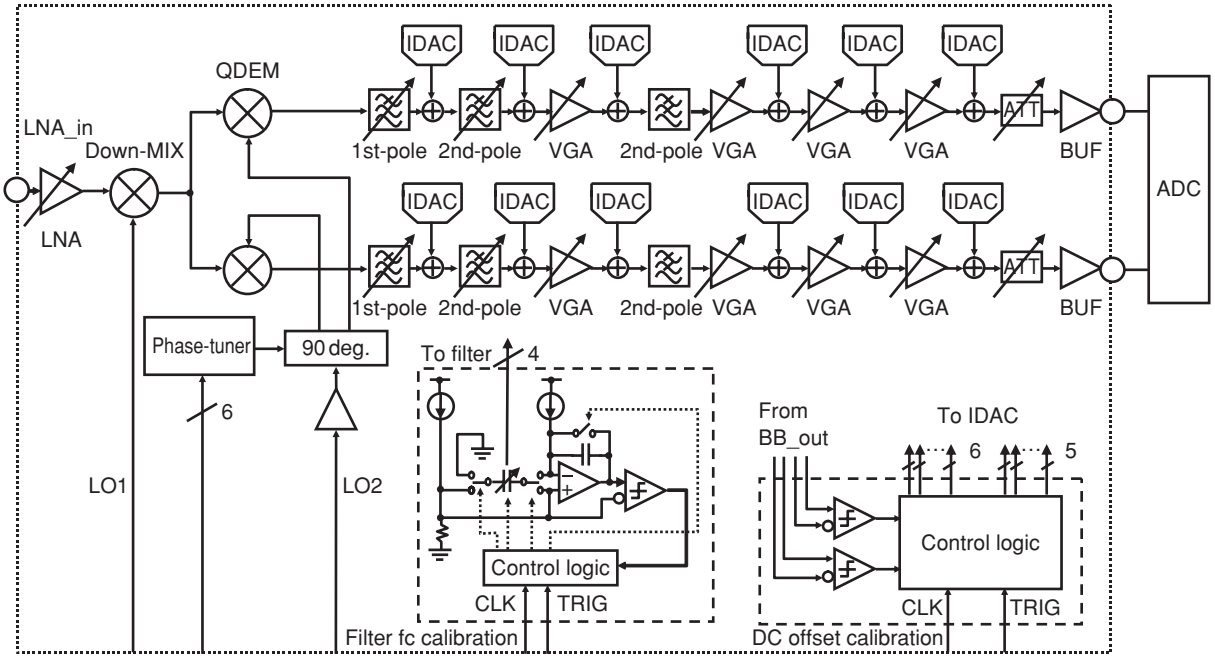


Figure 3
Chip microphotograph.

technique. The simulated return loss of the input port is less than –20 dB in the operating frequency range from 2.496 to 2.69 GHz. The cascode transistor switches the gain between 8/23/28 dB using the logic of SW1, SW2, and SW3, respectively, to avoid distortion. SW1X, SW2X, and SW3X use inverted logic. The simulated noise figure is 2.5 dB at the maximum gain of 28 dB.[8] The down-MIX topology is a double balanced mixer with quasi-differential resistive source degeneration.[9] This down-MIX has a single-differential converter circuit in the front of the input.

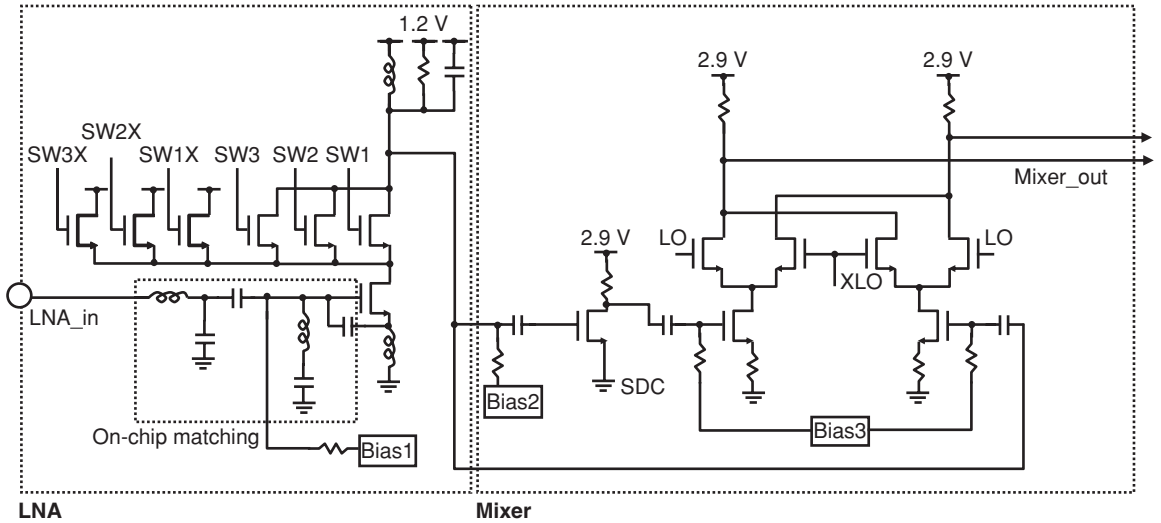
The QDEM has two double balanced mixers for the I and Q channels. The flicker noise of the QDEM is the one of the most important factors for the WiMAX receiver because the WiMAX subcarrier is at 10.9375 kHz. Therefore, the transistors in the QDEM are large in size to reduce the flicker noise. The measured corner frequency of the flicker noise was around 30 kHz.[1]

The 1st-pole LPF topology is an RC-active filter. The variable capacitors compensate for the process and the temperature variation of the cutoff frequency (fc). The digital code of the variable capacitor is fed by the filter fc calibration circuit. The digital code of the variable capacitor is determined by comparing the RC time constant with the clock. The variable resistors select the baseband bandwidth and the gain. The cutoff frequency can be chosen as 2.5 or 5 MHz. The gain can be selected from –3 to 9 dB in 6-dB



BUF: Buffer
BB: Baseband

Figure 4
Receiver and calibration block diagram.



XLO: Crystal local oscillator
SDC: Single differential converter

Figure 5
Receiver RF front end.

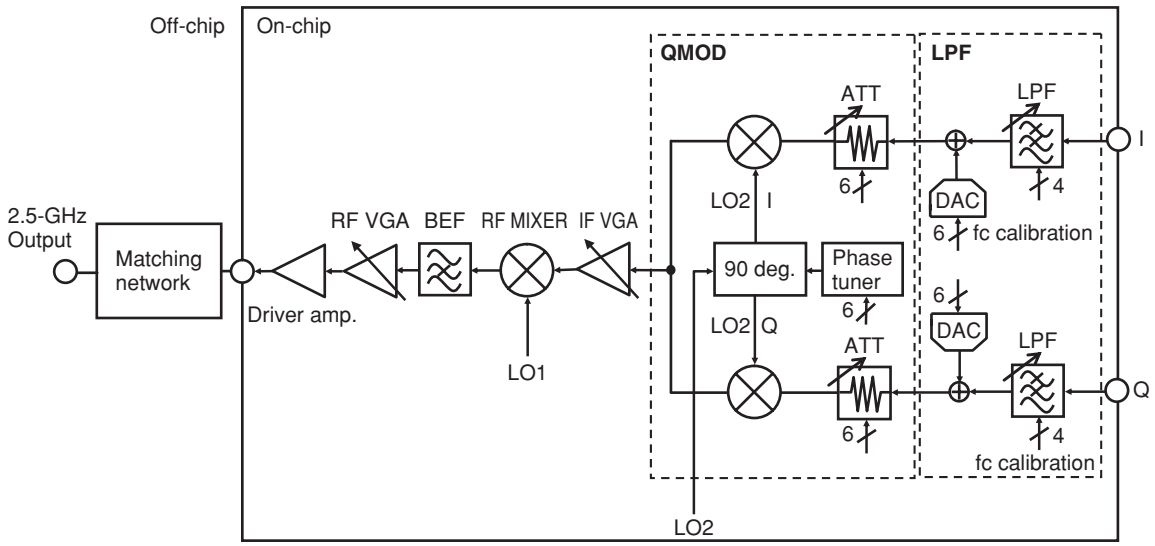


Figure 6
Transmitter block diagram.

steps. The current digital-to-analog converter (IDAC) is used to calibrate the output DC offset voltage. The IDAC digital code is fed by the DC offset calibration circuit shown in Figure 4. The binary search for the IDAC digital codes starts from the 1st-pole LPF and proceeds to the last stage of the VGA.

Two biquad-RC-active LPFs (2nd and 3rd stages) and four VGAs follow the 1st-pole LPF. The 2nd stage of the LPF has a variable gain range from 0 to 6 dB in 1-dB steps. Each VGA has a variable gain ranging from −2 to 12 dB in 1-dB steps.

4.2 Transmitter block

A detailed block diagram of the transmitter is shown in **Figure 6**. The transmitter consists of baseband LPFs, VATTs, QMOD, IF-VGA, up-mixer, RF band elimination filter (BEF), RF-VGA, and driver amplifier. The IF-VGA and the RF-VGA are used to expand the transmitter dynamic range. The IF-VGA provides 29.5 dB of gain control in 0.5-dB steps and the RF-VGA provides 48 dB of gain control in 6-dB steps.

The analog I/Q modulation signals are generated by DACs. The LPFs are designed to have a fifth-order active Butterworth low-pass filter response with 3-/6-MHz cutoff frequency settings. The process and the temperature variation of the cutoff frequency are compensated by the calibration circuit. The QMOD converts to an IF modulated signal. A pair of double balanced mixers is used in the QMOD. Two 6-bit VATTs and a 6-bit phase-tuner in the QMOD section are used to correct quadrature amplitude and phase errors. The quadrature error correction improves the modulation accuracy. This is one of the key issues for Mobile WiMAX systems. With our correction technique, the QMOD achieved a measured RCE of less than −46 dB.[10)]

The IF signals are converted into an RF signal by a double balanced up-mixer. The BEF rejects the image output of the RF mixer and improves the linearity of the driver amplifier. It consists of on-chip capacitors and inductors.

The driver amplifier has a cascode structure to ensure that the driver's amplifier outputs are isolated from its input and to maintain the stability of the driver itself. It consists of two stages, and it has a normal mode and a power-saving mode, achieved by controlling the bias to reduce the current consumption at each output power

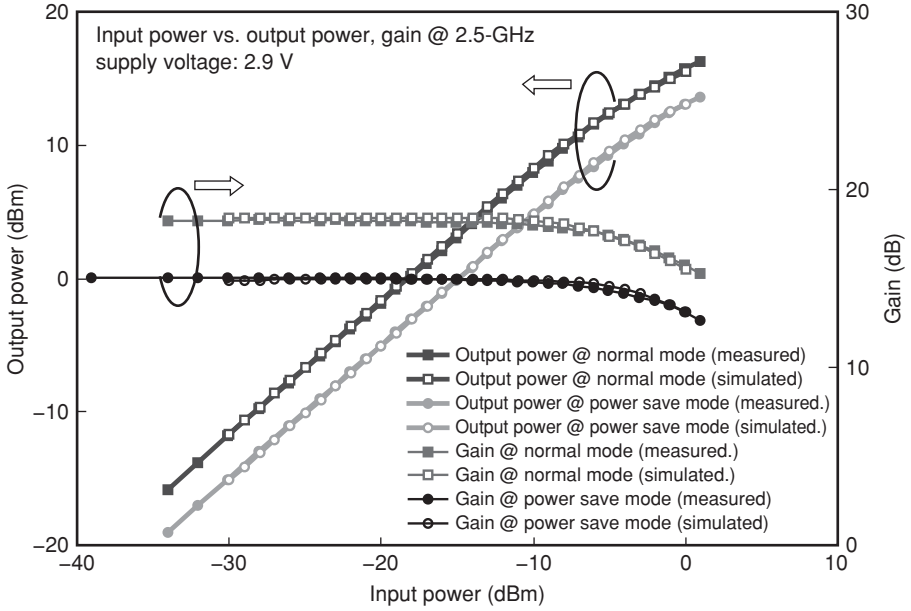


Figure 7
Measured driver amplifier output power.

level. The first amplifier is a class A amplifier for linearity, while the second amplifier is class AB for low power consumption. The output of the transmitter is a single-ended circuit, which avoids the use of an external element such as a balun. The output impedance is matched to 50 ohms in the operating frequency range from 2.496 to 2.69 GHz by a matching network that uses external surface-mounted devices.

The measured output power and gain of the driver amplifier at 2.5 GHz are shown in **Figure 7**. In normal mode operation, the driver amplifier had 12.4 dBm output power at 1 dB compression (OP1dB) and power gain of 18.3 dB. In the power saving mode operation, the driver amplifier had 10.8 dBm OP1dB and power gain of 15 dB.

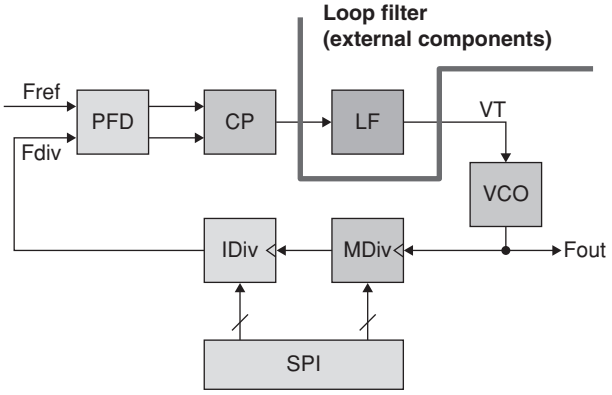
The simulated output power and gain of the driver amplifier are also shown in Figure 7. The measured and simulated results show good agreement. The simulation was carried out by applying a transmission line model. This model takes into consideration the parasitic resistance, capacitance, and inductance of the wiring in the LSI. It gives an accurate characteristic of the RF elements in our RF CMOS.

4.3 Synthesizer block

A block diagram of the synthesizer is shown in **Figure 8**. The voltage control oscillator (VCO) is designed for a wide spread of process corners and guaranteed frequency range. A low-phase noise oscillator is achieved by using an LC tank oscillator with a self-tuning amplitude tuning block. The evaluated phase noise at an offset of 100 kHz was −100 dBc/Hz. The size of the varactors is designed to achieve low VCO gain for better noise performance and to have a margin for process corners and for temperature and voltage variations. To get fine tuning steps with fast hopping, a fractional-N PLL is used. A third-order sigma-delta algorithm is implemented by digital design and guaranteed up to the 40-MHz reference clock (reference clock frequency = Fref [Hz]). The frequency step is

$$\frac{Fref}{2^{24}}\ [\mathrm{Hz}].$$

For the sigma-delta algorithm, a high-speed



CP: Charge pump
IDiv: Ordinary digital divider
LF: Loop filter
MDiv: High-speed programmable divider
PFD: Phase frequency detector
SPI: Serial port interface

Figure 8
Block diagram of synthesizer.

programmable divider is inserted between the VCO and the ordinary digital divider. It is designed to use CMOS inverter logic for low power consumption. An EXOR-type phase frequency detector is used for better linearity, and reference leakage is suppressed by a conventional external loop filter with an additional RC-LPF.

5. RF module

The RF module is designed for downlink multiple-input multiple-output (MIMO) mobile applications. The module is fully integrated with the transceiver LSIs, antenna switches, power amplifier, band-pass filters, detector and voltage-controlled temperature compensated crystal oscillator on a four-layer FR4 substrate. The RF input/output port impedances are matched to 50 ohms in the operating frequency range from 2.496 to 2.69 GHz. To reduce the module size, we reduced the number of external parts by reviewing the layout of external parts and selecting the best circuit topology. Moreover, we applied high-density mounting in consideration of the RF circuit isolation. Signal losses are reduced to 2 dB by matching the off-chip circuits. The module has a small size package (15 mm × 15 mm × 1.5 mm). This is the smallest size in the world to date. The target power class is class 1.[10] A photograph and block diagram of the module are shown in **Figure 9**.

The benefits that this RF module brings to design engineers include good-quality RF performance that can be obtained easily without special RF knowledge.

6. RF module performance

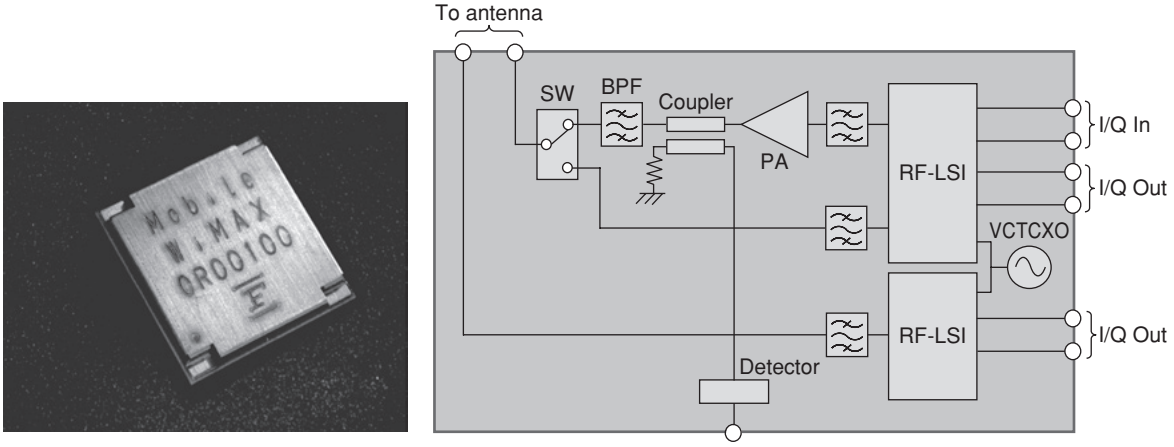
In this section, we describe the RF performance of a Mobile WiMAX terminal using the RF module.

6.1 Receiver characteristics

The receiver characteristics were measured with a vector signal generator and vector signal analyzer for modulation of OFDMA signals and analysis of the baseband outputs. The downlink signal used partial usage of subchannels (PUSC) with bandwidth of 10 MHz and a modulation coding scheme of QPSK12, 16QAM, or 64QAM.

The measured RCE of the output signal for various input powers is shown in **Figure 10**. The value of RCE at low input power was determined by the thermal noise of the circuit, and the noise figure was calculated to be 5.5 dB from the ratio between the RCE and the thermal noise of the input signal. At higher input levels, RCE was –32 dB, which equals the phase noise of the local oscillator. Labels in Figure 10 indicate the minimum required signal-to-noise ratio (including a 5-dB margin for implementation loss) for the minimum receiver sensitivity requirement.[10]

The bit error rate (BER) measured on the RF module connected to the digital baseband is shown in **Figure 11**. As predicted from the RCE results, the BER was lower than 1 x10^{-6} at the maximum sensitivity level. As shown by this figure, the specification was satisfied. Therefore, our receiver has sufficient performance to be used in Mobile WiMAX. The current consumption of



(a) Photograph (b) Block diagram

SW: Switch
PA: Power amplifier
VCTCXO: Voltage-controlled temperature compensated crystal oscillator

Figure 9
Photograph and block diagram of RF module.

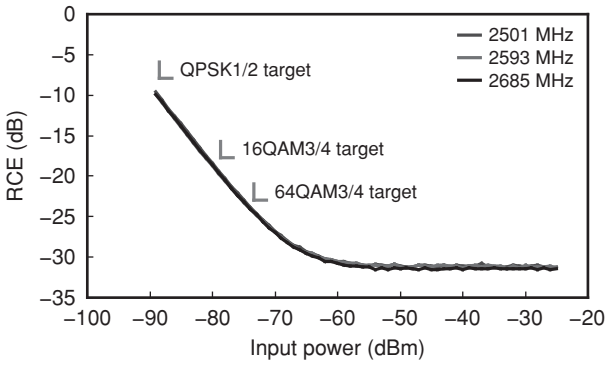


Figure 10
RCE of receiver baseband output (BW = 10 MHz).

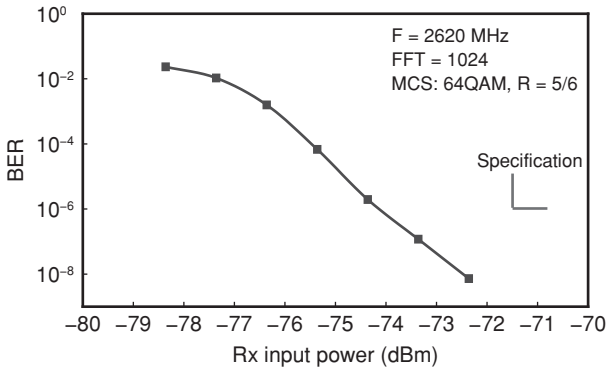


Figure 11
BER measurement results.

the receiver was 230 mA in MIMO mode.

6.2 Transmitter characteristics

The transmitter characteristics were measured with an uplink signal of PUSC and modulation coding scheme of QPSK or 16QAM with bandwidth of 10 MHz.[10] The variation in RCE with output power is shown in **Figure 12**. The main characteristics of the power amplifier are power gain of 25 dB and OP1dB of 27 dBm (including losses at the filter before and after the power amplifier). The power supply voltage of the power amplifier was 3.3 V. The total output level was controlled by the RF-LSI. RCE is the parameter used for indicating the quality of modulation accuracy. The available power is limited by RCE requirements of less than –24 dB. An available power range of more than 50 dB was achieved. The output spectrum at 20 dBm was within the emission mask (**Figure 13**). Thus, the performance of the transmitter met the specifications sufficiently with a wide bandwidth. The current

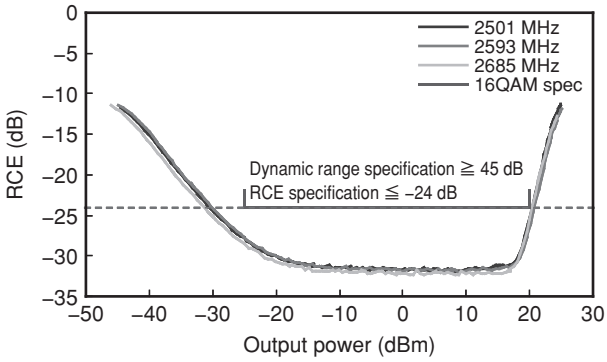


Figure 12
RCE of transmitter RF output (BW = 10 MHz).

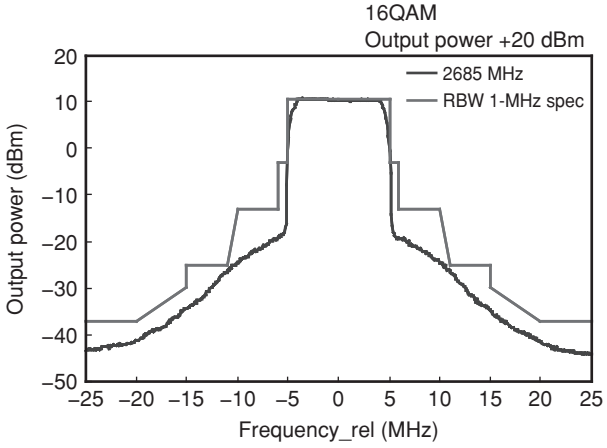


Figure 13
RF output spectrum and emission mask.

consumption was 498 mA at an output level of 18 dBm, and 549 mA at 20 dBm; the increase is also attributed to the power amplifier.

7. Conclusions

This paper discussed a fully integrated transceiver LSI using Fujitsu's 90-nm CMOS technology developed for 2.5-GHz-band Mobile WiMAX systems. The characteristics of an RF module applying this RF LSI were confirmed to satisfy the Mobile WiMAX specifications. Moreover, we achieved, for the first time, an RF Module for Mobile WiMAX terminals that is small and has low power consumption. Its size is the smallest in the world. A summary of the RF module's performance is given in **Table 1**. These performances meet all the specifications of Mobile WiMAX. As the next step, we plan to develop an RF-LSI that is even smaller and has even lower power consumption for Mobile WiMAX downlink MIMO systems with multi-band capability.

Table 1
Summary of the RF module performance.

Module size		15 mm × 15 mm × 1.5 mm
Frequency range (3A)		2.496–2.69 GHz
RF bandwidth (3A)		5/10 MHz
RF input/output impedance		50 ohms (< –15 dB return loss)
Supply voltage		1.2/2.9/3.3 V (for PA)
Rx	current consumption	230 mA
	RCE (–71.5 dBm input)	–27.6 dB
	RCE (–88.5 dBm input)	–12.4 dB
Tx	power consumption	549 mA @ 20 dBm
	dynamic range	Over 50 dB (spec.: over 45 dB)
	maximum output power	20 dBm (power class 1)

3A: WiMAX Forum's certification profile

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