TMP for Assuring Quality of Hardware Products

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Today's high-end servers require leading-edge hardware designs and growing numbers of components made by outside manufacturers. This makes it increasingly difficult to ensure the highest possible quality of such servers. We have therefore developed a Test and Maintenance Program (TMP) that assures product quality throughout the life cycle. The main development goals for this TMP are high fault detection performance, powerful fault analysis functions, and simple operability. The quality assurance and field support units use TMP to verify the design of Fujitsu's hardware products and maintain the products at customer sites. This paper describes the development policies for TMP and the technologies employed.

1. Introduction

The logical design of hardware products in the field of information and communication has recently become increasingly complex, along with a larger scale of firmware to realize higher capacity, performance, and reliability. Ensuring the quality of such products at earlier stages has become a major concern. Accompanying the high-density packaging of LSI and devices, signal integrity problems due to noise and temperature margin problems posed by higher temperatures are likely to occur. It has therefore become important to evaluate actual devices by focusing on packaging designs.

Given this situation, Fujitsu has developed a Test and Maintenance Program (TMP) for verification, mass-production testing, and field maintenance so that customers can use high-quality hardware products with a high sense of security. Fujitsu uses the program to assure product quality throughout the life cycle, including design, manufacturing, and maintenance (**Figure 1**).

This TMP covers most Fujitsu products including enterprise servers, storage and network products, ubiquitous PCs, and cellular phones. Fujitsu employs this program for conducting shipment tests of other companies' OEM products, such as Sun servers and CISCO routers, and thus contributes to compliance with Fujitsu's rigorous quality standards. Fujitsu also cooperates with the manufacturers of such components as memories and optical disk devices, and performs Joint Qualification (JQ) through TMP to improve the quality of parts shipped by those manufacturers.

This paper describes the TMP development policies and TMP technologies employed for design verification, device evaluation, and maintenance support.

2. TMP development policies

Fujitsu develops TMP in line with the two policies described below, along with three targets established for each policy. Fujitsu improves TMP on a daily basis upon receiving feedback from customers and according to advances made in hardware devices. Above all, Fujitsu attaches high value to high fault detection performance, powerful fault analysis functions, and simple operability.

1) Testability (for high fault detection performance)
- Comprehensively verify the functions of a device to avoid the shipment of defective products (by using powerful fault analysis functions).
- Detect and identify failures and promptly solve trouble (by using powerful fault analysis functions).
- Detect both logical and physical incorrectness and identify problems attributed to design or manufacturing (for higher equipment quality).

2) Operability (for higher user satisfaction)
- Conduct tests automatically in a short time with execution controls corresponding to design verification and mass production tests (for ensuring operability).
- Display test results in an easily understood manner and clearly articulate criteria (for judgment of acceptance).
- Collect information about test conditions and mid-results to accelerate failure investigation and provide a variety of reports (for providing fault identification information).

3. TMP technologies for design verification

In design verification, the Test Program (TP) guarantees that hardware is designed in accordance with device and interface specifications. As listed in **Table 1**, TP is developed depending on the purpose of verification. TP verifies individual functions, combinations of functions, robustness under high stress, Reliability, Availability, and Serviceability (RAS), and the hardware performance.

It is crucial to extract the test cases necessary for developing TP. For that reason, we prepare test cases from the viewpoints of designers and users, upon fully understanding not only the architectural specifications of targeted devices, but also the specifications to be implemented. After extracting the test cases from product specifications through the input of external and internal device specifications, we implement TP from the following standpoints.

1) High fault detection performance

High fault detection performance is used to verify the operations and specifications described in device specifications and design diagrams in full detail. All normal operations, exceptional operations, and competitive conditions are extracted as possible test cases that can be realized by software.

2) Verification of test results

All test cases should have correct values for

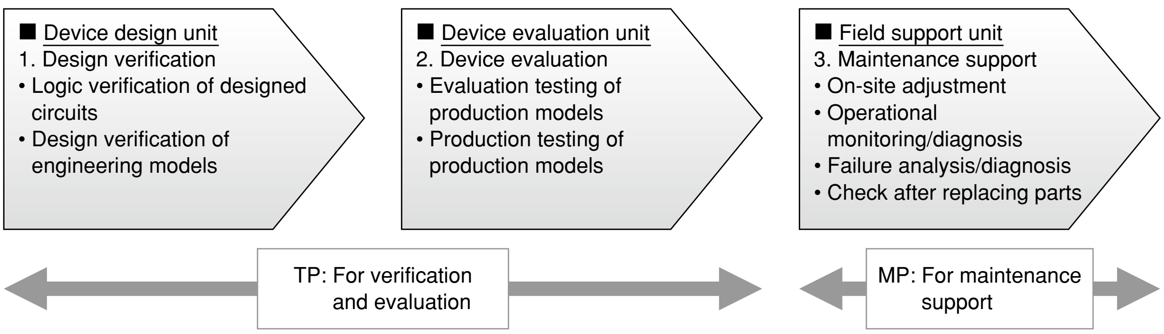

Figure 1
TMP for hardware life cycle.

comparison with the results of tested devices. Manually preparing the correct values for all test cases would entail a huge amount of man-hours and the likely occurrence of errors. Therefore, we use software that simulates tested devices assumed to be the targeted devices, and then collect the expected values for input into TP.

Figure 2 shows a schematic diagram of the logical design verification of CPUs and the chip set mounted in a server. A design model is laid out in the emulator with TP installed for verifying the logical design mode. Palladium II (Cadence Design Systems, Inc.) used for verifying SPARC Enterprise has a maximum clock frequency of 1.5 MHz, which is twice as fast as that of the previous generation. Once TP is run, CPU firmware, Solaris and SPECmark (benchmark software) can be run. This co-verification between hardware and software facilitates testing on actual test model devices as described below.

Table 1
Test program categories.

Functional test	Verification of individual functions
	Verification of combined functions
	Verification of micro-architecture
Load test	Verification of operation loads
	Verification of competitive timing
RAS test	Verification of failure detection mechanism
Performance test	Verification of individual performance
	Verification of complex operation performance

Figure 3 shows the sequence for verification of a mobile phone prototype. The average development period for a mobile phone is as short as 12 months. Therefore, testing a software-mounted device after testing the hardware is too late relative to shipping the product. In addition, consistency with the procured parts must be verified for designing boards as new mobile phones contain CPUs, chip sets, cameras, and flash memories incorporating the latest technologies. This is why we confirm the co-verification between hardware and software, for which we design a prototype called an “enlarged board” and run TP, basic software and applications on that board.

4. TMP technologies for evaluating devices

We test hardware and RAS functions, verify execution performance, and test operational stability with various margins, such as for temperature, voltage and the clock. We have developed three types of TPs for use in these tests: the firmware built-in type, stand-alone

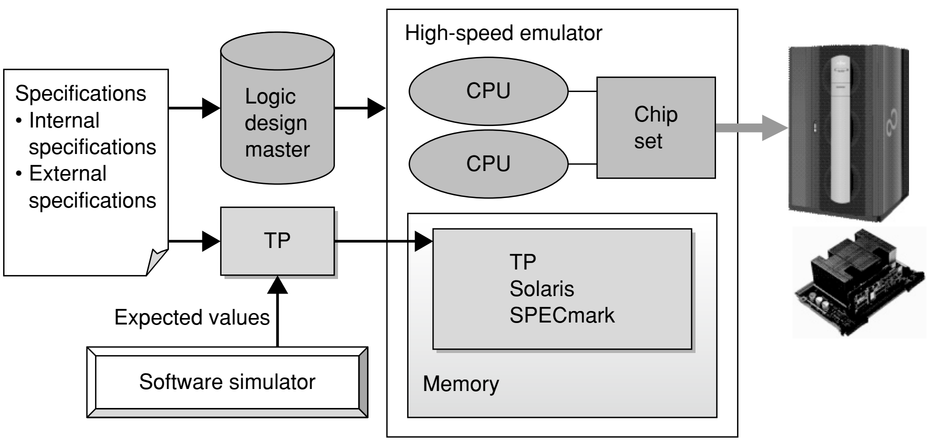

Figure 2
Logical design verification of server.

type, and application type which run on the operating system. Stand-alone type TPs were the mainstream for mainframes and UNIX servers. However, more application-type TPs are now being used for recent open platform products. The main reasons for such change are that the specifications of target products represent black boxes (i.e., invisible from outside) and product development periods are becoming increasingly shorter. TP development conventionally took the authors about six months on average. The development periods for PCs and mobile terminals, however, are now as short as two or three months. Thus, we are being requested to shorten the development period every year. The precision of technologies used for verifying the black boxes has become more important because Fujitsu products consist of many parts procured from vendors. The authors are improving techniques by referring to white papers published by vendors, investigating bus operations, and accumulating data on the recurrent testing of defective products, in addition to know-how cultivated in verifying mainframes.

The products designed by Fujitsu and those being procured reflect an accelerated trend toward higher frequency, lower voltage and miniaturization. Moreover, it is difficult to avoid design and manufacturing defects that involve physical or electrical factors at the upstream logical verification phase. In particular, noise and heat pose common problems among mobile terminals and mission-critical server products. These problems must be detected in earlier phases of evaluating devices. We horizontally spread the following activities for all Fujitsu products:

1) Accelerating rises in temperature through concentrated access of the CPU core, chip set and memory
2) Detecting SRAM/DRAM defects based on crosstalk and switching patterns
3) Detecting crosstalk noise defects of the system and I/O bus
4) Detecting load change failure of the DD converter through excessive memory access

Like ubiquitous products, server products are encountering increasing problems regarding thermal design. CPUs and memories are said to account for 70% of all heat generated by a device. The authors have developed TP that fully activates the internal logic of the CPU core and memory to guarantee that heat exceeding the specifications is not generated even when running an application. **Figure 4** shows the results of an internal temperature accelerated test of the CPU used in Fujitsu's PRIMEQUEST mission-critical IA server. Fujitsu's TP establishes + 3 to 5°C in a shorter time than the linpack and SPECmark benchmarks known as high-load tools in the field of High Performance Computing (HPC), thus contributing to the selection of chips that exceed the rated power consumption.

Figure 5 shows the results of tests that

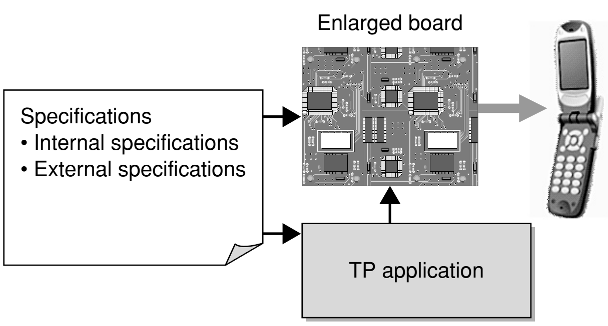

Figure 3
Verification of mobile phone prototype.

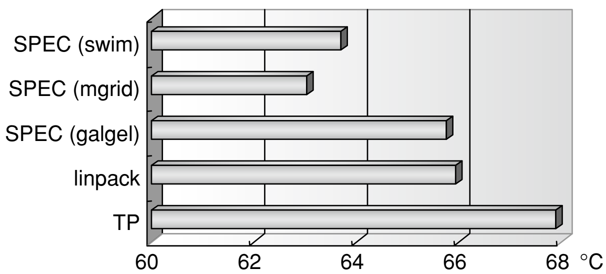

Figure 4
Comparison between TP and benchmarks regarding acceleration performance at different CPU internal temperatures.

induce switching noise in Fujitsu routers. These tests were conventionally conducted by applying packets from a general tester. Given the higher speeds of devices, however, it is becoming increasingly difficult to apply sufficient loads. In GeoStream R980, the packet forwarding circuit has a looped configuration formed by TP to make an internal loop for realizing loads near the theoretical figure. For applied data, crosstalk and Serdes patterns are used for parallel and serial buses, respectively, thus enabling the detection of noise failure, which a general tester cannot detect.

5. TMP technologies for supporting maintenance

The Maintenance Program (MP) is software used by Customer Engineers (CEs) to securely and effectively perform operations in order to stably operate customer systems. MP is used for adjusting and repairing devices, conducting periodic inspections, and monitoring operations at customer sites following device shipment. The main features of MP are as follows:

- Identification of failed parts by diagnosing hardware
- Collection of system logs and analysis of failure
- System configuration display and notification of modified system settings
- Handling multiple PCs and servers through one-touch operation
- Remote notification

There are two types of MP: the stand-alone and online types. Both are used depending on the characteristics of maintenance.

5.1 Stand-alone type of maintenance program

This type of MP is used for confirming normal operation and identifying any failed parts of hardware, mainly during on-site adjustments and maintenance with the system stopped. This tool does not involve use of the customer's OS. It starts up from bootable media and diagnoses the hardware.

Users in other countries often maintain their own PCs and open servers. Customers in Japan are now also reflecting this trend.

We initially began shipping notebook computers with the BIOS built-in diagnosis function in models released in the summer of 2006. Because diagnostic software is built into the devices, it is possible to diagnose hardware immediately after trouble occurs. Customers can thus make the primary judgment on whether to recover the software or contact the call center based on the results they have diagnosed. We now plan to support the BIOS built-in diagnosis function in desktop PCs and PC servers as well.

5.2 Online type of maintenance program

Nowadays, systems generally operate 24 hours a day, 365 days a year. There are high requirements for monitoring systems and diagnosing hardware without interfering with customer business operations. This tool operates as a common application on customer systems,

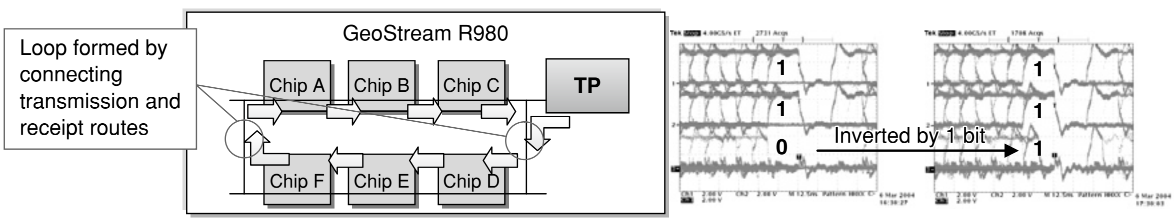

Figure 5
Effect of noise pattern testing.

displays system configuration information, diagnoses hardware online, monitors failures, analyzes logs, and collects such environmental information as device temperature and voltage. The following describes the Hardware Resource Monitor (HRM) that has been provided for open platform products (e.g., PCs, UNIX servers) since 2005.

The HRM client program is bundled in the Field Support Tool (FST) carried by CEs, with the HRM agent program preinstalled in monitored PCs and servers. It is possible to monitor multiple servers, storage, and network devices by IP-connecting FST to a customer network. The management software included as standard in devices typically employs different user interfaces. This proved burdensome for CEs. The HRM offers a unified view, however, and makes it possible to display the hardware configurations of up to 1024 servers, collect logs and perform online diagnosis through easy operations. **Figure 6** shows the system configuration view of multiple servers and the ETERNUS connection state. As of April 2007, the HRM supports Fujitsu's PRIMERGY, PRIMEPOWER, PRIMEQUEST, SPARC Enterprise, the ETERNUS series, and the FMV series. It is characterized as follows:

1) Unified operational views supporting multiple platforms
- The burden on CEs is reduced due to the unified maintenance of different devices.
- Effective maintenance is possible due to the gang operation of multiple devices.

2) Easy-to-understand system configuration and status
- Device configurations and statuses are displayed, with modified configurations being reported.
- Time-series variations in device temperature, voltage, and fan revolution are possible.

3) Online diagnoses not affecting business operations
- Such core parts as the CPU, memory, and HDD are diagnosed.
- Preventive diagnosis is possible during periodic patrols.

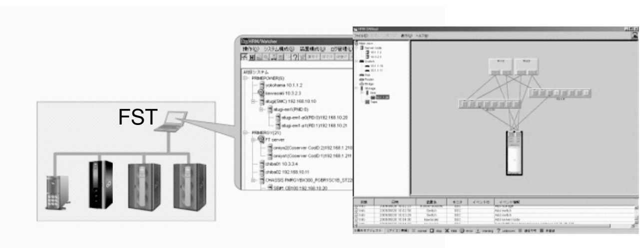

Figure 6
System configuration view of HRM.

6. Conclusion

As described above, Fujitsu has developed technologies for supporting the design verification, device evaluation and maintenance of various types of information-communication equipment such as servers and ubiquitous devices. Now that mobile networks are expected to expand in the future, we will focus on TMP development for high-speed wireless network-related devices. As Fujitsu continues to employ more procured products such as CPUs, memory, and HDDs, we should adopt more sophisticated evaluation technologies in both a logical and physical manner. In this way, we should continue to provide high-quality and reliable products to customers.

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