Power Noise Analysis of Large-Scale Printed Circuit Boards

● Toshiro Sato ● Hiroyuki Adachi

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Recent increases in digital-equipment operation frequency and decreases in LSI supply voltage have caused various noise problems relative to LSI, packages (PKG), system in package (SIP), and printed circuit boards (PCBs). These problems entail power-and-ground bounce noise, simultaneous switching noise, and EMI noise. Solving these problems requires a long development period and high costs. The authors have developed a new power noise analysis system as a computer-aided design (CAD) system, and applied it to equipment design. This system optimizes noise countermeasure design by performing large-scale simulation to unify the LSI and PCB design for all stages from the upper stage to the verification stage of final design. We confirmed that this system greatly reduced the time and cost of redesign necessary to solve noise problems. This paper introduces the features of this system, and describes the results of its application to high-end servers.

1. Introduction

The operation frequency of printed circuit boards (PCBs), multi-chip modules (MCM), and system in package (SIP) used in such digital equipment as high-performance, high-end servers has recently increased. The integration density of LSI used for the PCB, MCM, and SIP has been dramatically increased to acquire higher levels of performance and functions by adopting the latest process miniaturization technology. Such development tends to significantly increase LSI consumption current. To suppress the power consumption caused by increases in operation frequency and consumption current, the LSI voltage must be reduced. For this reason, LSI design in recently years has reduced LSI voltage; however, it posed another problem. Given the lower LSI voltage, recent digital equipment is subject to being affected by power-and-ground bounce noise[note 1)] due to time serial changes in consumption current caused by LSI operation, as well as simultaneous switching noise and noise caused by return current. This makes it very difficult to design digital equipment not influenced by such noise when employing a noise countermeasure design method based on conventional calculation formulas and theoretical expressions. Moreover, recent designs to reduce excessive noise have increased the cost of noise countermeasure design, and apparent noise problems caused by inadequate noise countermeasure design in recent years cannot be ignored.

Addressing these problems through LSI

note 1) Voltage noise detected in the power and ground terminals of elements due to time serial changes in the consumption current of LSI mounted on PCBs.

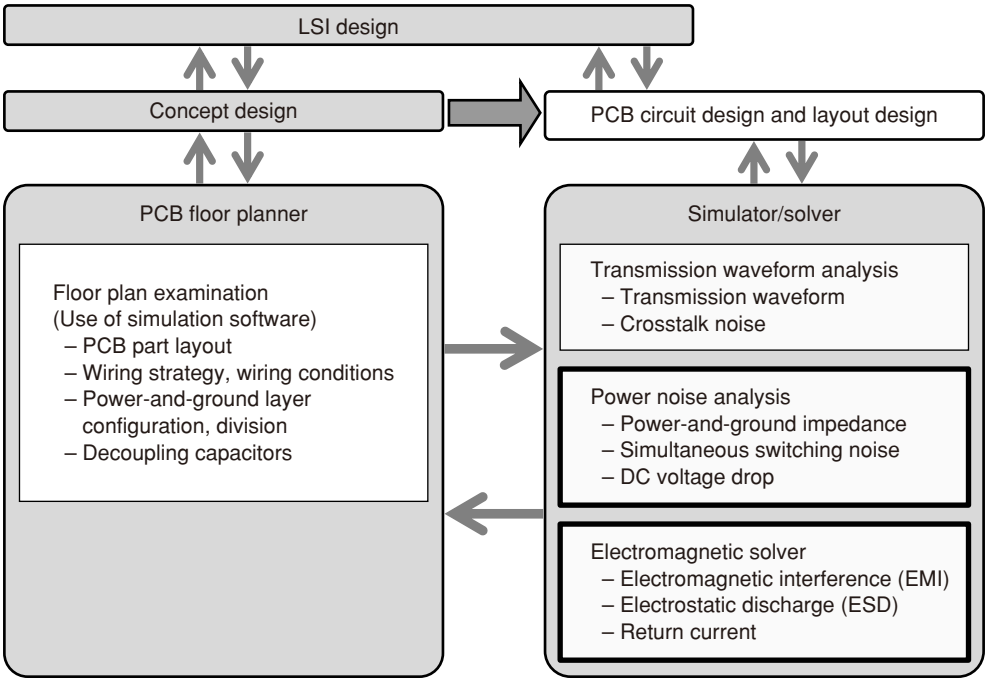


Figure 1
Configuration of power noise analysis system.

design free from the influence of power-and-ground bounce noise and simultaneous switching noise necessitates a new noise countermeasure design method using higher-level simulation for precise solutions.

The authors developed a new power noise analysis system as a computer-aided design (CAD) system and applied it to layout design. This system provides optimal noise countermeasure design by conducting large-scale power noise analysis for unified LSI, packages (PKG), MCM, SIP, and PCB models for all stages from the upper stage to the verification stage of final design. This system significantly reduced the time and cost of redesign necessary to solve noise problems. This paper introduces the features of this system, specifically the mechanism of large-scale noise analysis, describes the noise countermeasure design in the upper stage by using the floor planning tool,[note 2)] and discusses the results of applying this analysis system to high-end servers.

2. Configuration and processing flow of power noise analysis system

The authors independently developed a new noise analysis system[1)] that can be easily used by linking with various CAD tools in all stages from the upper stage to the verification stage of final design (**Figure 1**). This system effectively shortens the development period, improves product quality, and reduces cost. The functions for executing power noise analy-

note 2) CAD tool used to analyze the element layout on PCBs, inter-element wiring routes and layout, and power-supply-system design conditions in the upper stage of design.

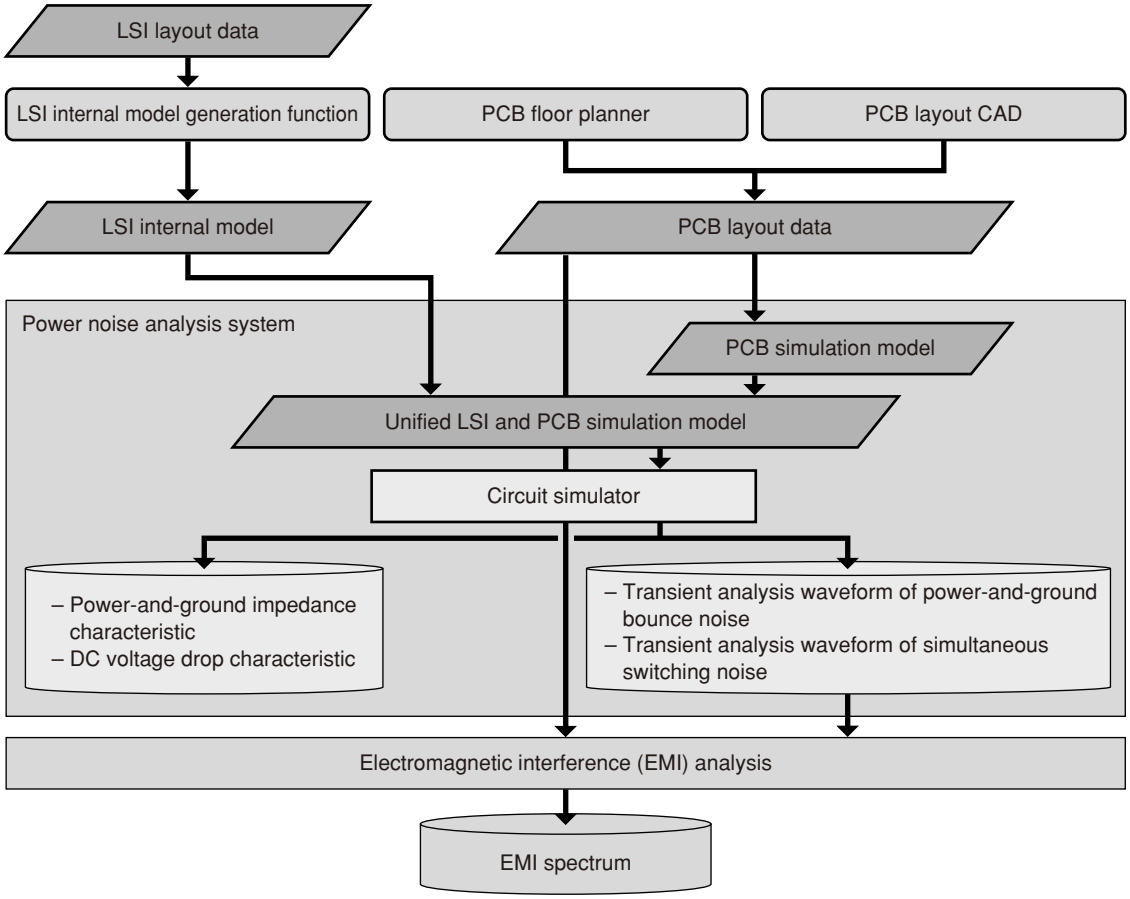


Figure 2
Flow of power noise analysis.

sis are built into this system, and supplied to in-company users. This system utilizes the PCB floor planner that creates a rough element layout and examines the wiring routes in the initial PCB design stage. The user of this system can utilize various analysis tools to efficiently determine an optimal PCB specification plan and design restriction conditions by considering signal integrity,[note 3)] power-and-ground bounce noise, and electromagnetic interference (EMI). Then the determined design restriction conditions are passed to the PCB circuit design and layout design processes so that actual design is performed under these conditions. Finally, the completed PCB design can also be analyzed by using these analysis tools to resolve all noise-related problems.

Figure 2 shows the processing flow of power noise analysis using this system for the unified LSI and PCB model. Data linkage between sub-units and processing flow are performed as follows: First, the PCB floor planner or PCB layout CAD generates PCB layout data for input into the power noise analysis system. The power noise analysis system then generates a PCB simulation model based on the PCB layout data. At the same time, the LSI internal model generation function reads LSI layout data to generate an LSI internal model, and inputs the generated model to the power noise analysis system. Next, the power noise analysis system

note 3) Correct digital signal transmission with high transmission waveform quality and correct timing.

combines the LSI internal model with the PCB simulation model to generate a unified LSI and PCB simulation model. The circuit simulator then analyzes the unified LSI and PCB simulation model, and outputs the power-and-ground impedance characteristic and transient analysis waveforms of simultaneous switching noise and power-and-ground bounce noise. The processing above is fully automated so that even logic designers, system designers, and layout designers not possessing sufficient technical knowledge about the circuit simulator can easily use this noise analysis system.

Next, the transient analysis waveforms of power-and-ground bounce noise from the power noise analysis system can be input to the EMI analysis system for analyzing the electric-wave radiation (EMI spectrum) of the unified LSI and PCB model.

3. Detailed analysis functions of power noise analysis system

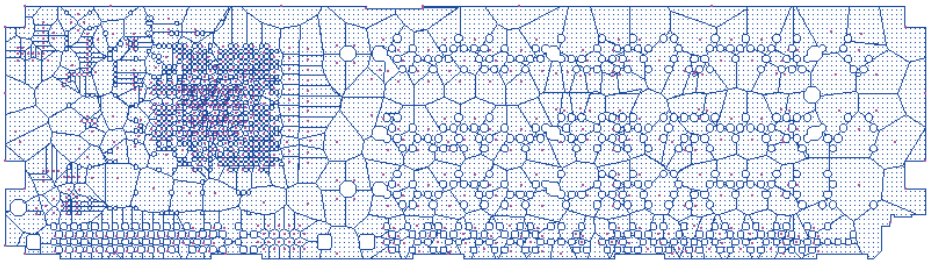
This section describes power-and-ground impedance analysis, DC voltage drop analysis, unified LSI and PCB power noise analysis, and large-scale parallel electromagnetic analysis in detail.

3.1 Power-and-ground impedance analysis and DC voltage drop analysis

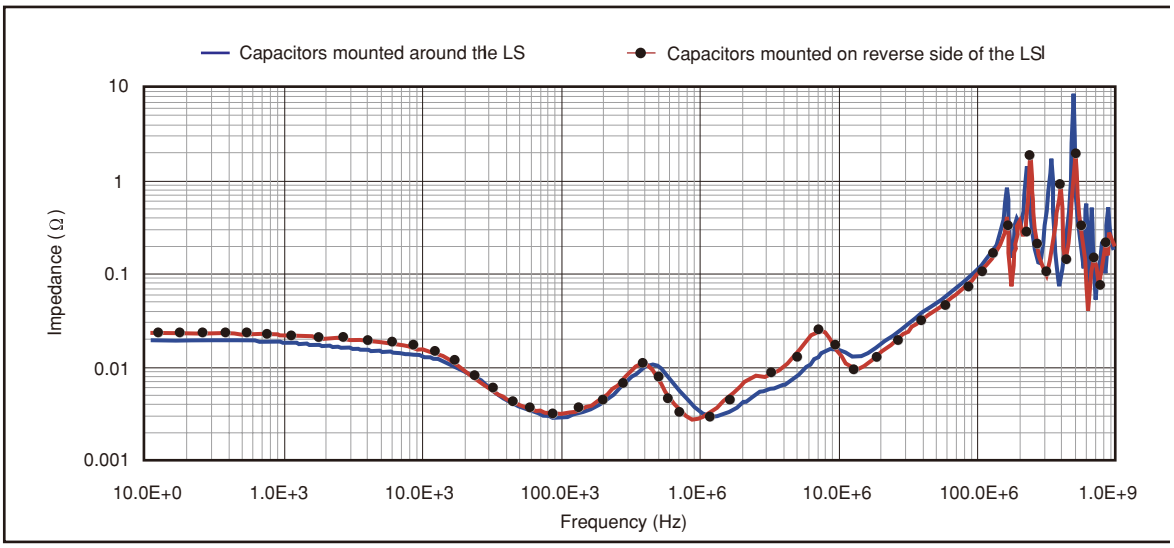
This system is used to examine conditions of the decoupling capacitor[note 4)] layout on PCBs developed by Fujitsu. Specifically, it allows designers to easily and efficiently examine power noise problems using the PCB CAD design data. **Figure 3** shows an example of the power-and-ground impedance analysis of a PCB. Figure 3 (a) shows a mesh model that was automatically generated from the PCB layout data. In this example, the capacitor layout that affects power-and-ground impedance is examined; that is, the characteristic acquired when capacitors are mounted around the LSI is compared with that acquired when the capacitors are mounted on the reverse side of the LSI. The power-and-ground impedance acquired when capacitors were mounted around the LSI was confirmed as being significantly lower (in a frequency range of 1 to 10 MHz) than the characteristic acquired when the capacitors were mounted on the reverse side of the LSI [Figure 3 (b)]. Based on these examination results, the occurrence of power-and-ground noise can be minimized at the design stage. In this example, the LSI is mounted on the left side of the PCB, with high mesh density just below the LSI and around the LSI, but low in other areas. The mesh density is high in the part where current is concentrated and low in other parts. This reduces the number of meshes without adversely affecting analysis precision, and also reduces the number of resistance-inductance-capacitance (RLC) element models proportional to the number of meshes. This enlarges the scale of analysis and shortens the calculation time. As a result, the entire area of a PCB, including large-scale PCBs for high-end servers, can be analyzed. This analysis method allows the correct mounting conditions of decoupling capacitors to be determined at the design stage, and consequently reduces the time and cost of redesign required to prevent power-and-ground noise, simultaneous switching noise, and drops in DC voltage. **Figure 4** shows an example of analyzing the DC voltage drop distribution of a PCB for high-end servers. Given the high power current of the element shown within the dashed-line circle in this example, it was feared that a serious drop in DC voltage might occur around the LSI. However, since the DC voltage drop distribution was visualized, the power supply system design could be easily improved. This made it possible to suppress the drop in DC voltage within the allowable range at the design stage.

As described in the previous section,

note 4) Capacitors mounted on a PCB, used to connect the power line to the ground line for reducing power-and-ground bounce noise.



(a) PCB mesh model



(b) Analysis results of power-and-ground impedance

Figure 3
Example of power-and-ground impedance analysis.

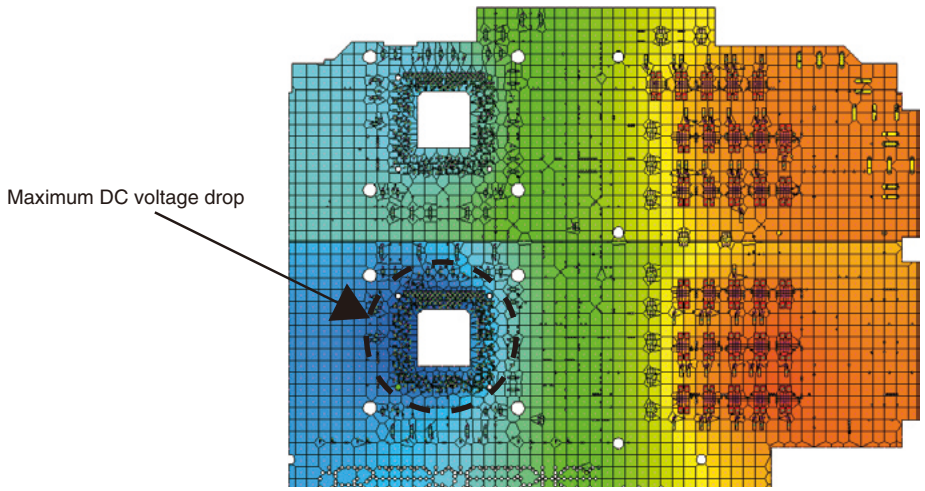


Figure 4
Results of DC voltage drop analysis.

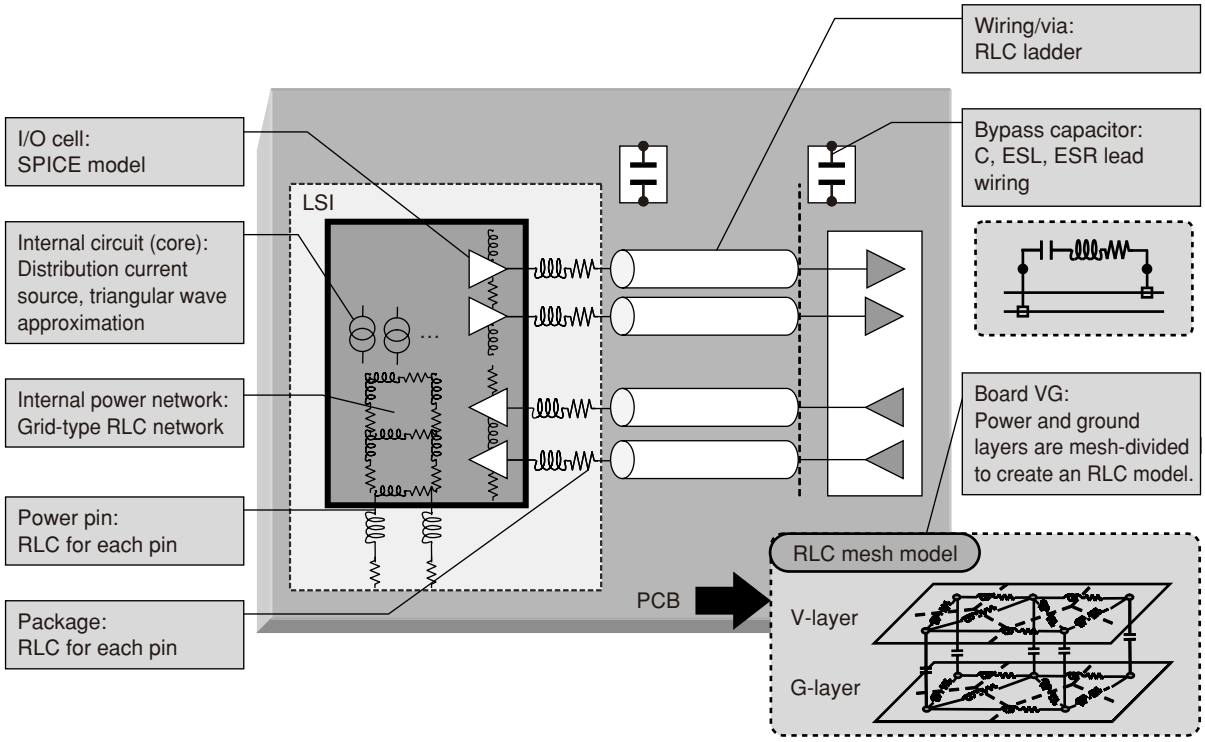


Figure 5
Configuration of the unified LSI and PCB analysis model.

implementing a power-and-ground noise countermeasure at the upper stage of design is very effective in reducing the time and cost of redesign. The mounting conditions of decoupling capacitors can thus be determined at the upper stage of PCB design by using the CAD tool supplied for simplified floor planning examination. Applying these determined mounting conditions to the design greatly reduces the time and cost of redesign required to solve noise occurrence problems in the later analysis process.[1),2)]

3.2 Unified LSI and PCB power noise analysis

Figure 5 shows the configuration of the unified LSI and PCB noise analysis model. The PCB power-and-ground pattern section is modeled by using the Partial Element Equivalent Circuit (PEEC) method using an RLC mesh model. The inter-LSI wiring is modeled as the transmission wiring.[3)-7)] The power-and-ground pattern in the LSI is represented by an RLC mesh model and the I/O circuit model by a SPICE model.[note 5)] The power current in the LSI core is modeled so that the power current in each cell of the LSI is represented by a current source and distributed.[8),9)] The unified LSI and PCB simulation model is then configured by interconnecting all these models. By using the circuit simulator to analyze this unified model, the transient waveforms of simultaneous switching noise and power-and-ground bounce noise can be acquired. Fujitsu and other companies have applied this function to analyzing many types of digital equipment containing Fujitsu's LSI, resulting in effective noise reduction and largely resolving

note 5) Circuit element model described with a transistor model devised for the simulation program with integrated circuit emphasis (SPICE).

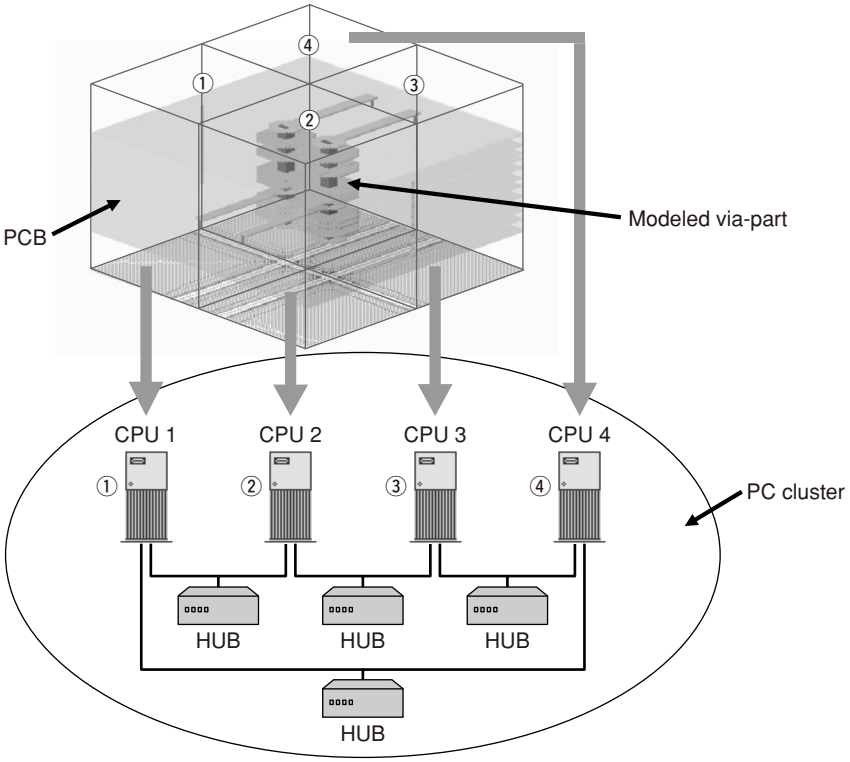


Figure 6
Large-scale parallel electromagnetic field analysis system using PC cluster.

timing problems.

3.3 Large-scale parallel electromagnetic analysis

When utilizing the PEEC analysis method described in the previous section, the level of the approximation method employing PCB modeling is generally known to affect analysis precision. This effect cannot be ignored in high-end servers or devices developed with advanced, large-scale, high-speed, and high-precision production technologies. To address this problem, the high-precision, full-wave electromagnetic analysis method[note 6)] that accurately analyzes an electromagnetic field by using Maxwell's formula must be used together with the PEEC analysis method. Fujitsu developed a parallel analysis environment using a PC cluster (**Figure 6**) to enable the analysis of a large-scale PCB. In this system, electromagnetic solvers using the finite difference time domain (FDTD) method are operated in parallel on the PC cluster having high-speed network connections. As shown in Figure 6, the space to be analyzed is divided into four parts (①-④), with each part assigned to one PC and calculated. Respective PCs exchange operation data via a high-speed network. As a result, a large-scale electromagnetic field can be analyzed at high speed.

Figure 7 is a partly enlarged view of an example of analyzing a large-scale PCB used in Fujitsu's high-end server equipment. We confirmed that return current bypassing upon the simultaneous switching of bus signals at the lower side in this figure caused control signal

note 6) Method of accurately analyzing electromagnetic phenomena by using Maxwell's formula without approximation.

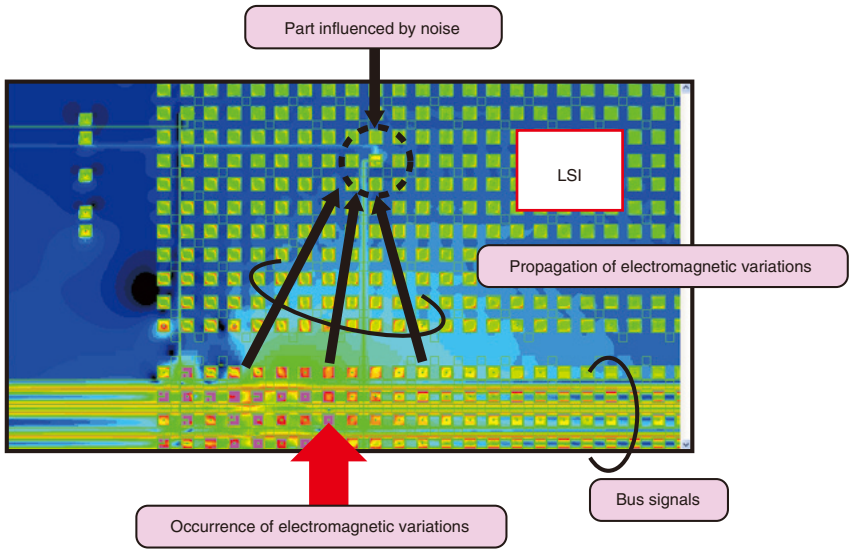


Figure 7
Return current simulated by large-scale parallel electromagnetic field analysis.

noise. Based on these analysis results, we could create a countermeasure design beforehand at the product design stage.

4. Conclusion

This paper described the power noise analysis CAD system developed by Fujitsu. This paper also described its application to high-end servers and explained its effects. In the future, the operation frequency of digital equipment will be further increased, along with a trend towards reduced voltage and higher integration density. Designing appropriate noise countermeasures under these conditions entails improved precision and a shorter calculation time. To address these problems, we will develop new analysis technologies and continue to advance the application of such technologies.

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Toshiro Sato, *Fujitsu Ltd.*
Mr. Sato received the B.S. degree in Electronics Engineering from Chiba University, Chiba, Japan in 1979 and the M.S. degree in Physical Information Engineering from Tokyo Institute of Technology, Tokyo, Japan in 1982. He joined Fujitsu Ltd., Kawasaki, Japan in 1982, where he had been engaged in development of circuit technology for high-performance mainframe computers. Since 1995, he has been engaged in research and development of noise countermeasure design systems. He is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan and the Japan Institute of Electronics Packaging.

Hiroyuki Adachi, *Fujitsu Ltd.*
Mr. Adachi received the B.S. degree in Electric Properties of Materials from Tokyo Institute of Technology, Tokyo, Japan in 1982. He joined Fujitsu Ltd., Kawasaki, Japan in 1982, where he has been engaged in research and development of high-speed, low-power technology for high-end servers, focusing on high-speed I/O macros.