New Ferroelectric Material for Embedded FRAM LSIs

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The strong growth of information network infrastructures in our society has enabled personal authentication services for electronic money systems and ticketless transportation services to become firmly established. Secure, high-speed, and low power consumption nonvolatile memories will be required for mobile devices used with smart RFID tags and secure IC cards. Ferroelectric random access memory (FRAM) is one of the best choices for these applications. Market needs must be paid attention for these mobile and secure applications. In FRAM research and development, we pursue scalability for increased memory capacity, unlimited read/write cycles, and a wider range of operating voltage, as well as to improve the conventional features of FRAM, we introduce a new ferroelectric material that will enable us to fabricate FRAM in a 90-nm technology node and beyond, by focusing on its superior characteristics. We also describe our plans to commercially produce FRAM devices in the near future.

1. Introduction

The Internet is being rapidly and widely spread on business and off business on our daily activities. The growth of information network infrastructures has enabled the firm establishment of personal authentication services for electronic money systems and ticketless transportation services. Secure and high-speed nonvolatile memories with low power consumption will be required for mobile devices used with smart RFID tags and secure IC cards, which contain IC chips with contactless read and write operations. For such applications, ferroelectric random access memory (FRAM)[note 1)] represents one of the best choices.

Fujitsu began mass-producing FRAM in 1999 and has shipped more than 500 million chips up to May, 2007. FRAM is completely new devices on principles of operation, compared with the conventional nonvolatile memories such as EEPROM and flash memory. Therefore, FRAM has a capability to create a new market, in addition to expanding the market for replacing existing products.

We have to pay attention to the market needs for the mobile and secure application. In FRAM development, we pursue scalability for increased memory capacity, unlimited read/write cycles, and a wider range of operating voltage, as well as to improve the existing features of FRAM.

We introduce a new ferroelectric material that will enable us to fabricate FRAM in a 90-nm technology node and beyond, by focusing on its superior characteristics. We also describe our plans to commercially produce FRAM devices in the near future.

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note 1) FRAM (also called FeRAM) devices are nonvolatile memories based on an electrical polarization phenomenon (whereby a charge is retained even without an externally applied voltage). FRAM uses a ferroelectric material to hold data.

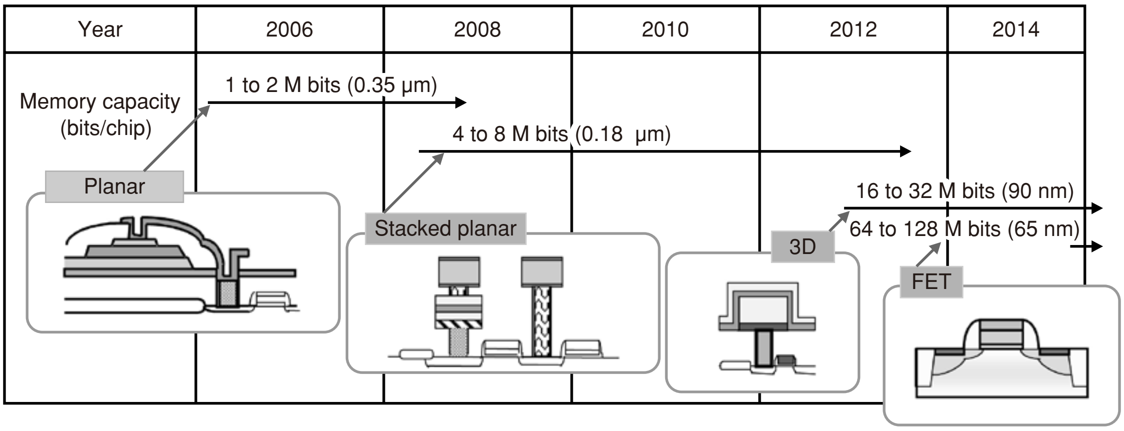

Figure 1
FRAM technology roadmap.

Science and Technology commissioned the Tokyo Institute of Technology (Tokyo-Tech) to conduct part of this technological research based on funding to promote science and technology. This paper looks at the achievements of joint research conducted between the Tokyo Institute of Technology and Fujitsu Laboratories Ltd. based on industry-university research collaborative partnership.[1)]

2. FRAM technology

2.1 Policy of FRAM technology development

Fujitsu began mass-production of FRAM in 1999 using a 0.5-µm technology node and currently manufactures 2 Mbit FRAM using a 0.35-µm technology node.[2)] Given its ideal memory properties, such as very low power consumption and high-speed read/write performance, FRAM has been applied to LSIs for IC cards, RFID tags, smart cards, and for alternate memory addressing with battery backup.

To further expand FRAM applications, it is essential to develop technology for increasing memory capacity, reducing operating voltage, and increasing the read/write cycles. It is also necessary to develop services and applications made possible only by using FRAM and the related underlying systems. The actualization of 90-nm FRAM technology through integration technology will enable increased memory capacity and significantly reduced operating voltage, and allow the reuse of an abundant design library already developed for logic LSIs. This will lead to shorter development periods and deadlines for FRAM-embedded devices, and allow us to promptly release products.

2.2 Progress of FRAM technology in material and structure

When we began mass-production of FRAM, the process was based on the 0.5-µm technology node. The technology was then scaled down to 0.35-µm and is currently at 0.18-µm generation.[3),4)] **Figure 1** shows the FRAM technology roadmap. It is assumed that the full extent of integration will be reached using the existing material and structure by 2009 or shortly thereafter. The existing ferroelectric capacitor — Pb (Zr,Ti) O_3 (PZT) — is limited regarding its remanent polarization (Qsw).[note 2)] A planar stack struc-

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note 2) Qsw is the charge equivalent to twice the remanent polarization Pr (the electric charge when applied voltage is removed).

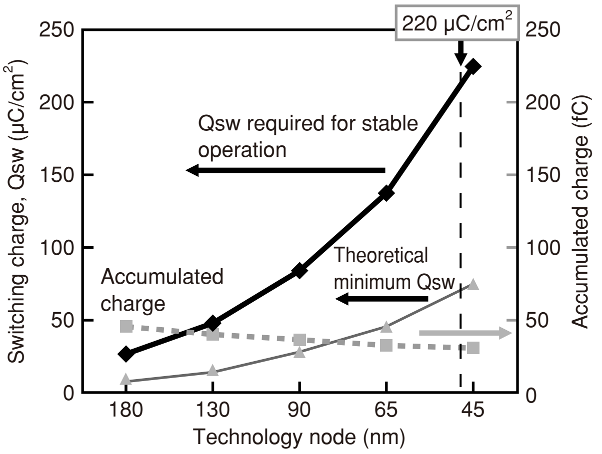

Figure 2
Qsw required for stable operation of 1T1C FRAM in stacked planar capacitor.

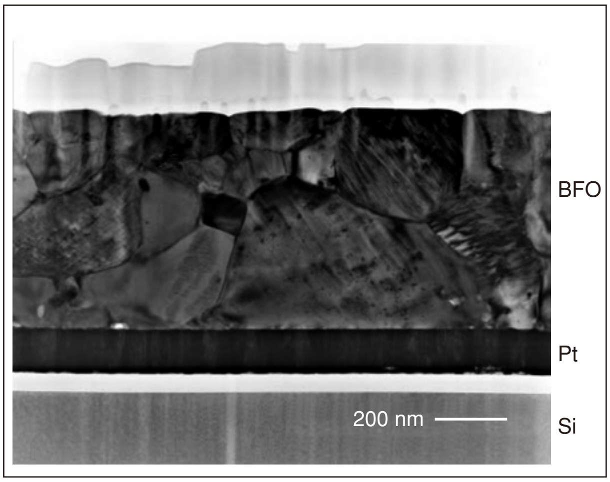

Figure 3
Cross-sectional TEM image of Mn-doped BFO layer on Pt layer.

tured 1T1C (1 Transistor/1 Capacitor) FRAM is considered to have a lower limit at 0.13 µm with regard to scalability. **Figure 2** shows the Qsw required for stable operation of five generations of 1T1C FRAM with a planar stack capacitor. For instance, the Qsw required for stable operation using a 90-nm technology node is estimated to be 84 µC/cm². Although the PZT material has a larger Qsw value, fabrication through the semiconductor process restricts FRAM to a maximum of 40 µC/cm². Therefore, a breakthrough is necessary to fabricate FRAM based on the 90-nm technology node using PZT.

One method of overcoming the Qsw limit regarding PZT is to expand the surface area by assembling a capacitor into a 3D structure. However, unlike dynamic random access memory (DRAM) having a similar structure, in FRAM, a ferroelectric layer forming a capacitor must be crystals oriented in the same direction and not amorphous. The 3D pattern requires a ferroelectric crystal layer on the side walls as well as on the bottom surface. While it is possible to expand the surface area, obtaining the required Qsw may prove extremely challenging because it is difficult to arrange the crystal orientation completely.

While FRAM with an FET-type capacitor enables a further reduction in cell dimensions and offers the advantage of low-voltage operation, there are currently many problems regarding the development of the required material and process technology. Since such development is predicted in a long range, practical use of such FRAM using a 65-nm technology node and beyond is expected.

3. Characteristics of Mn-doped BFO

We have successfully developed a new ferroelectric material for a 90-nm technology node and beyond that consists of 5% Mn-doped BFO ($BiFeO_3$, bismuth ferrite).[5] We substituted some of the Fe ions with Mn ions to decrease the leakage current in the BFO film at room temperature and increase the withstand voltage. Our experimental results revealed that 5% Mn-doping to BFO achieves a Qsw value of 180 to 220 µC/cm², which is five times larger than that of PZT. The leakage current due to reduced hopping conduction by the electron of Fe ions was suppressed by adding Mn ions having a larger number of valence than Fe ions and substituting part of the Fe ions. As a result, we obtained the large Qsw in the original nature of BFO.[6],[7] **Figure 3** shows a cross-sectional TEM image

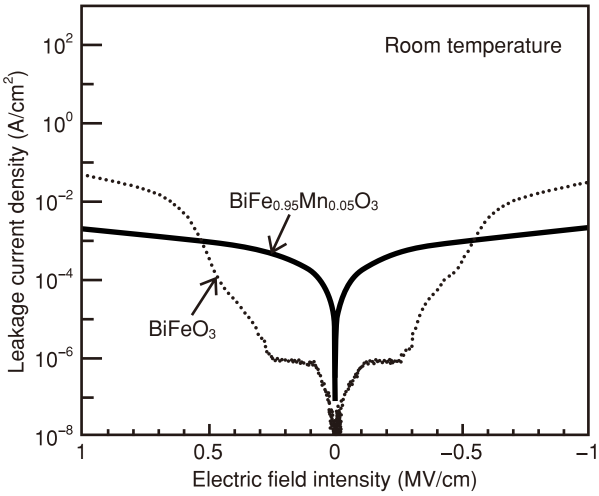

Figure 4
Dependence of leakage current density on applied electric field in Mn-doped BFO.

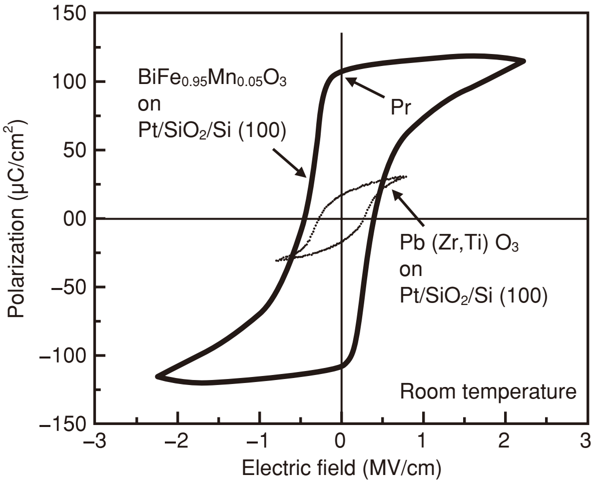

Figure 5
Hysteresis characteristics in Mn-doped BFO.

of the Mn-doped BFO layer prepared by the sol-gel/spin-coating method that is used to form a BFO thin film with thickness of 400 nm.

Figure 4 shows the dependence of the leakage current density on the applied electric field in a Mn-doped BFO at room temperature. The leakage current in Mn-undoped BFO film at electric field up to about 0.25 MV/cm is low, but increases abruptly above 0.25 MV/cm. The effect of Mn addition results in a moderate increase in current in the low electric field region of less than 0.5 MV/cm. The withstand voltage in the film is also improved, and the current at electric field up to about 1 MV/cm exhibits a gradual increase.

Figure 5 shows the remanent polarization (Pr = Qsw/2) versus electric field in a 5% Mn-doped BFO at room temperature. Due to its high leakage current, the hysteresis characteristics of undoped BFO could not be obtained at room temperature. Mn-doped BFO shows a square-shaped hysteresis at room temperature, however, as well as a high Qsw of 220 μC/cm^2. Mn-doped BFO has a sufficient Qsw for stable operation in consideration of 65-nm FRAM technology node, except difficulty to achieve polarization reversal (coercive electric field, Vc[note 3)]) with the comparatively low voltage applied in 65-nm generation circuits due to the high Vc of current BFO films.

In addition, the relative dielectric constant of BFO is one-fourth that of the conventional ferroelectric material like PZT, and its Curie temperature[note 4)] is 800°C, which is more than double that of the conventional material. These properties advance high-speed read/write and high-temperature operation, and indicate the potential for developing FRAM applications on a much wider scale.

4. Future issues

Mn-doped BFO shows a large Qsw of 180 to 220 μC/cm^2 and exhibits a low leakage current level of 1×10^{-4} A/cm^2 at room temperature. These characteristics make its application to 1T1C planar capacitor structured FRAM up to the 65-nm generation possible. Characteristics

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note 3) Voltage applied to remove the residual surface charge of a ferroelectric material.

note 4) The Curie temperature is the temperature at which polarization is not caused by changes in the atomic configuration of a ferroelectric material. FRAM loses its nonvolatility at and above the Curie temperature.

such as the Qsw and leakage current, however, have only reached an acceptable level and simply represent the baseline characteristics at the material and property levels. To commercialize FRAM using BFO, the following problems should be solved:

1) Reduction of Vc

FRAM using a 90-nm technology node and beyond requires an operating voltage of less than 1.2 V. To reverse polarization with this voltage, we must enhance the electric field intensity by reducing the thickness of the ferroelectric layer, improve the characteristics of coercive electric field, and reduce the Vc of the BFO.

2) Low temperature deposition

The lower-limit of BFO film deposition temperature is determined by the crystallization temperature of the BFO film, and is about 600 °C. To fabricate FRAM using a 90-nm technology node and beyond, we need to lower the temperature of film deposition by, for example, improving the sol-gel solution or adding a dopant other than Mn.

3) Selection of passivation film to prevent Fe diffusion

Fe is considered an undesirable element in the silicon process because it rapidly diffuses into silicon substrates. Therefore, the ferroelectric oxide layers are covered with passivation films for protection to avoid the deoxidation by hydrogen from invading during the fabrication process. This passivation film also has to prevent the diffusion of Fe.

We have been developing technologies to find solutions to these problems. Moreover, we have been promoting research and development for fabricating FRAM using BFO materials. It is additionally important to find a deposition method for mass production, other than the sol-gel method, as well as to develop an oxide electrode material that prevents the degradation of properties.

5. Conclusion

This paper described our newly developed Mn-doped BFO that enables us to fabricate FRAM in a 65-nm technology node with a device structure similar to that of FRAM being produced using 0.18-µm technology. This new material is expected to enable fabrication using a 90-nm technology node and beyond and a large memory capacity up to 2014. With further development of BFO, FRAM having capacities exceeding 256 M bits and a memory cell capacity that is two orders of magnitude higher than the current capacity of 1 M bits can be realized in the future. These higher capacities will allow FRAM to be used in hybrid HDDs for computers, storage caches, electronic paper devices, and document viewers that let users store and browse information that is traditionally written on plain paper, as well as in IC cards. Moreover, we expect to significantly help reduce the power consumption of electronic devices. In the future, we will establish a BFO material and process technology for embedded FRAM LSIs and work toward achieving the practical use of FRAM in a 90-nm technology node by 2011.

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