New Technology for High-Density LSI Mounting in Consumer Products

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The ongoing trend toward downsizing and the growing sophistication of electronic devices require increasingly higher LSI mounting densities. Flip-chip technology is used to mount LSIs without using wire and thus enables higher mounting densities than conventional mounting technology, which uses Au wire bonding. Fujitsu has developed a new high-density flip-chip mounting technology for use in consumer products to reduce size and improve performance. This paper describes the bump method, assembly process, reliability, and applications of this new technology. It also examines Fujitsu's efforts to develop an ultrasonic assembly technology that achieves high throughput and reduced cost.

1. Introduction

The ongoing trend toward downsizing and the growing multi-functionality of electronic devices in recent years require increasingly higher LSI mounting densities.

LSIs are conventionally directly connected to the printed circuit board (PCB) by bonding with gold wire 20 to 25 μm in diameter. Demands for higher-density mounting, however, have prompted a shift toward flip-chip technology, which enables LSIs to be mounted without using wire (**Figure 1**).

Fujitsu has developed a proprietary high-density flip-chip mounting technology for use in consumer products to reduce size and weight and to improve performance. New LSI packages and PCBs for flip-chip mounting have also been developed.[1),2)]

In this paper, we introduce a flip-chip mounting technology that was developed to achieve high-density mounting of LSIs in consumer products. We then describe the latest assembly technology that uses ultrasonic energy.

2. Flip-chip mounting technology

In this section, we introduce the flip-chip mounting structure and features, describe a general flip-chip mounting process, and then provide a comparison of mounting methods.

2.1 Flip-chip mounting structure and its advantages

In flip-chip mounting, the LSI chip is mounted facedown on the PCB. A non-conductive adhesive called the underfill is used to fill in the spaces between the LSI and PCB [**Figure 2(a)**]. The electrical connections are made by joining metal protrusions called bumps on the LSI's terminals to the PCB [**Figure 2(b)**].

The flip-chip mounting method has the following advantages compared to the conventional wire-bonding mounting method:

1) The mounting area can be reduced to just the area of the LSI chip because no area is required for connecting leads.
2) The high-frequency transmission characteristics of the connections are good because

they have a low inductance.

3) Because all the terminals are connected in one operation, the mounting throughput can be improved.

2.2 General flip-chip mounting process

Before mounting, the plating or wire-ball bump method is used to form bumps on the LSI's terminals. As shown in **Figure 3**, the bumps are formed (①), the LSI is mounted on the PCB (②), an underfill is used to fill in the gaps between the LSI and the PCB (③), and then the underfill is hardened (④).

In many cases, a process that supplies material for connecting the bumps to the PCB is added.

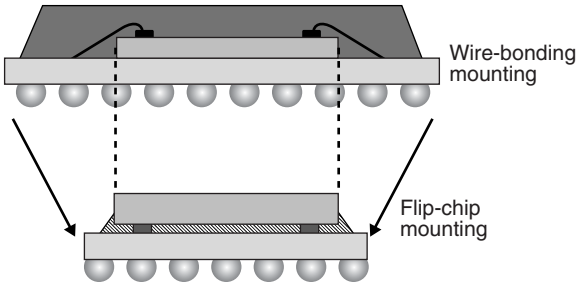

Figure 1
Comparison of wire-bonding and flip-chip mounting.

2.3 Comparison of flip-chip mounting methods

In flip-chip connection, the bumps are usually connected to the PCB using one of four methods (**Table 1**): 1) use of a conductive material (usually Ag paste); 2) use of an anisotropic conductive material and pressure contact; 3) use of solder deposited on the PCB; and 4) use of metallic joints made by ultrasonic welding.

Which of these methods is used depends on the product specifications and usage conditions.

3. Bump forming technology

Bump forming technology can be divided into two main categories: the wire-ball bump method and the plating method.[3)]

3.1 Wire-ball bump method

In this method, the bumps are formed using the normal wire bonding method (**Figure 4**). This method is easy to use, and no special processing such as adding a barrier metal layer (which is performed in the plating method) is required.

In the bump forming process, a high-voltage spark is used to melt the gold wire into a ball (①, ②); heat and ultrasonic energy are used to perform bonding via a tool called a capillary (③); and the gold wires are broken off, leaving bumps on the LSI (④, ⑤).

So far, we have established a high-precision

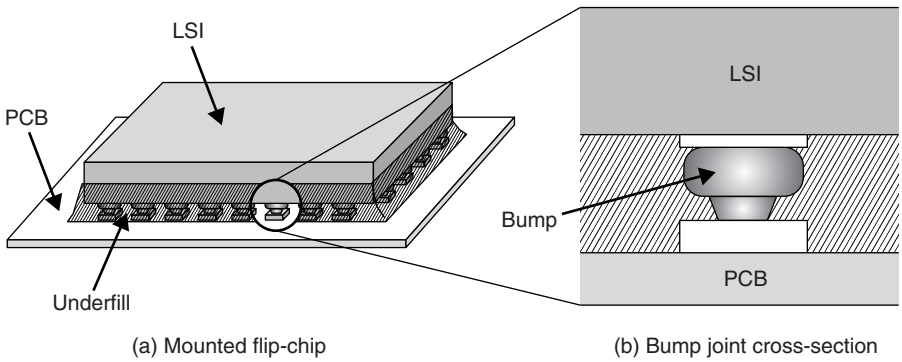

Figure 2
Flip-chip mounting structure.

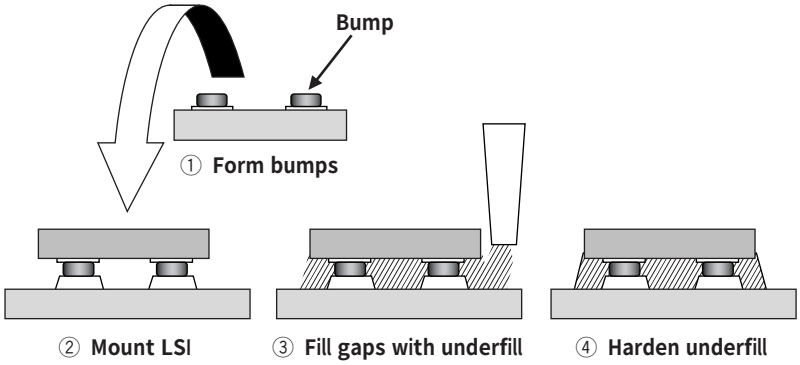

Figure 3
General flip-chip mounting process.

Table 1
Comparison of flip-chip mounting methods.

Mounting method	Bump joint structure	Fine pitch	Low cost	Multi-pin	Applicable products
Conductive material bonding	Conductive material	△	×	○	All ICs
Anisotropic conductive material bonding	Anisotropic conductive material	○	△	△	LCD driver ICs
Soldering	Solder	○	△	○	All ICs
Ultrasonic welding	Metallic joint	○	○	×	ICs such as SAW filters with only a few pins

○: Superior to other methods
△: Average level
Can be used for general products
×: Inferior to other methods
(Use is limited to applicable products.)

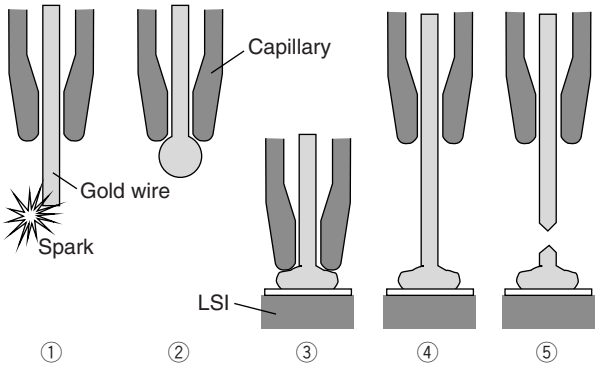

Figure 4
Wire-ball bump forming.

microwire bonding technology with a bump diameter of 25 ±2 μm and a bump placement precision of ±3 μm that is suitable for LSI electrode pitches as fine as 40 μm (**Figure 5**).

3.2 Plating method

There are two plating methods: electroplating and non-electroplating. Solder or gold is mainly used for the bump-forming material.

Fujitsu is on the verge of establishing a gold electroplating technology for forming bumps having pitches from 20 to 40 μm. The next step, which will be difficult, is to form flip-chip plating bumps at a pitch of 20 μm or less (**Figure 6**).

4. Pressure contact flip-chip mounting technology

In this section, we describe the mounting structure, features, mounting process, reliability, and some application examples of a pressure contact flip-chip mounting technology developed by Fujitsu. This mounting technology offers low costs, high universality, and high reliability when compared to general flip-chip mounting technologies.

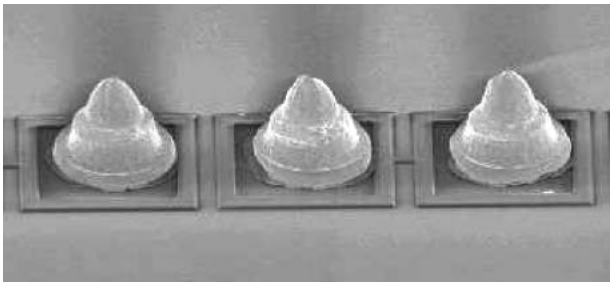

Figure 5
Photograph of wire-ball bumps.

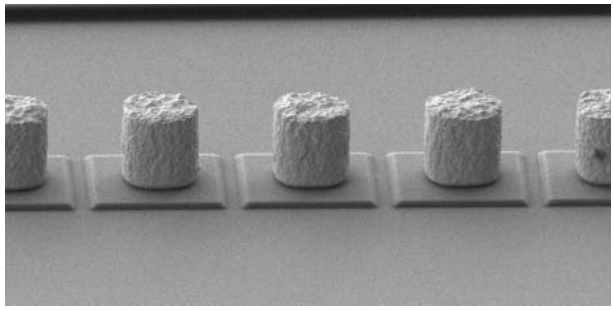

Figure 6
Photograph of plated bumps.

4.1 Pressure contact flip-chip mounting structure and features

The wire-ball bumps formed on the LSI terminals and the PCB are pressure contacted to make an electrical connection. The contractive force caused by the hardening of the underfill between the LSI and PCB increases the strength of the contacts (**Figure 7**).

With this mounting technology, no adhesive is required to connect the LSI bumps to the PCB. Pressure contact flip-chip technology, therefore, has the following advantages compared to general flip-chip mounting technology.

1) Costs are lowered because there is no adhesive or adhesive application process.
2) Because there is no conductive material around the bumps, a finer pitch is enabled.
3) Unlike in the normal mounting method, the underfill is applied to the PCB before the LSI is mounted. Therefore, less underfill escapes the underfill area and the mounting area can be reduced.

4.2 Pressure contact flip-chip mounting process

As shown in **Figure 8**, the wire-ball bumps are formed on the LSI terminals (①), the underfill for sealing is applied to the PCB (②), the LSI is positioned on the PCB (③), and then heat and pressure (200 to 240°C, 5 seconds, 0.1 to 0.7 N/bump) are applied to connect the LSI to the PCB (④).

4.3 Connection reliability

Some results of connection reliability tests performed on pressure contacted flip-chips are shown in **Table 2**. The following environmental tests were performed: temperature cycling (–55°C for 10 minutes, then 125°C for 10 minutes), high temperature (150°C), and high temperature plus high humidity (121°C, 85% RH). The test results show the connection reliability surpasses the required technical standards.

4.4 Application example

We have used this pressure contact flip-chip mounting technology to fabricate a multi-chip package (MCP) consisting of two LSI chips laminated together that have the same dimensions, which is difficult to do using conventional wire bonding (**Figure 9**).

Another example is the use of pressure contact flip-chip mounting technology to mount the sensor chips in CMOS image sensors. This flip-chip technology was used to produce the world's smallest sensor (7.0 × 7.8 mm) at that time.

5. Multi-pin ultrasonic flip-chip mounting technology

Ultrasonic flip-chip mounting enables an entire LSI to be connected in a single operation in less than 0.5 second, making it a very high throughput, low-cost mounting technology.

This technology is generally limited to LSIs having only several 10s of pins. We therefore

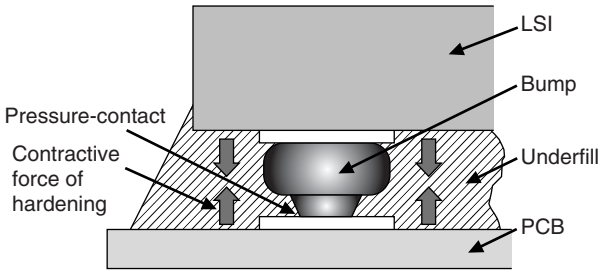

Figure 7
Cross-section of bump joint.

Table 2
Connection reliability of pressure-contact flip-chip mounting.

Test	Test conditions		Results
Temperature cycle	-55 to 125°C	800 cycles	OK
High temperature	150°C	504 h	OK
High temperature, high humidity	121°C, 85% RH	504 h	OK

Chip specifications: 6.1 × 6.1 × 0.2 mm, 294-pin, 70 µm pitch
Pre-processing conditions: 30°C, 80% RH, 5 days+4 days+4 days
Reflow temperature: 250°C

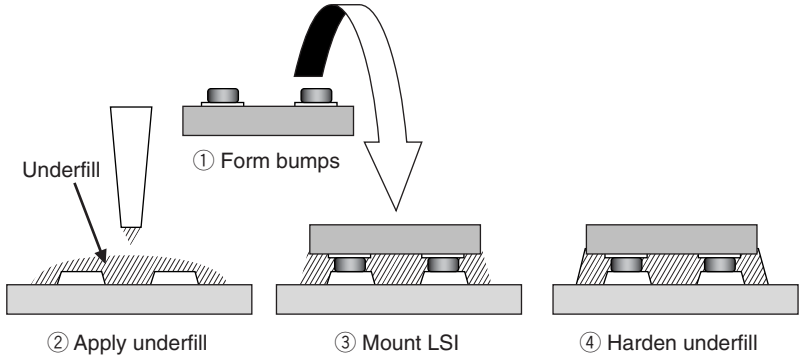

Figure 8
Pressure-contact flip-chip mounting.

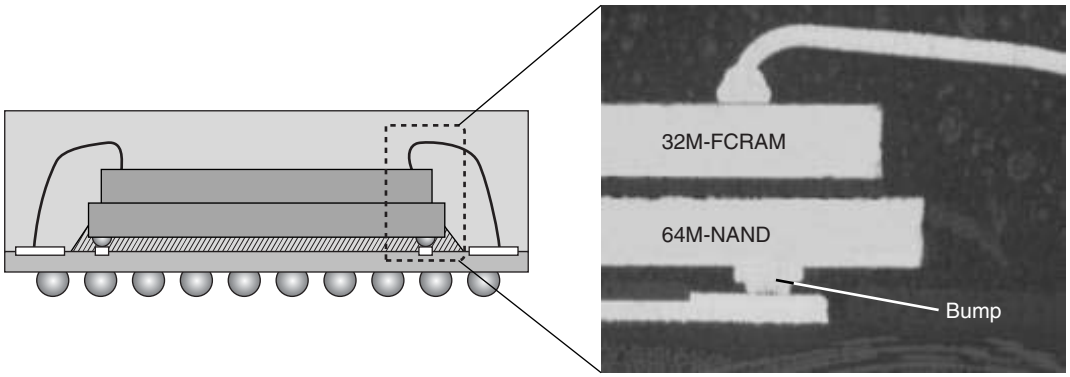

Figure 9
Cross-section of multi-chip package (MCP).

adapted it for application to LSIs having several 100s of pins.

In this section, we introduce this new ultrasonic flip-chip mounting technology.

5.1 Ultrasonic multi-pin flip-chip mounting structure and features

The structure is the same as that used to mount pressure flip-chips. With ultrasonic mounting, however, ultrasonic energy is used to create metallic joints between the LSI's wire-ball bumps and the PCB. This mounting technology has the following advantages.

1) Because no connective material is required between the LSI bumps and the PCB, this method has the highest throughput and lowest cost among the flip-chip mounting methods.
2) Because ultrasonic energy is used, low-temperature, low-load, fine-pitch mounting is enabled.
3) Because the joints between the bumps and PCB are metallic, the joint resistance is lower than in pressure contacted flip-chips.
4) Conventional ultrasonic flip-chip mounting can only mount LSIs of up to several millimeters square and having up to several 10s of pins. However, the technology developed by Fujitsu can mount LSIs of up to 12 millimeters square and having up to 500 pins.

5.2 Ultrasonic flip-chip mounting process

The ultrasonic flip-chip mounting process is the same as the general flip-chip mounting process (Figure 3), except that metallic joints are formed using ultrasonic energy (**Figure 10**). The LSI is vacuum-attached to an ultrasonic horn and aligned with the PCB (①). Then, the horn is lowered, a pressure of 0.05 to 0.2 N/bump is applied, and the ultrasonic horn applies ultrasonic energy with a peak-to-peak amplitude of 0.5 to 3 μm to weld the bumps to the PCB (②). Lastly, the vacuum is released and the ultrasonic horn is returned to the starting position (③).

After the LSI has been mounted, underfill is injected between the LSI and PCB and then hardened. As in the pressure contact flip-chip method, because the underfill is first applied to the PCB to enable the LSI to be mounted, this mounting method is very flexible.

This multi-pin ultrasonic flip-chip method visualizes the transmission of ultrasonic vibrations when LSIs are mounted (**Figure 11**), and by optimizing the ultrasonic wave generation profile and controlling the vibration of the PCB, it can accurately apply the ultrasonic energy to the bumps.

Moreover, by optimizing the process conditions such as the internal temperature and the specifications of the ultrasonic generator and other equipment, we achieved ultrasonic connection of LSIs having up to 500 pins.[4)]

5.3 Connection reliability

The results of connection reliability tests we conducted are shown in **Table 3**. The connection reliability level is the same as that for pressure contact flip-chip mounting and surpasses the required technical standards.

5.4 Next-generation flip-chip mounting technology initiatives

With the continuing development of fine-pitch LSI terminals and low-k (low-dielectric constant) materials, it is becoming increasingly necessary to develop low-load, low vibration amplitude technologies to reduce the mounting stress.

At Fujitsu, we have started developing a next-generation ultrasonic flip-chip mounting technology that raises the ultrasonic frequency from the conventional 50 kHz to 200 kHz.

So far, using 200 kHz, we have achieved a stress reduction of approximately 65% in the connections and about a 30% reduction in vibration amplitude (**Figure 12**). In addition, we performed a simulation that confirmed a reduction of 25 to 40% in the stress applied to the LSI

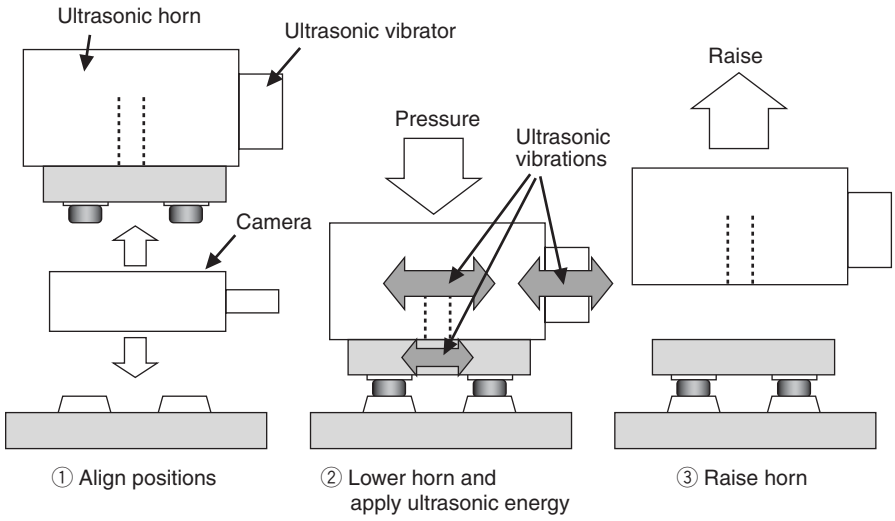

Figure 10
Ultrasonic flip-chip LSI mounting.

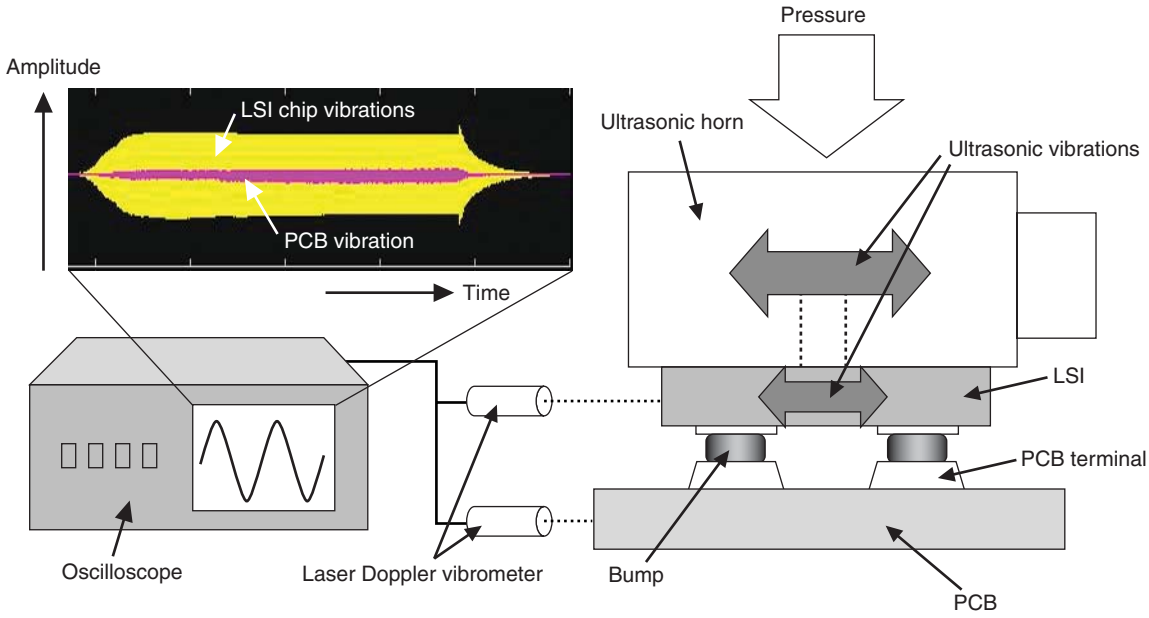

Figure 11
Visualization of ultrasonic vibration transmission when LSI is mounted.

Table 3
Connection reliability of ultrasonic flip-chip mounting.

Test	Test conditions		Results
Temperature cycle	-55 to 125°C	800 cycles	OK
High temperature	150°C	504 h	OK
High temperature, high humidity	121°C, 85% RH	504 h	OK

Chip specifications: 6.1 × 6.1 × 0.2 mm, 294-pin, 70 µm pitch
Pre-processing conditions: 30°C, 80% RH, 5 days+4 days+4 days
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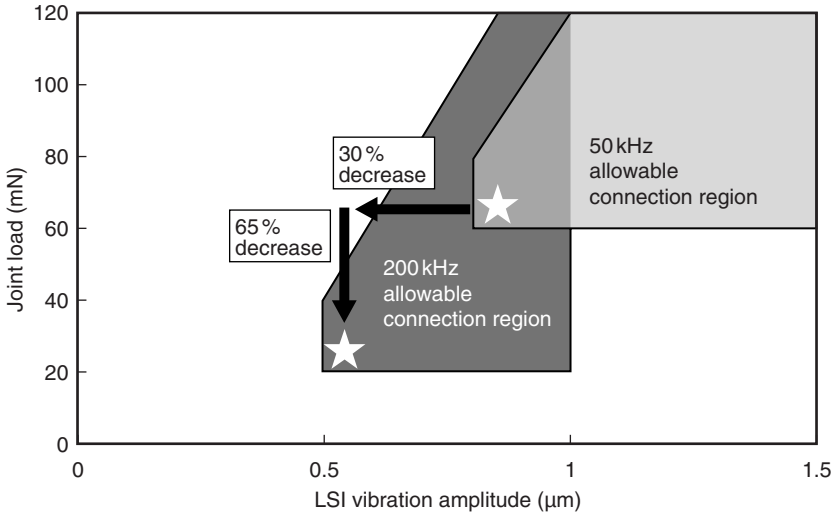

Figure 12
Allowable connection conditions for 50 kHz and 200 kHz vibration.

terminal pads when LSIs are mounted using a high vibration frequency of 200 kHz.[5)]

6. Conclusion

In this paper, we outlined the flip-chip mounting technology that Fujitsu has developed for consumer products and the latest mounting technology that uses ultrasonic energy.

In response to the increasing use of fine-pitch LSI elements and brittle low-k materials, we plan to use the ultrasonic flip-chip mounting technology we are developing as the basis for initiating development of new LSI mounting technologies.

In addition, we will further develop the ultrasonic connection technology that we cultivated for LSI mounting so it can be used in other fields such as the assembly of hard disk drives and strive to achieve further breakthroughs in micro-assembly technology.

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