LSI Noise Model for Power Integrity Analysis and Its Application

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Semiconductor scaling is making power integrity inside system-on-a-chips (SoCs) a major design issue. To investigate this issue, we developed an LSI noise model and simulation methodology to analyze power integrity. Using this methodology, we can simulate power supply noise inside an LSI, for example, the simultaneous switching noise of I/O circuits and core noise caused by dynamic switching currents. We can also use this model in the initial design stage to optimize the power wiring and minimize the power pin-count and thereby minimize the chip cost. In this paper, we first describe the noise that must be considered when designing an LSI's power system. We then describe the structure and generation flow of the LSI noise model, the measurement results of a test chip we used for verifying the model's accuracy, and the application of the model in product development.

1. Introduction

Progress in semiconductor scaling has enabled the performance and functionality of system-on-a-chips (SoCs) to be dramatically improved, and SoCs have become key devices in digital consumer products.

This scaling, however, has also brought a serious noise problem in SoCs. This problem, called the power integrity problem, is caused by two factors. Firstly, power supply noise induced by logic gates and simultaneous I/O switching is increasing due to the higher transistor and I/O count and the higher operating frequencies of modern technology. Secondly, to maintain the reliability of LSIs, their power supply voltage must be reduced. However, reducing the voltage also reduces the noise immunity because LSI operation is more sensitive to voltage fluctuations at lower power supply voltages, and malfunctions can easily occur unless these fluctuations are considered in the design phase. Because of these two factors, verification for noise problems and noise-reduction design methods have been recognized as major design issues among LSI and printed circuit board (PCB) designers.

In previous work, designers focused on solving problems caused by power supply noise. For example, experimental results have indicated that the maximum clock speed of an LSI depends on the amount of decoupling capacitance on the Si die.[1)] Other reports have described that electromagnetic interference (EMI) can be reduced when the amount of decoupling capacitance increases.[2)] Low-noise design methods must consider, for example, the I/O simultaneous switching noise (SSN), I/O delay penalty, and clock jitter. SoC designers must find a solution that meets all the customer requirements regarding these specifications.

Generally speaking, a power supply noise model consists of three parts: aggressors, noise propagating paths, and victims. When we developed the LSI noise model described in this paper, we focused on aggressors and noise propagating

paths. If both these parts are modeled properly, designers can easily find the origin of a noise problem and its effect on victims. As a result, they can find the most effective way to cope with the problem. An LSI noise model must include the properties of all noise sources inside the LSI and noise propagating paths so that every noise waveform can be simulated at the same time.

In this paper, we describe the noise that must be considered when designing an LSI. We then describe the overall configuration and generation flow of our LSI noise model and present measurement results for a test chip we used for verifying the model's accuracy. Finally, we describe the application of the model in product development.

2. Requirements for LSI noise model

An LSI noise model must include the following two types of noise in order to apply it to an LSI design.

1) Core logic switching noise
2) I/O switching noise

The first noise causes an instantaneous voltage drop on the power line, resulting in a logic malfunction or performance reduction. Moreover, when this noise enters the clock distribution network, clock jitter increases and the LSI's operating frequency must be lowered. We need to simulate this noise so we can estimate its influence on victims and then study how to deal with the problems it causes.

The second noise is caused by simultaneous switching of many I/O circuits and is called the SSN. SSN causes malfunctions in inter-LSI interfaces and adds a delay penalty by causing timing variations in I/O delays. The delay penalty caused by SSN must be considered when determining the timing window for switching in recent high-speed interfaces, for example, the interfaces for double-data-rate synchronous DRAM (DDR) and RAMBUS DRAM.

LSI noise models must be used not only for LSI design but also for PCB design. LSIs are major noise sources in PCBs (**Figure 1**). The noise induced by an LSI's switching current propagates into a PCB and then emits EMI that affects other equipment. LSI noise models must include an LSI's noise sources and parasitic components. There are various commercial tools that claim to simulate this noise propagation and emission, but without an accurate noise source model, their results are not sufficiently accurate. However, if PCB designers use simulation tools with an accurate LSI noise model, they can effectively suppress noise propagation and emission.

3. Structure of LSI noise model

Our LSI noise model is composed of three sub-models: the core logic model, I/O model, and package model (**Figure 2**).

3.1 Core logic model

If all the components of the core logic, for example, the metal wires and vias, are extracted accurately using a conventional method, it is well known there will be too many circuit elements for circuit simulators such as HSPICE to simulate. To overcome this problem, our new LSI noise model is based on power unit abstraction for the core logic circuit. The power unit model has three components: the power supply line network, a capacitor, and a current source. The power supply network is modeled as a two-dimensional series LR circuit. The capacitor represents the parasitic capacitances between the power and ground lines such as decoupling capacitances, non-switching gate capacitances, and junction capacitances within each power unit. The current source represents the switching behavior of the clock buffers, logic gates, and memories within each power unit.

The physical dimensions of the power unit depend on the noise sampling distance and are decided based on a trade-off between the simulation time and simulation accuracy. They are typically set from 100 × 100 to 200 × 200 μm^2. In the case of simulating noise frequencies up to

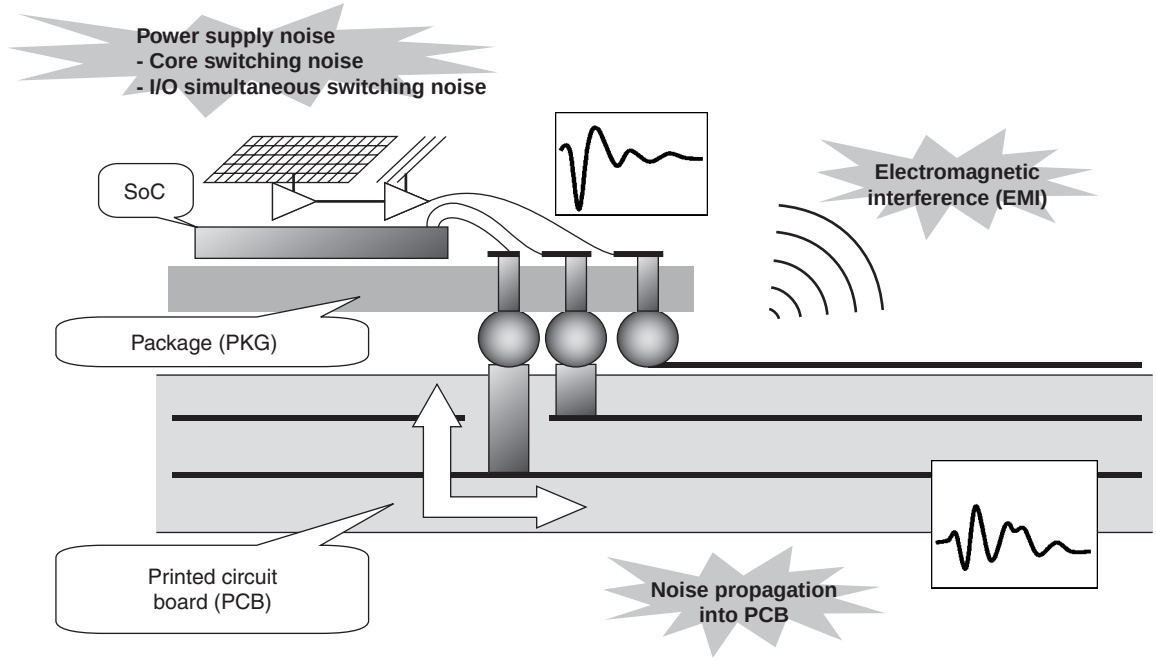


Figure 1
Behavior of LSI power noise.

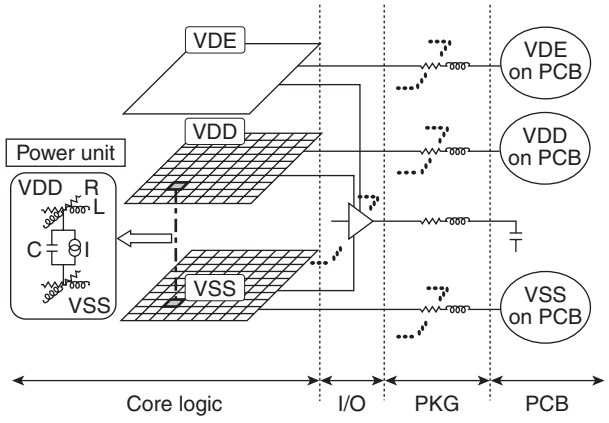


Figure 2
Structure of LSI noise model.

5 GHz, the wavelength of electromagnetic waves inside the LSI becomes 2 mm because the noise propagation speed is typically about 10 mm/ns due to the large capacitance of the LSI. Accurate noise simulation requires that the noise wavelength be divided into 10 phase zones, which gives a power unit size of 200 μm. By using this power unit abstraction, the model can be roughly 10^{-5} smaller than a conventional model.

3.2 I/O model

The I/O buffers are modeled in a different way from the core logic. Because crosstalk noise between the many I/O signal lines and between the signal and power lines can cause malfunctions, each I/O buffer must be modeled independently in order to simulate the effect of crosstalk noise.

We use a transistor-level netlist for the I/O cells because the number of I/O cells is not so large and the model size has less impact than that of the core logic. Macro models such as IBIS version 3.2 are not accurate enough for the LSI noise model because they do not include a model of the power line.

3.3 Package model

We used commercial tools for extracting the parameters of the package model. Each signal pin and power pin must be modeled separately because they must be consistent with the I/O model. The modeling of the mutual inductance and capacitance between pins depends on the trade-off between accuracy and simulation time.

4. LSI noise model generation and simulation flow

The generation and simulation flows of the LSI noise model are shown in **Figure 3**. The left side of this figure shows the estimation flow, which is mainly used in the early design stage. The LCRI value is created manually from the LSI specifications. The right side of this figure shows the verification flow, which is mainly used in the final design phase. The LCRI value is extracted from the final design data. We have developed an extraction tool called paragraph. In both the estimation and verification stages, the LCRI values are fed into the PI_ANALYSIS netlist formation tool, and then the LSI noise model is generated. The LSI noise model is simulated with a circuit simulator such as HSPICE.

Generally speaking, the design of the power distribution network, for example, the package type, pin count, and power-line area of the Si die, has a large influence on an LSI's cost. Moreover, in the final design stage, it is only possible to make very minor changes to the power distribution parameters. Therefore, the parameters must be fixed at the beginning of layout design. By using the design flow shown in Figure 3 together with an LSI's floorplan, we can minimize the LSI's cost and avoid the need to redesign.

Figures 4 (a) and **4 (b)** show the noise distribution of the ground voltage (VSS) power mesh for two phases in a clock cycle on the Si die of an LSI that had troubled electronic equipment designers with EMI problems. At the bottom of Figure 4 (a), there is a noise peak caused by simultaneous switching of synchronous DRAM (SDRAM) I/O operating at 100 MHz. The peak noise voltage is about 200 mV, which is a serious source of EMI.

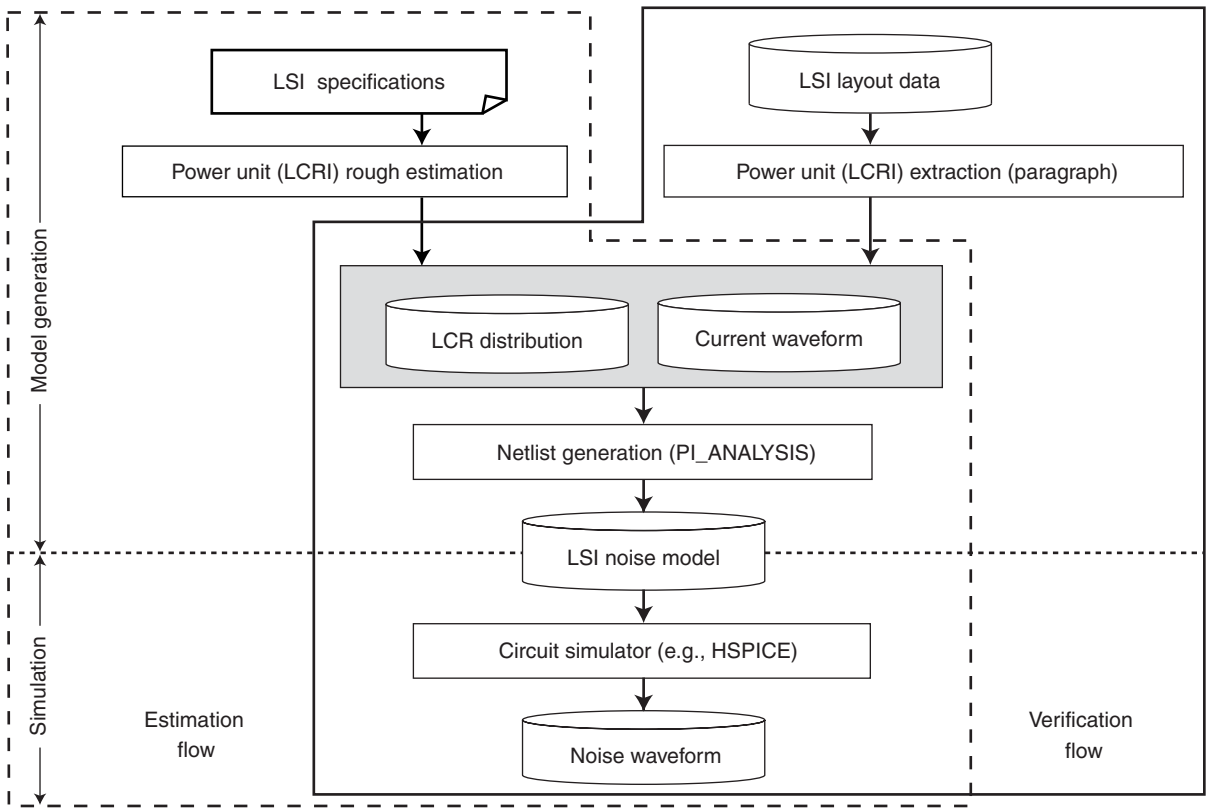


Figure 3
LSI noise model generation and simulation flow.

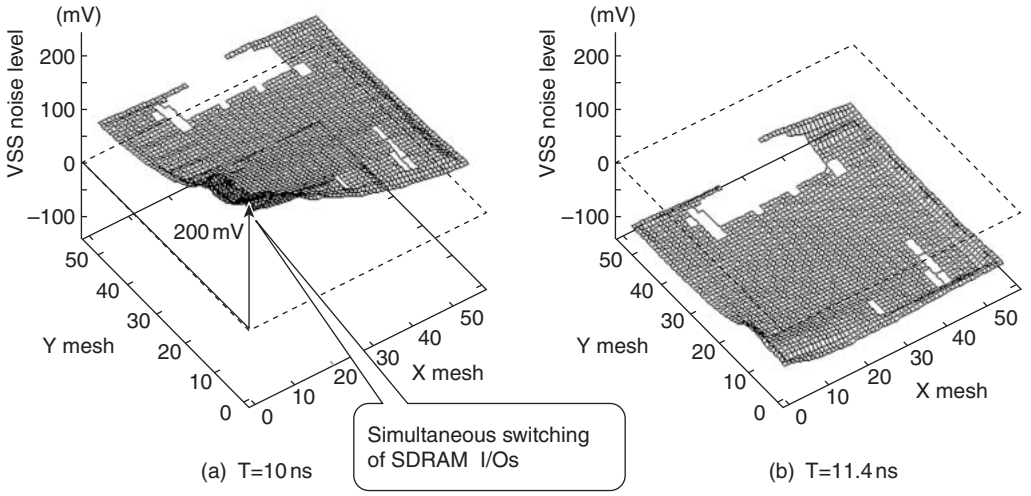
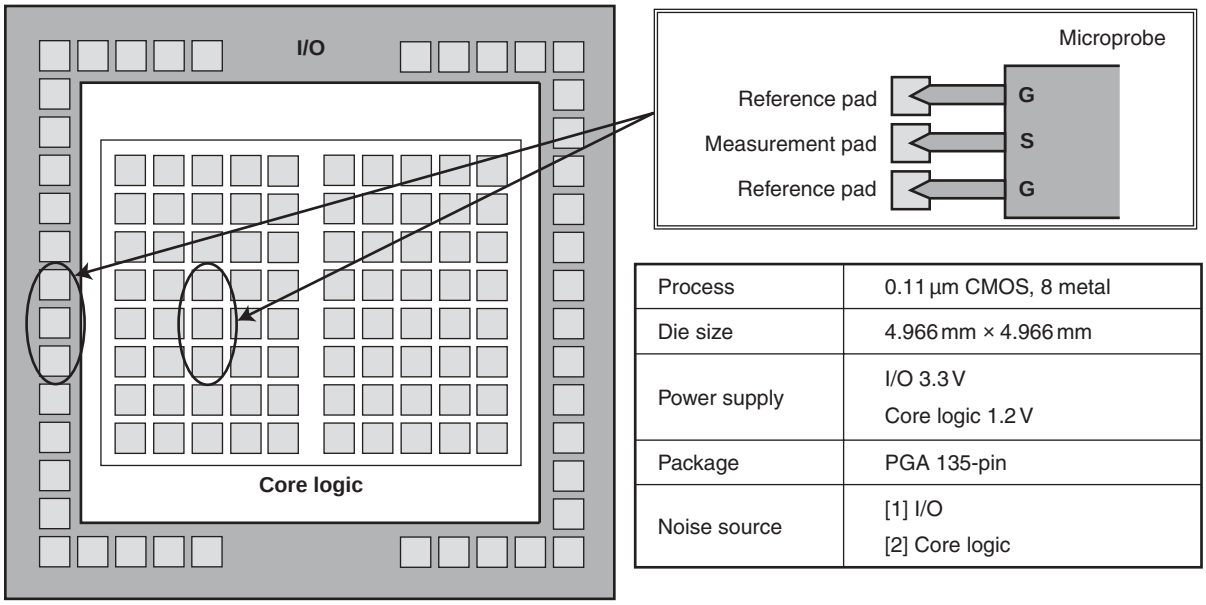


Figure 4
Simulation results of VSS plane.



Process	0.11 µm CMOS, 8 metal
Die size	4.966 mm × 4.966 mm
Power supply	I/O 3.3 V Core logic 1.2 V
Package	PGA 135-pin
Noise source	[1] I/O [2] Core logic

Figure 5
Structure of test chip.

By using our LSI noise model at an early design stage, designers can easily find this type of problem and eliminate it.

5. Test chip and measurement results

To verify the accuracy of this LSI noise model, we have designed and measured a test chip, the structure of which is shown in **Figure 5**. The chip consists of two noise sources — the core logic and I/O — and measurement and reference pads. The reference pads are used to distribute the measurement GND voltage level, so they have no DC path to the logic and I/O circuits. We directly attached a microprobe to these pads to measure the noise waveforms.

The measured and simulated waveforms are shown in **Figure 6**. In the simulation, the LSI

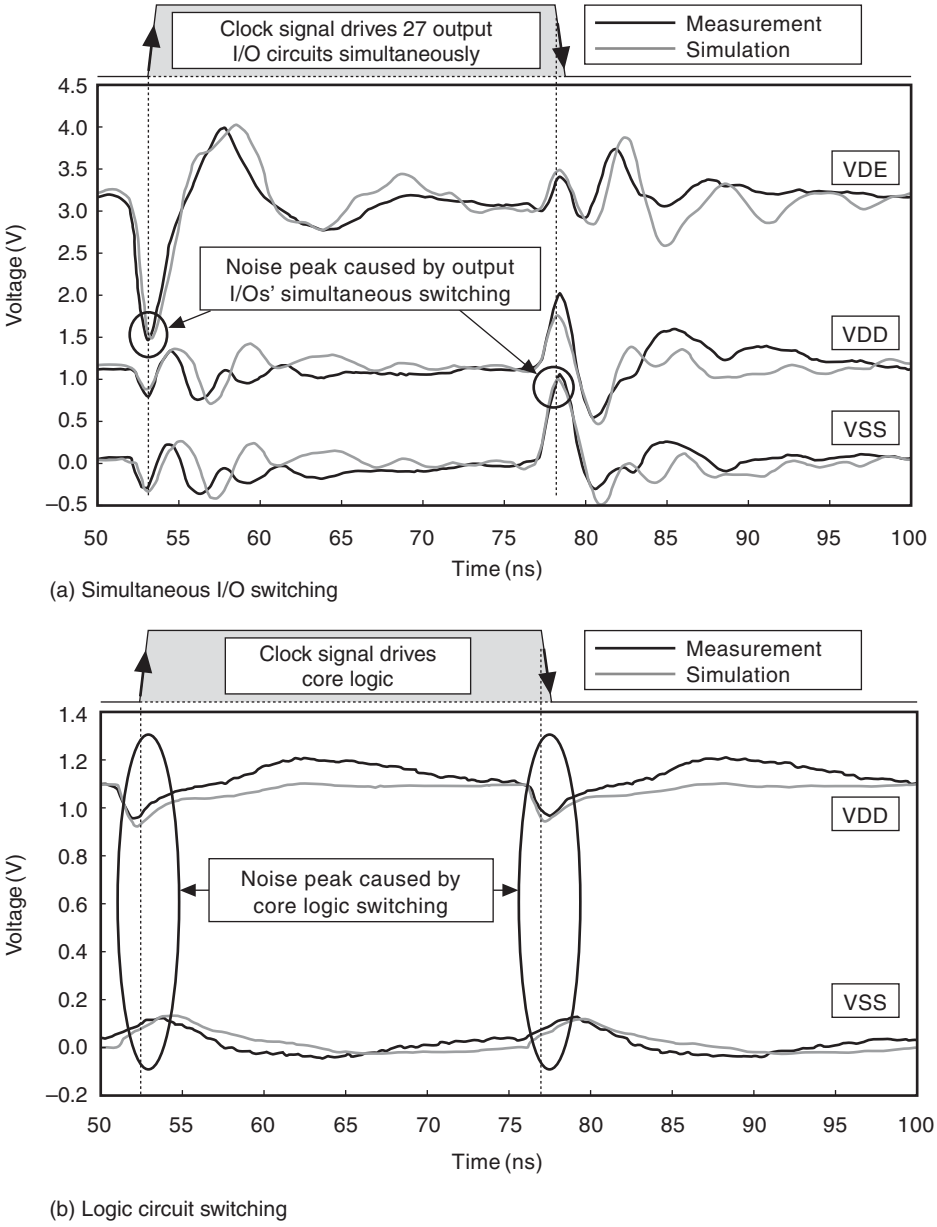


Figure 6
Comparison of measured and simulated noise.

model was analyzed in cooperation with the PCB model. PCB power integrity analysis tool SIGAL-PI[3] was used for PCB model extraction. **Figure 6 (a)** shows the SSN when 27 output I/O signals switch simultaneously. When the output signals switch from low to high, a large negative noise pulse is induced on the I/O power voltage (VDE) line, which can cause malfunctions and degrade performance. As shown in Figure 6 (a), the measured and simulated waveforms have good agreement, which indicates that the model is sufficiently accurate. Similarly, when the output signals switch from high to low, a positive noise pulse is induced on the VSS power line. There was good agreement between the simulated and measured peak noise voltages.

Figure 6 (b) shows the noise waveform caused by the dynamic switching current of the core logic circuit. Because of the logic behavior, there is a positive noise pulse on the VSS line and

a negative noise pulse on the core power voltage (VDD) line. The difference between the simulated and measured peak noise voltages was less than 10%.

Between these noise pulses, the simulated waveforms were not consistent with the measured ones. This was due to differences between the LC values — and therefore the resonant frequencies — of the package and PCB that were used in the simulation and the actual values. These differences can be minimized by improving the extraction method for the package and PCB models.

6. Application to LSI-PCB co-design

In product development, LSI and PCB co-design is strongly recommended, especially for high-performance PCB design. With a co-design methodology, designers can easily find the most effective place or parts to suppress power plane noise and thereby minimize PCB costs. Fujitsu has already developed a PCB power integrity analysis tool called SIGAL-PI. By combining this tool with our LSI noise model, we can design products that have a high noise immunity. We applied this methodology to our FR1000 media processor.[4] In the early design stage, we found a resonance noise on the power distribution line that exceeded our target window (**Figure 7**). We corrected this problem by decreasing the bypass capacitance of the power lines from 494 pF to 156 pF. We also created a PCB design guideline to suppress power and signal noise within the LSI and on the PCB. The first FR1000 prototype board has no noise problems and works well at the target specifications.

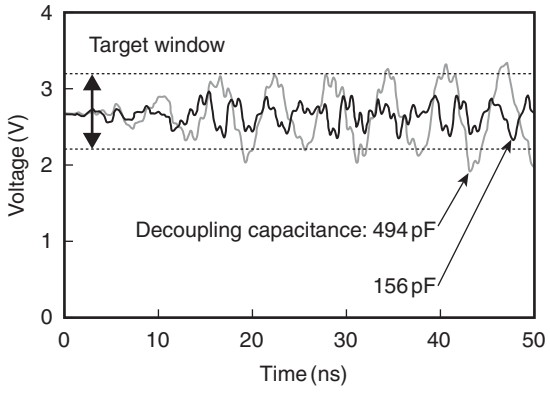


Figure 7
Simulated clock I/O power supply voltage noise in FR1000.

We are already offering this LSI and PCB co-design methodology as a consulting design service called PLACATE.

7. Conclusion

In this paper, we presented an LSI noise model that is very useful for achieving low-noise designs. We described LSI and PCB noise, the structure of the LSI noise model, and the model's generation and simulation flow. Using a test chip we fabricated for evaluating this LSI noise model, we found good agreement between measurement and simulation results. We also described an application of this model.

References

1) T. R. Arabi et al.: Design & Validation of the Pentium III and Pentium 4 Processors Power Delivery. Dig. Tech, Papers, Symposium on VLSI Circuits, 2002, p.220-223.
2) N. Matsui et al.: FDTD_SPICE Analysis of EMI and SSO of LSI ICs Using a Full Chip Macro Model. 2002 IEEE Int. Symp. Electromagnetic Compatibility, p.99-104.
3) T. Hirai et al.: Power Integrity Analysis of High-Speed PCBs. (in Japanese), *FUJITSU*, **55**, 3, p.257-261 (2004).
4) T. Shiota et al.: A 51.2 GOPS 1.0 GB/s-DMA Single-Chip Multi-Processor Integrating Quadruple 8-Way VLIW Processors. ISSCC Dig. Tech. Papers, 2005, p.144-146.

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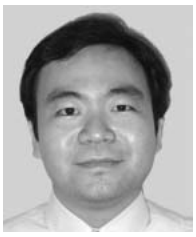

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