

Mobile Multimedia Platform (MMP)

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Mobile phones incorporating camera modules and music players are rapidly becoming popular not only in Japan, but throughout the world. This growth has led to stronger demands for mobile phones equipped with additional functions that offer graphics, audio, and images of higher quality. To fully meet these demands, we have constructed a mobile multimedia platform (MMP) based on an ARM processor with common intellectual properties (IPs). We used this platform to develop three system-on-a-chips (SoCs): the MB86V00, MB86V01, and MB86V02 (which incorporates audio/speech processing functions for the mobile phone market). These SoCs provide all the high-resolution camera/video functions required for mobile phones on a single chip with low power consumption. This paper describes the design concepts of the MMP, the development of these SoC products, and the SoCs' low-power consumption technology.

1. Introduction

Recent years have seen the proliferation of mobile phones that incorporate many embedded functions, including camera modules with resolutions higher than 3 megapixels and games that employ 2D and 3D graphics, coupled with TV-phone and music-player capabilities — all of which use high-function image and audio processing techniques. Thus, mobile phones are no longer just tools for communication or conversation: they now also incorporate the functions of various devices used in daily life.

Until several years ago, baseband LSIs designed for communications processing were used in mobile phones for this type of image processing. However, as the performance requirements for image and audio processing functions became increasingly advanced, processing capability also increased beyond the level that could be handled by these baseband LSIs.

Given the fact that the service life of mobile phone batteries remains inadequate for the use

of such features as a TV-phone function, providing the high-level functions demanded while at the same time reducing power consumption are issues that must be addressed.

Fujitsu consequently decided to build a platform for developing high-performance products for mobile multimedia use that meet the customers' needs in addition to providing a solution for the issues mentioned above.

This platform is a hardware framework that improves both system-on-a-chip (SoC) design efficiency and inspection characteristics simultaneously. Using this platform as a base of development will facilitate the prompt release of new SoC products that satisfy market demands.

This paper describes the development of this platform and the multimedia processing SoCs developed using this platform as a base. These SoCs include the MB86V00, MB86V01,¹⁾ and the latest SoC, the MB86V02, which has the music-player and speech-processing functions that are positioned as important applications for the

latest cellular phones.

2. Development of mobile multimedia platform (MMP)

Power consumption generally increases in line with higher levels of performance. For hand-held devices such as the mobile phone, however, the battery represents a crucial consideration in that high power consumption is definitely not acceptable. Mobile phone performance is increasing virtually on a daily basis, with the provision of high-quality moving images considered essential.

To provide a solution for these issues and satisfy market demands, Fujitsu has made full use of the abundant proprietary intellectual property (IP) cores that it retains to configure an MMP by using the ARM processor, considered the industry-standard CPU, and the AMBA bus as the pillars of this platform. This MMP was developed using the three design concepts described below. Among these concepts, achieving low power consumption was considered the most important.

- 1) Achieving flexibility regarding low power consumption, processing requirements, and processing functions

With regard to processing functions having particularly high requirements for low-power operation, all necessary functions were incorporated as hardware engines in the SoC, thus allowing us to provide high performance and low power consumption at the same time. Conversely, for processing requirements and functions that demand even more flexibility, we employed various methods such as a processor for software processing, a hardware assist function with a newly implemented configurable processor^{note)} at the core, and the necessary software.

- 2) Implementing hardware IPs

We incorporated the following hardware IPs in the platform to perform mobile multimedia

note) This processor can use special environments and tools for the flexible customization of functions.

processing: an ultra-low-power, high-resolution MPEG-4 codec engine; a 2D/3D graphics engine that has shown proven results in the car navigation system industry; and a CCD data-path processing engine that has likewise been widely acclaimed in the digital camera industry. Selecting these engines enabled us to achieve high-function image processing.

- 3) Realizing wide-ranging expandability

We intended to achieve even further functional expansion by enabling the respective high-performance hardware engines on the MMP to be functionally linked or combined. For this reason, we provided a platform that allows data to be sent and received between the IPs and can be freely reconfigured. Moreover, because the platform architecture was designed to enable easy verification, we were able to easily prevent bugs that tend to occur with functional expansion.

The ARM7, ARM9, and ARM11 processors, along with the accompanying high-end processor cores, were added to the processor lineup. By linking these processors to a variety of hardware IPs, we were able to fully meet user demands for a wide range of functions and performance.

3. Development of MB86V00/MB86V01 and example of system configuration

The MB86V00 and MB86V01 multimedia processing LSIs for mobile phone applications were developed in 2004 by using the MMP described in the preceding section as first-generation SoC series products.

The MB86V00 and MB86V01 incorporate an ARM7TDMI 32-bit processor (hereafter the ARM7TDMI processor) equipped with an 8 KB cache memory.

The MB86V00 and MB86V01 are positioned as companion LSIs for multimedia processing instead of a baseband LSI when the baseband LSI or similar device is used as the host CPU.

As well as realizing such multimedia processing functions as photography (for still shots) and

a video stream codec, implementing a 2D/3D graphics engine also allows the superimposing of 2D/3D animation with respect to photographed content (superimpose function), as well as the loading of superimposed images as still or moving images.

For the MB86V00, we were able to save space by packaging it together with a 64M-bit SDRAM for mobile applications. The MB86V01 is a standalone logic product without SDRAM for more flexible memory selection.

Figure 1 shows an example of a typical system configuration employing the MB86V00 and MB86V01.

The host CPU must generally perform companion LSI module management and control processing functions. Conversely, because the implemented ARM7TDMI processor performs these functions for the MB86V00 and MB86V01, the system is completely free from the high-load multimedia processing performed by the baseband LSI

and complex companion LSI control. This means that high-function multimedia processing is possible even in a system that uses a relatively low-speed host CPU.

With the MB86V00 and MB86V01, dedicated hardware engines handle almost all the other important functions required for multimedia processing. When comparing a system that employs a dedicated low power consumption circuit built into the SoC to realize functions with a software-based image processing system that uses general processors and digital signal processors (DSPs), a considerable reduction in power consumption is clearly evident. We estimated the power consumption for software operation would be 100 mW or more; however, we achieved a power consumption of just one-third of that estimate.

Moreover, when new functions must be added to an already installed system or devices such as mobile phones, the use of the ARM7TDMI processor allows new functions to be added with-

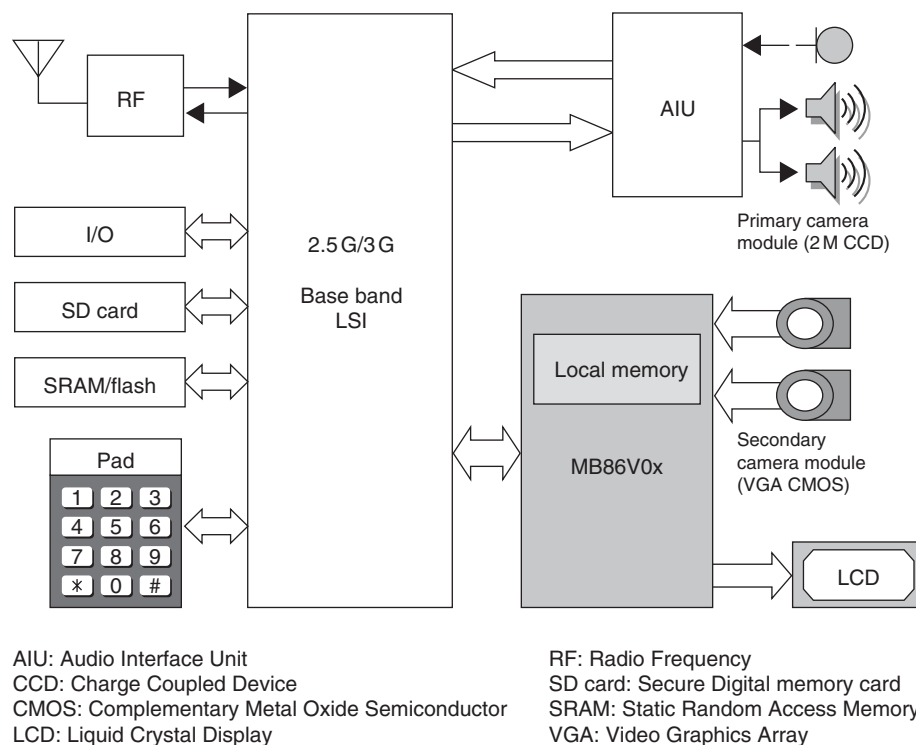


Figure 1
 Diagram of typical MB86V00/MB86V01 system configuration.

out significantly changing the system.

4. Overview of MB86V00/MB86V01 functions

The hardware macros incorporated in the MB86V00 and MB86V01 are implemented in the control bus and data path bus (both conforming to Advanced High-performance Bus [AHB]) as AHB masters. Because both macros function as an AHB master, data transferred to the DMAC that acts as an AHB slave bus can be reduced to one-half the amount of data flowing through the bus when compared to the reference architecture. This feature allowed us to maintain existing levels of bus performance and low-speed operation, thus facilitating a significant reduction in power consumption.

Table 1 lists the main specifications of the MB86V00 and MB86V01. **Figure 2** shows the internal block diagram.

The following describes the main function macros and related concepts.

4.1 Control bus macros

1) ARM7TDMI processor and peripheral circuits

Fujitsu's proprietary ARM7TDMI processor with an 8 KB cache memory, 16-bit timer, interrupt controller, DMAC, and other components are

implemented in the control bus macro, which operates at up to 54 MHz. Also incorporated is a 16 KB SRAM (no-wait).

A switchover function based on the load status of the operating clock and a function to stop the clock during CPU idle status are also provided.

2) Host CPU interface controller

An asynchronous data bus is used for the SRAM slave interface to enable the MB86V00 and MB86V01 to be accessed from the host CPU, transfer of the display list, reading and writing of codec data, and reading from and writing to areas of VRAM (SDRAM).

The host CPU interface controller was implemented as an AHB master with the same priority as for the ARM7TDMI processor on the same control bus.

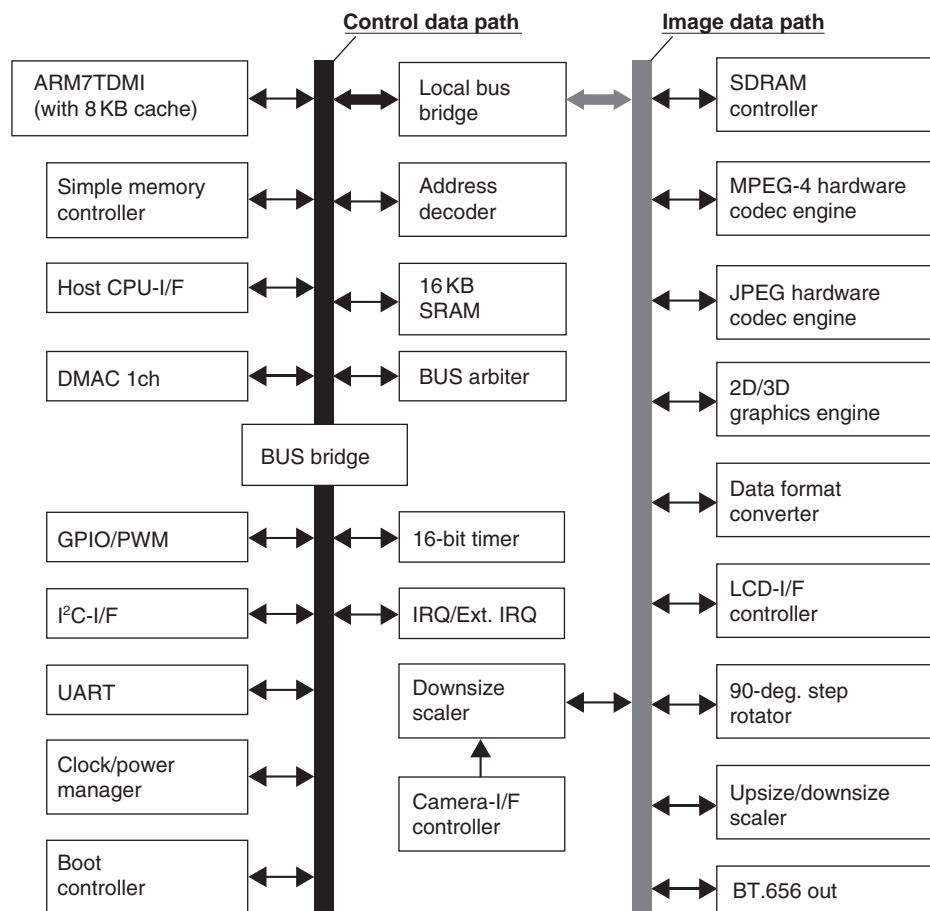
4.2 Data path bus macros

1) MPEG-4 hardware codec engine

This engine supports video stream data codec functions conforming to the MPEG-4 Ver.1 Simple Profile standard. We achieved low power consumption and high-performance operation simultaneously by implementing a video stream architecture and all the processing functions required for analysis as dedicated circuits in the SoCs. Processing is enabled at 30 fps (frames per

Table 1
MB86V00/MB86V01 specifications.

Item	Specifications
Maximum frequency	54 MHz chip, 108 MHz SDRAM
Power	1.65 to 1.95 V core and SDRAM, 2.60 to 3.60 V I/O
Technology	Low-leakage 0.18 μ m CMOS process
Packaging	289-pin FBGA, 10 mm \times 10 mm, 0.5 mm ball spacing
Main features	ARM7TDMI processor core with 8 KB cache MPEG-4 full hardware codec engine JPEG full hardware codec engine 32-bit 2D/3D graphics engine 2 megapixel camera module interface CPU type LCD module interface 16-bit asynchronous interface for baseband processor Up/down size scaler engine 90-degree step rotator engine ITU-R.BT.656 TV output



DMAC: Direct Memory Access Controller
 GPIO: General Purpose Input/Output
 I²C: Inter Integrated Circuit
 IRQ: Interrupt ReQuest
 JPEG: Joint Photographic Experts Group
 LCD: Liquid Crystal Display

MPEG: Moving Picture Coding Experts Group
 PWM: Pulse Width Modulation
 SDRAM: Synchronous Dynamic Random Access Memory
 SRAM: Static Random Access Memory
 UART: Universal Asynchronous Receiver Transmitter

Figure 2
 Block diagram of MB86V00/MB86V01.

second) for Common Intermediate Format (CIF) size (352×288 pixels) encoding and decoding functions, 15 fps for QVGA size (320×240 pixels) codec functions (e.g., teleconferencing), and 15 fps for VGA size (640×480 pixels) encoding and decoding functions.

Moreover, a Reversible Variable Length Coding (RVLC) function that employs a backward search function for error correction is supported, with codec functions for maintaining image quality even in error-prone environments also provided.

2) JPEG hardware codec engine

This codec engine has user-specifiable Huffman tables (two each for AC and DC) and four quantization tables. It also supports compression and expansion modes that conform to the JPEG baseline method.

The engine is compatible with the YUV4.2.2, 4.1.1, and 4.2.0 data formats and can compress approximately 2.2 screens of 2-megapixel (1600×1200) data per second.

3) 2D/3D graphics engine

Such functions as Gouraud shading (process-

ing of shadows), Z-buffer algorithm 3D rendering and alpha blending (translucency processing), texture mapping, and anti-aliasing processing to produce smooth line images have been incorporated into the 2D/3D graphics controller.

4) LCD interface controller

The LCD interface controller supports a CPU interface for VGA formats up to 16 777 216 colors; two-plane superimposition compatible with liquid crystal display (LCD) modules having bus widths of 8, 16, 18, and 24 bits; and functions for transparency processing and partial display processing.

Two chip-selection signals for the LCD are provided to enable compatibility with two LCD systems (primary and secondary). In addition, a function to enable access from the host CPU to the LCD module is provided via an internal resistor.

5) ITU-R.BT656 8-bit parallel outputs

Connecting an NTSC/PAL encoder and digital/analog converter (DAC) to the MB86V00 and MB86V01 permits the output of 8-bit parallel data conforming to the ITU-R.BT656 standard for display on television screens.

5. Challenge of low power consumption

To achieve low power consumption in the MB86V00 and MB86V01, a hardware IP macro for low power consumption was implemented, with middleware used to make effective use of the detailed clock control and hardware architectures.

Suppressing power at the function macro level facilitates a more precise reduction in power consumption in the chip.

The MPEG-4 codec macro and 2D/3D graphics engine are representative of products that promote low power consumption at the function macro level. These macros reduce power consumption by stopping the clocking of inactive circuit blocks, reducing the frequency of memory access, optimizing the data path and clock path structures, and implementing other measures.

At this point, without referring in detail to the reduction of power consumption achieved at the function macro level, we will focus on the chip level and describe the functioning of clock control, use of middleware for power dissipation control, and adoption of a low-leakage wafer process that allowed us to meet the challenge of achieving low power consumption.

5.1 Clock control

A clock on/off function is incorporated in the chip and in each function macro in order to reduce power at the chip level. A generally available gated clock circuit is used as the basis for clock control.

The clock control mechanism employs a manual description function and tools at the Register Transfer Level (RTL) to permit the use of automatic generation and insertion functions in tandem. The gated clock circuit on which RTL is implemented also performs frequency control by conducting clock-activity control.

Moreover, as mentioned in the overview of functions in the previous section, dividing the internal blocks and making the control blocks and data path blocks independent of each other enables operation at the required clock frequency according to the processing content.

Dividing the circuit blocks and controlling the clock frequency according to the load status and clock supplied to each circuit block enables a reduction in power consumption by reducing unnecessary clock idling.

Actually, because the major function macros are implemented in hardware with these SoCs, if required, the ARM7TDMI processor can be made to actively transition to the sleep status (i.e., clock-stopped status, recovery after interruption status).

5.2 Power dissipation control by middleware

For the middleware developed for the MB86V00 and MB86V01, a concept was adopted whereby modes are used to flexibly configure the

application functions in combination with processing of the various types of hardware macros incorporated.

According to this mode concept, an independent function processing block is selected to match the required performance speed, image size, and other factors for linking the processing blocks to perform the required functions. Moreover, the requirements for additional functions (modes) can also be flexibly handled.

To use the mode concept, it is essential to correctly determine the required processing blocks and processing performance necessary for each performance mode. The power control performed here supplies a clock according to the mode. That is, once the number of blocks required for processing and the clock frequencies have been determined, switching is performed so only the hardware blocks required for the current mode are clocked and the clocks to those blocks have the appropriate frequencies.

By implementing the major functions as hardware macros, we have achieved a large-scale reduction in power consumption when compared with software-based multimedia processing.

When middleware is used for power dissipation control, the load is monitored, thus eliminating the need to incorporate a complex, high-level mechanism to perform timely power reduction. For this reason, we decided to only employ the power dissipation control method described above.

5.3 Adoption of low-leakage wafer process

To minimize the amount of power that is wasted when not performing high-level multimedia processing, a 0.18 μm low-leakage process was used in the design and manufacturing to suppress standby leakage current.

By using this process, we suppressed leakage current to around 30 μA in samples created under standard process conditions at normal temperature and standard voltage.

6. Outline of MB86V02

In 2005, we developed a new mobile multimedia product, the MB86V02, based on the MB86V00 and MB86V01.

The MB86V02 is positioned as a companion chip like the MB86V00 and MB86V01 and has an equivalent basic system configuration. The hardware function macros used in the MB86V00 and MB86V01, as well as the ARM946E 32-bit processor and a 256 KB SRAM, are also embedded in the MB86V02. The music player/speech processing functions and interface functions such as the AD/DA converter are, however, newly added.

Conversely, the video processing performance was reduced somewhat to achieve better cost-effectiveness.

A low-tier to mid/high-tier cellular phone system can be flexibly realized according to targeted cost through the combined middleware and memory design (by using external SDRAM) of the MB86V02.

The middleware for the MB86V02 is roughly equivalent to that for the MB86V00/MB86V01, so the MB86V02 can also function as an SoC by combining the functions of the baseband LSI and the companion LSI that controls the driver software on the baseband LSI. In the latter case, the MB86V02 is well suited for use in low-tier, cellular-phone systems because the system resources (e.g., memory) are suppressed and system cost can be kept low.

Table 2 lists the MB86V02 specifications.

We adopted a 130 nm low-leakage technology and separated the power supply of the logic (two lines) and I/O (seven lines). Separating the power supply of the logic makes it possible to directly control the path from the baseband LSI to the LCD when the multimedia processing function of the MB86V02 is not needed. Under such power control, it becomes possible to cut the power supply to the main logic circuit. As a result, for a device fabricated under standard process conditions, the logic's leakage current at

Table 2
MB86V02 specifications.

Item	Specifications
Maximum frequency	104 MHz CPU, 52 MHz other logic
Power	1.10 to 1.30 V core, 1.8 V (typ, option), 2.8 V (typ), 3.3 V (typ) I/O
Technology	Low-leakage 0.13 μ m CMOS process
Packaging	204-pin FBGA, 11 mm \times 11 mm, 0.65 mm ball spacing
Main features	ARM946E processor core with 16 KB I-cache and 16 KB D-cache MPEG-4 full hardware codec engine JPEG full hardware codec engine 16-bit 2D graphics engine 2 megapixel camera module interface with up/down sizing zoom CPU and RGB type LCD module interface 8/16-bit asynchronous host-interface for baseband processor Up/down size scaler engine 90-degree step rotator engine Host-I/F ~ LSC-I/F direct-access (thru) path 256 KB onchip SRAM Audio (AAC, MP3), speech (NB-AMR) and MIDI (mobileXMF) support External SDRAM interface

normal temperature and standard voltage can be reduced to below 10 μ A. Moreover, because the I/O power supply is separated, there is greater flexibility when selecting parts for a system containing peripheral devices having different power supply voltages.

7. Future outlook

We are currently developing new mobile multimedia products based on the MB86V00, MB86V01, and MB86V02. We plan to develop companion LSIs and other processors for mobile phone systems as well as a wide range of application processor products that target system engines.

In the future, we will develop new products with due consideration given to product performance and price range. We will expand our product range by designing products positioned at the same level as the MB86V00, MB86V01, and MB86V02 and develop other products that provide higher levels of performance.

The following research themes are represen-

tative of our current activities: H.264 and digital terrestrial compatibility, high-quality audio, handshake correction when shooting still and moving pictures, dynamic power consumption observation and control functions, and improved security management. In all our product lineups and research themes, we are developing a range of products that can adequately meet various needs while maintaining a suitable balance between functions and performance on the one hand and power consumption on the other.

8. Future challenges

In terms of functions, performance, and pricing, the MB86V00, MB86V01, and MB86V02 are positioned in the low-to-middle tier of the current MMP. With regard to the functions provided, many have established specifications, and we were able to positively recommend the use of hardware. Because most of the functions are implemented using hardware macros, we were able to suppress power use to 35 mA (63 mW at 1.8 V for the MB86V00 [measured]) even when performing pro-

cessing equivalent to that required for TV-phone functions (e.g., image rotation, expansion/compression).

From now on, it will be necessary to flexibly satisfy requirements for new multimedia functions, while maintaining existing power consumption levels.

With these requirements in mind, we intend to incorporate objective pricing and discernment techniques that will allow us to more readily determine which processing areas should be software based and which should be hardware based. This objective is linked to our co-development and verification of software and hardware as a flow of development, which we believe will enable us to realize high-quality product development in a short period.

9. Conclusion

This paper introduced our mobile multimedia platform designed to facilitate the development of high-level-function SoCs with low power consumption that will be required for mobile phones and similar applications from now on. It also introduced our first-generation MB86V00 and MB86V01 series and second-generation

MB86V02.

During our development of the MB86V00, MB86V01, and MB86V02 in conjunction with Fujitsu Laboratories Ltd., we applied a new UML-based SoC design methodology called Cedar. This is the first time we used this methodology for developing products, and we delivered such impressive results as improved specification quality in the early stages; adherence to the development plan; and No-bug, No-mistake development.

The mobile multimedia platform is not just a hardware platform. We are now working to raise the co-operability level of software used in the platform as well as that of the design and verification techniques.

While proceeding with the improvement of related technologies such as those for design and development, we will continue to further develop SoCs (hardware) and middleware (software) so we can offer a reliable product range with full confidence.

Reference

- 1) MB86V00/MB86V01 multimedia processing SoCs for mobile phones. *FIND*, **22**, 4, p.18-20 (2004).



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