Approaches to Using Al_2O_3 and HfO_2 as Gate Dielectrics for CMOSFETs

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We report on recent approaches to using Al_2O_3 and HfO_2 in MOSFETs. A MOS diode with an Al_2O_3 gate dielectric into which dimethylhydrasin (DMH) was doped shows a minimum D_{it} of 4×10^{10} $cm^{-2}eV^{-1}$, which is half that of Al_2O_3. Mobility enhancement and an increase of saturation current were obtained with the DMH-doping. A SiN/HfO_2/SiON gate stack was found to suppress HfO_2/polysilicon reaction and dopant diffusion. The base oxide of SiON also helps to improve the reliability and thermal stability of the gate stack. An inversion EOT of 1.7 nm was obtained with a SiN/HfO_2/SiON gate stack that shows a saturation current of 357 μA/μm at L_g of 0.35 μm. A 55 nm CMOS with a 3 nm HfO_2 gate dielectric was fabricated using high-temperature annealing at ≥ 1000°C and cobalt silicide. Gate leakage current was decreased by more than three orders of magnitude and a low off-state current was obtained. We also investigated the thermal stability of $Hf_xAl_{1-x}O_y$. Within $0 \le x \le 0.8$, $Hf_xAl_{1-x}O_y$ stays amorphous up to 800°C, which is 300°C higher than the corresponding temperature for HfO_2.

1. Introduction

Down-scaling to sub-100 nm technology nodes requires the introduction of novel materials and processes to both the front end of line and back end of line to achieve the performance indicated in the ITRS roadmap. Channel engineering of nondoped channels, strained Si,[1),2)] and strained SiGe[3)] can be considered to be the most practical method that is compatible with conventional processes. However, gate oxide scaling is reaching the point where gate leakage current due to direct tunneling starts to occur. Although optimization of the silicon nitride/oxynitride stack[4)] and SiON gate[5)] is being pursued to suppress the leakage current, the inevitable issues of negative bias temperature instability[6)] and mobility lowering must also be considered.[7)] To overcome these problems, an alternative gate dielectric with high permittivity (high-k) is strongly required for both high-performance and low standby power (LSTP) applications.

High-k materials have been extensively studied in recent years. Ta_2O_5 was one of the first materials that were eagerly studied for their high permittivity.[8),9)] Because Ta_2O_5 is unstable on a Si surface,[10)] Ta_2O_5 tends to form an underlying SiO_2 film at the Ta_2O_5/Si interface during deposition that significantly decreases the effective capacitance. The barrier height of Ta_2O_5 from silicon is as small as 0.28 eV.[11)] Then, researchers became very interested in zirconium oxide because its heat of formation is larger than that of SiO_2[12)] and it exhibits medium permittivity in addition to a relatively large band gap and barrier height compared to Ta_2O_5.[13)] However, ZrO_2 reacts with the poly silicon gate that forms Zr-silicides.[14)] Consequently, HfO_2, whose Hf constituent is in the same column of the periodic table as zirconium, emerged as a significant gate-dielectric candidate[15)] because it forms fewer silicides than ZrO_2

and its permittivity and barrier height are comparable to those of ZrO_2. This promising material exhibits crystallization even with an as-grown CVD thin film.[16] Crystallization may give rise to a leakage path for current and dopant impurities from the polysilicon gate.[17] Because high-k MOSFETs can be fabricated using conventional CMOS process technology, the thermal stability is one of the most important criteria that must be considered when selecting materials. Al_2O_3 exhibits a high thermal stability; it remains in the amorphous phase even during annealing at > 1000°C.[18]

Recently, nitrogen doping and nitridation of high-k gate dielectrics have been reported.[18)-22] Nitrogen in high-k gate dielectrics can be expected both to suppress boron diffusion from the polysilicon gate and to increase the thermal stability. Although nitrogen is usually incorporated before or after high-k deposition, there have been few reports of in-situ nitrogen doping into high-k gate dielectrics.[20] Also, a stacked gate with a nitrided film and a high-k film should be studied to investigate the effectiveness of nitrogen.[23]

In this paper, we describe high-k MOSFETs with an Al_2O_3 film, mainly focusing on in-situ nitrogen doping into the Al_2O_3 [20] by MOCVD. Then, we evaluate the effectiveness of SiN and SiON insertions at both sides of a HfO_2 gate dielectric and apply them to an ultra-thin gate stack.[23] Then, we show the feasibility of high-k, HfO_2 gate dielectrics for low standby power applications.[24] Finally, we compare the thermal stabilities of $Hf_xAl_{1-x}O_y$ and HfO_2.

2. Preparation of high-k gate dielectrics and MOSFETs

2.1 Al_2O_3

We used low-pressure metalorganic chemical vapor deposition (LP-MOCVD) to deposit an Al_2O_3 film on a Si substrate. The precursors were triethyl aluminum ($Al(C_2H_5)_3$, TEA) and dimethylhydrasin ($NH_2N(CH_3)_2$, DMH) as a nitrogen source. The precursors were regulated with a nitrogen carrier gas. O_2 gas was used as an oxidant. A Si substrate with LOCOS isolation was chemically cleaned by the RCA method prior to the MOCVD. The substrate was heated to the deposition temperature of 500°C.

The conductance method[25] was used to investigate the interface trap density of D_{it} using the three-element model.[26] In the investigation, a quantum-mechanical CV simulation was used to derive the equivalent oxide thickness (EOT), flat band voltage (V_{fb}), and hysteresis.

2.2 HfO_2

HfO_2 was deposited by ALCVD on a thermally grown oxynitride layer (bottom SiON) or a chemical oxide layer (bottom SiO_2) after standard RCA cleaning. The typical HfO_2 layer was 3 nm thick. To form a gate stack with a thinner EOT, the HfO_2 layer thickness was decreased and an LPCVD-SiN layer was grown on the HfO_2 (top SiN) to suppress silicide formation and dopant penetration. This was followed by poly-Si gate deposition. We used the split CV method at 100 kHz to measure the gate capacitance in the inversion region.

2.3 $Hf_xAl_{1-x}O_y$

$Hf_xAl_{1-x}O_y$ was deposited by the same method as the one used for Al_2O_3. The composition ratio (atomic percentage ratio) of x was defined by Rutherford Back Scattering (RBS) and spectroscopic ellipsometry. The thermal stability was estimated by X-ray diffraction (XRD) and cross-sectional transmission electron microscopy (XTEM).

2.4 Device fabrication process

After high-k gate dielectric film deposition, post-deposition annealing and sequential polysilicon deposition were performed. The polysilicon was patterned with EB or photolithography using dry etching. The minimum gate length, L_{CAD}, was 50 nm. After extension and pocket implantation, if needed, a side wall of the polysilicon gate was formed and source/drain/gate implantation

was performed. The following activation annealing was done in the range from 800°C to 1050°C. Metal Co-silicide contacts were used except for the Al_2O_3 MOSFETs. Post metallization annealing was performed at 450°C in an H_2/N_2 ambient.

3. Results and discussion

3.1 Al_2O_3 gate dielectrics

Al_2O_3 exhibits a high thermal stability. If nitrogen could be readily incorporated, dopant diffusion would be suppressed and any negative fixed charge would be neutralized. In this section, we investigate the effect of in-situ nitrogen doping into Al_2O_3 using DMH, which is as an active source of nitrogen.

Figure 1 shows the CV characteristics of an Al_2O_3 MOS diode that is 3.5 nm thick. We corrected experimental capacitance data using the three-element model with a series resistance determined by Vogel's method.[26] The CV parameters obtained by fitting a quantum mechanical simulator to the calibrated data and setting a gate leakage current of J_g at V_{fb}-1 V are shown in **Table 1**. We also fabricated DMH-doped, nMOS and pMOS versions of this 3.5 nm, Al_2O_3 MOS diode. Compared to the non-DMH-doped diodes, the EOT and hysteresis are slightly lower in the nMOS and the pMOS, ΔV_{fb} is higher in the nMOS and lower in the pMOS, and J_g is higher in the nMOS and the pMOS. The source/drain annealing conditions were 950°C for 10 s for pMOS and 1000°C for 5 s for nMOS. Changing the annealing temperature of the pMOS diode from 800°C to 950°C made little difference to the work function difference between the polysilicon gate and well. Nitrogen in silicon oxynitride induces a positive charge. Therefore, the decrease of ΔV_{fb} in pMOS may be caused by the introduction of N to the Al_2O_3 film. Actually, N was distributed around the Al_2O_3/Si-substrate interface with a peak density of about 0.5%. The opposite shift of ΔV_{fb} in nMOS is not well understood. Since the precursors include alkyl groups, other chemical reactants may contribute to the shift and the increase of J_g.

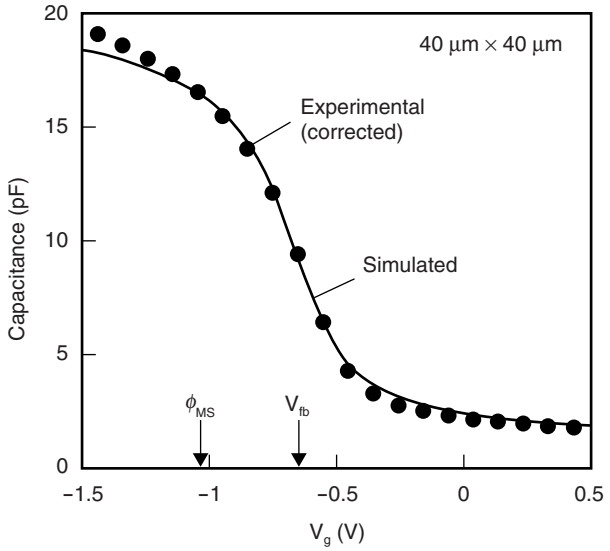

Figure 1
CV characteristics of 40 μm□ Al_2O_3 MOS diode. Circles show corrected capacitances obtained using the three-element model. Solid line shows a simulated result that accounts for quantum mechanical effects.

Figure 2 shows the I_d-V_g characteristics of Al_2O_3 MOSFETs with and without DMH doping. Both types of MOSFETs show a subthreshold slope of 70 mV/decade. The I_d-V_g of the Al_2O_3 MOSFET is unsymmetrical and is further shifted in the positive direction by DMH doping. The nMOSFET shows a larger V_{th} shift, which corresponds to the results of MOS diodes. **Figure 3** shows the I_d-V_d characteristics. The DMH-doped Al_2O_3 MOSFET apparently shows a higher current drivability (I_{dsat} [I_{on}]) than that of the Al_2O_3 MOSFET, even when the gate overdrive is taken into consideration. **Figure 4** shows the normalized transconductance

Table 1
CV parameters and leakage current of Al_2O_3 MOS diodes with and without DMH doping.

	nMOS		pMOS	
	Al_2O_3	DMH-doped Al_2O_3	Al_2O_3	DMH-doped Al_2O_3
EOT (nm)	2.6	2.5	2.5	2.3
Hys. (V)	0.06	0.05	0.16	0.07
ΔV_{fb} (V)	0.42	0.47	0.23	0.17
Jg (A/cm^2)	0.003	0.02	0.1	0.5

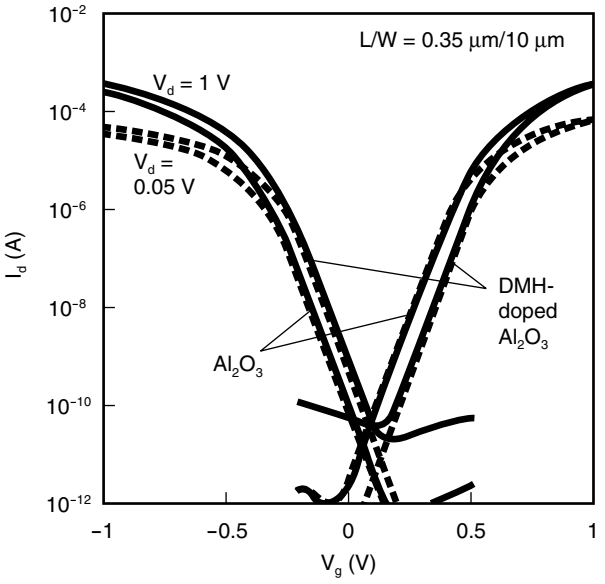

Figure 2
I_d-V_g characteristics of Al_2O_3 MOSFETs with and without dimethylhydrasin (DMH) doping. L/W = 0.35 μm/10 μm.

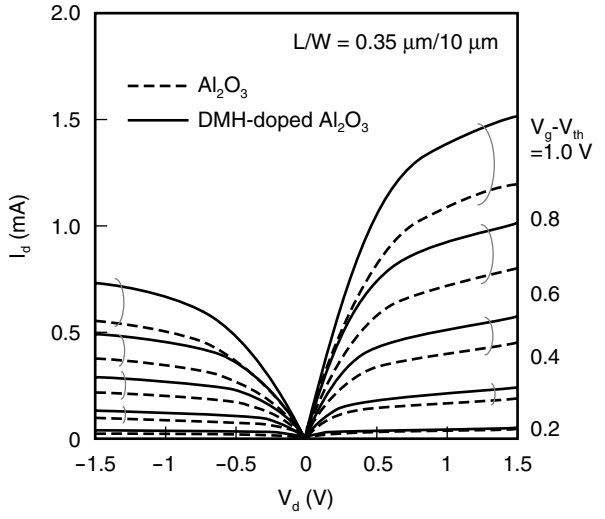

Figure 3
I_d-V_d characteristics of Al_2O_3 MOSFETs with and without DMH doping. L/W = 0.35 μm/10 μm.

(g_m) -gate voltage relationship of the Al_2O_3 MOSFET. The capacitive effective thickness (CET) is defined as the C_{max} in the accumulation region of the CV curve. We used a MOSFET with a SiON gate dielectric as a reference. The difference in normalized transconductance between Al_2O_3 and

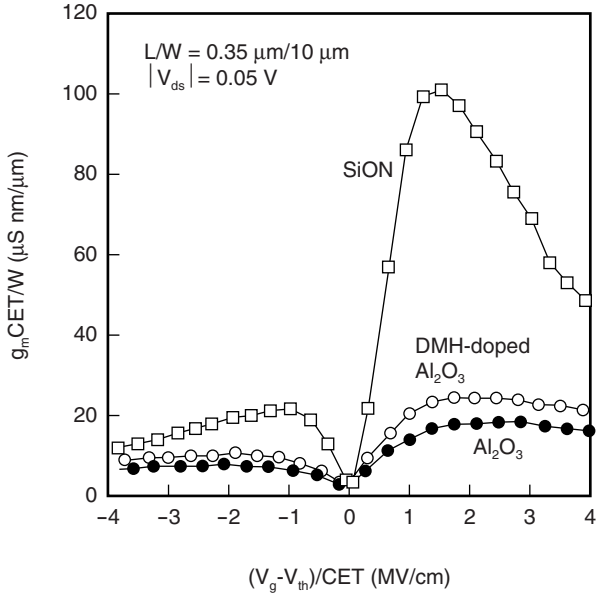

Figure 4
Normalized g_m-V_g characteristics of Al_2O_3 MOSFETs with and without DMH doping (L/W = 0.35 μm/10 μm) and for a reference MOSFET with a SiON gate dielectric.

the reference MOSFETs is large. However, the effect of DMH-doping into the Al_2O_3 clearly contributes to a mobility enhancement over the entire range. Since it is well known that MOSFETs with Al_2O_3 gate dielectrics show a lower effective mobility due to a large amount of ionized, scattered particles near the lower interface of the high-k,[27] we also consider that this lower g_m is caused by Coulomb scattering near the channel.

Figure 5 shows the energy dispersion of the interface trap density, D_{it}, at the lower interface of the high-k. To obtain D_{it}, we used the conductance method and the following relationship:[20),25)]

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{MAX} \quad (1)$$

The samples used were MOS diodes with a large area of 160 μm□ to increase the signal-to-noise ratio. The diodes were on the same wafer as the MOSFETs. The DMH-doped Al_2O_3 MOS diodes show a lower D_{it} in the whole range of p- and n-types. The pMOS had a larger D_{it} because they were subjected to a lower activation annealing temperature (950°C) than the nMOS (1000°C).

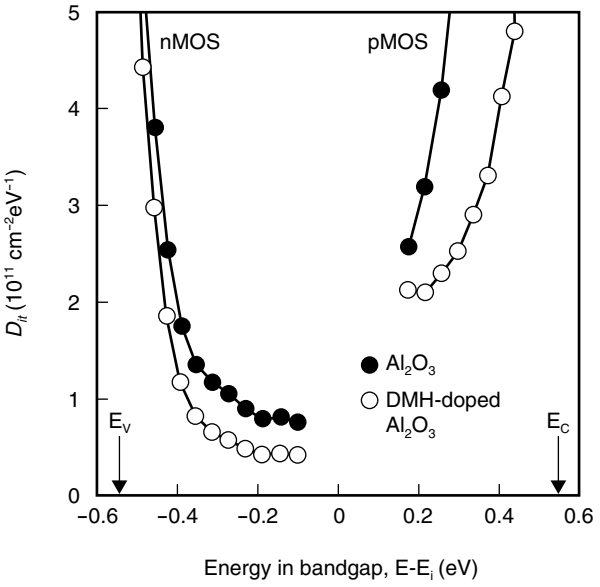

Figure 5
Energy dispersion of interface trap density (D_{it}) of Al_2O_3 MOS diodes with and without DMH doping. Samples are 160 μm□ and were fabricated on the same wafer as the MOSFETs.

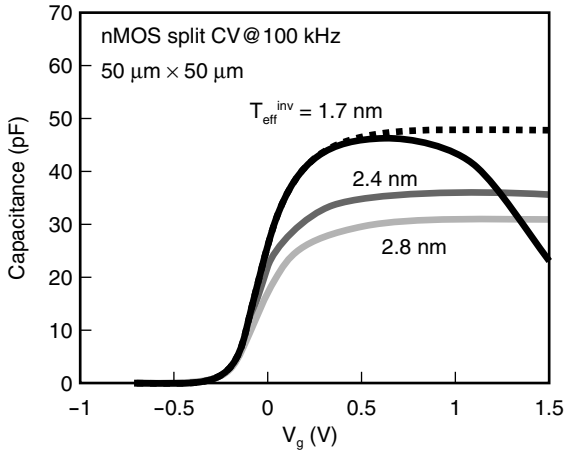

Figure 6
CV characteristics of nMOS diodes with SiN/HfO_2/SiON gate stacks in the inversion region. Area is 50 μm□. Measurement frequency was 100 kHz.

This temperature difference strongly affects the formation of D_{it}. A minimum D_{it} of 4×10^{10} $cm^{-2}eV^{-1}$ was obtained in the DMH-doped Al_2O_3 MOS diode near the midgap, which is half of that obtained in the Al_2O_3 MOS diode. Since the DMH-doping slightly decreases the EOT, interface layer growth could be suppressed even with a nitrogen content as low as 0.5%, which helps decrease the D_{it}. Although, as discussed previously, other causes can be considered, this mobility enhancement and increase of I_{dsat} is attributed to DMH-doping into the Al_2O_3.

3.2 Ultra-thin HfO_2 gate stack

As far as J_g is concerned, it is crucial that we suppress chemical reactions between the polysilicon gate and high-k material, especially in an ultra-thin gate stack. As is the case that the reaction between ZrO_2 and polysilicon is well understood, an HfO_2/polysilicon interface also shows area-dependent breakdown characteristics.[28] In addition to a base oxide of SiON, we investigated the effect of a SiN insertion layer between the HfO_2 and polysilicon gate.

Figure 6 shows the CV characteristics in the inversion region of SiN/HfO_2/SiON gate stacks having three different thicknesses. The decrease of capacitance at higher gate voltages is due to gate leakage; however, the inversion EOT, T_{eff}^{inv}, was estimated to be 1.7 nm. This means that after gate depletion and the inversion layer thicknesses have been factored in, we can expect to achieve an EOT as small as 0.9 nm. **Figure 7** shows the J_g-T_{eff}^{inv} relationship for the SiN/HfO_2/SiON gate stacks. J_g was defined as the leakage current at V_g = 1.2 V in the accumulation region. A J_g of less than 30 mA/cm^2 at 1.2 V was obtained with a T_{eff}^{inv} of 1.7 nm. These devices have a J_g that is 5 to 6 orders of magnitude smaller than that of a reference SiO_2 gate stack. We investigated the effect of a SiN layer on the breakdown voltage of V_{BD}. We prepared SiN/HfO_2/SiON, HfO_2/SiON, and HfO_2/SiO_2 gate stacks with, respectively, a T_{eff}^{inv} of 2.4 nm, 2.5 nm, and 2.6 nm. The SiN/HfO_2/SiON gate stack showed a small distribution and a V_{BD} as high as –4 V, while the other two gate stacks showed a very low V_{BD} of under –1.3 V. The area dependence of the V_{BD} of the SiN/HfO_2/SiON gate stack was also quite small. These results imply that the SiN layer on the HfO_2 completely

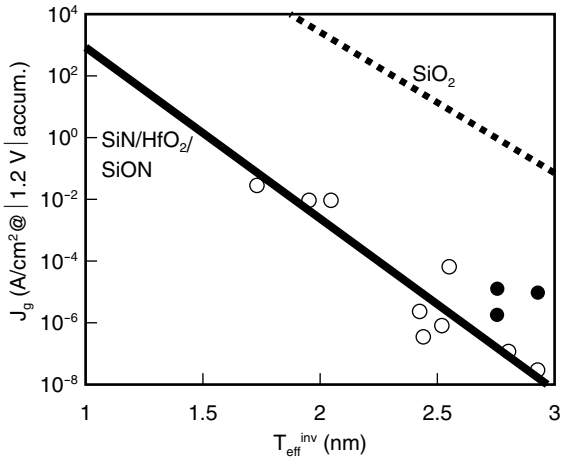

Figure 7
J_g-T_{eff}^{inv} relationship of SiN/HfO_2/SiON gate stack. J_g was defined as the leakage current at V_g = 1.2 V in the accumulation region. White circles are for nMOS, and black circles are for pMOS. The dotted line shows the case for SiO_2.

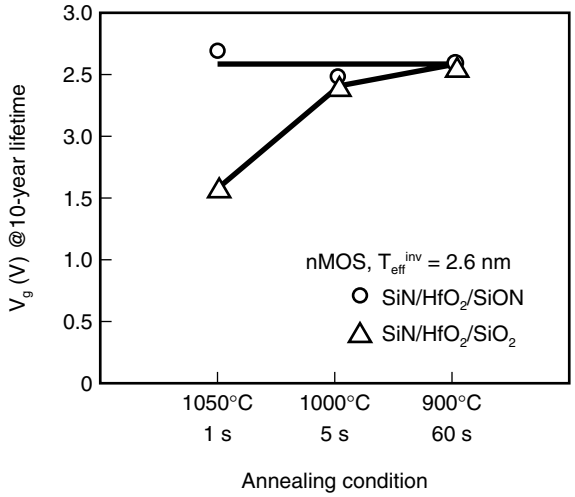

Figure 8
Annealing temperature dependence of time dependent dielectric breakdown of nMOS diodes with SiN/HfO_2/SiON and SiN/HfO_2/SiO_2 gate stacks.

suppressed the partial reaction between the HfO_2 and the polysilicon gate. This phenomenon was confirmed by AES analysis. In addition, we also observed that the SiN top layer suppressed gate dopant diffusion through the gate stack. Therefore, the SiN/HfO_2/SiON gate stack is a promising technology for realizing ultra-thin, gate stacks in 65 nm nodes and beyond.

We now focus on the effects of the base oxide on reliability and mobility. **Figure 8** shows the annealing temperature dependence of the time dependent dielectric breakdown (TDDB) of nMOS diodes with SiN/HfO_2/SiON and SiN/HfO_2/SiO_2 gate stacks for a 10-year lifetime. Both gate stacks have a T_{eff}^{inv} of 2.6 nm. The figure shows that the SiN/HfO_2/SiON gate stack has an almost constant V_g of around 2.6 V when it is annealed at between 950°C and 1050°C. However, the V_g of the SiN/HfO_2/SiO_2 gate stack decreases by 1 V as the annealing temperature increases over the same range. This indicates that the base oxide of SiON has a better thermal stability[29] than SiO_2, which may strongly influence reliability. However, as shown in **Figure 9**, from the point of view of effective mobility, the SiN/HfO_2/SiON gate stack

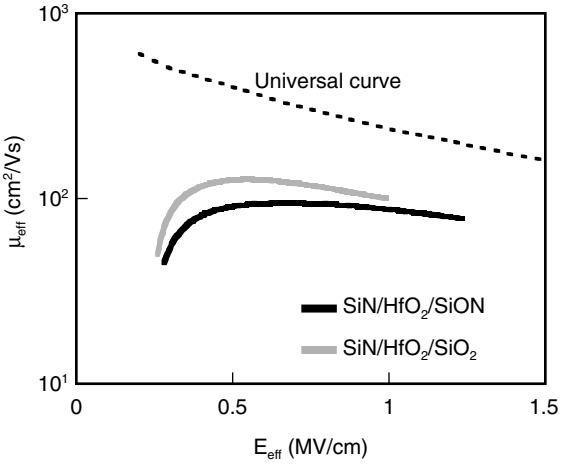

Figure 9
Effective mobility curves of nMOSFETs with a SiN/HfO_2/SiON gate stack and a SiN/HfO_2/SiO_2 gate stack.

shows a lower mobility than the SiN/HfO_2/SiO_2. This may be caused by a fixed charge that is induced by N-doping into the SiO_2. It is well known that N incorporation into the SiO_2 lowers the mobility in SiON and SiN gate stacks; therefore, this difference may be due to the presence of nitrogen.

Figure 10 shows the characteristics of an nMOSFET with an optimized SiN/HfO_2/SiON gate stack. An I_{dsat} of 357 µA/µm at L_g of 0.35 µm was

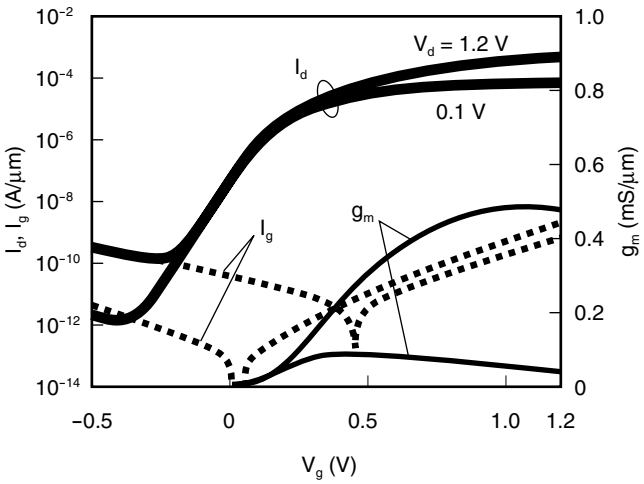

Figure 10
Characteristics of an nMOSFET with an optimized SiN/HfO_2/SiON gate stack. The thick solid lines show I_d-V_g, thin solid lines show g_m-V_g, and dotted lines show I_g-V_g.

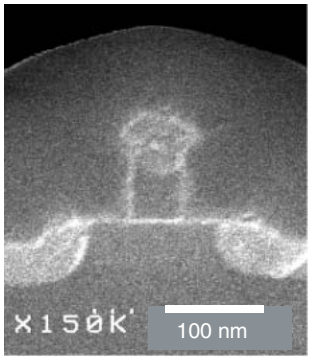

Figure 11
Cross-sectional SEM image of HfO_2 MOSFET with 50 nm polysilicon gate and Co-silicide contact.

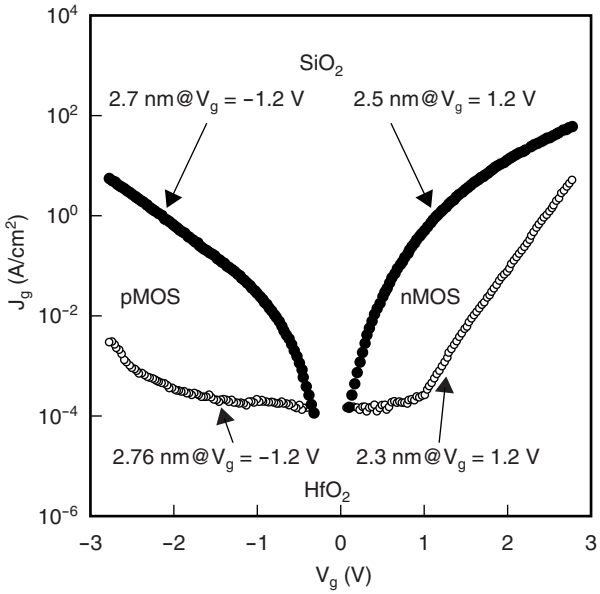

Figure 12
J_g-V_g characteristics of HfO_2 MOSFETs in inversion condition and a reference MOSFET with a SiO_2 gate oxide. RTA was performed at 1025°C.

obtained with a T_{eff}^{inv} of 1.7 nm. The gate leakage current was very low, despite the small T_{eff}^{inv}. An excellent subthreshold swing of 73 mV/decade was also obtained.

3.3 Feasibility of using HfO_2 gate dielectric MOSFET in low standby power applications

From the practical point of view, high-k gate dielectrics are expected to be used in low leakage and LSTP applications. In this section, we show the feasibility of a HfO_2 gate dielectric MOSFET for LSTP applications whose L_g is much lower than has been reported so far.[30] The HfO_2 thickness in this experiment was 3 nm.

Figure 11 shows a cross-sectional SEM image of a HfO_2 MOSFET with a 50 nm polysilicon gate and Co-silicide. The extension and pocket implant conditions were varied to facilitate the removal of residual HfO_2 during the wet process. From CV measurements, the gate depletion was suppressed by increasing the activation annealing temperature to 1000°C. The EOT of the HfO_2 MOSFETs was estimated to be 1.4 nm. **Figure 12** compares the J_g-V_g characteristics of the HfO_2 MOSFETs in the inversion condition with a reference MOSFET having a SiO_2 gate oxide whose thickness was nearly equal to that of the HfO_2 MOSFETs. The J_g of the HfO_2 MOSFETs was decreased by as much as three orders of magnitude due to the increase of permittivity. **Figure 13** compares the I_d-V_g characteristics of the HfO_2 MOSFETs with L_g of 300 nm and a reference MOSFET having the same channel dose. V_{th} was defined at an I_d of 10^{-7} A/μm for all samples. The I_d of the HfO_2 MOSFETs in the off-state (I_{off}) is

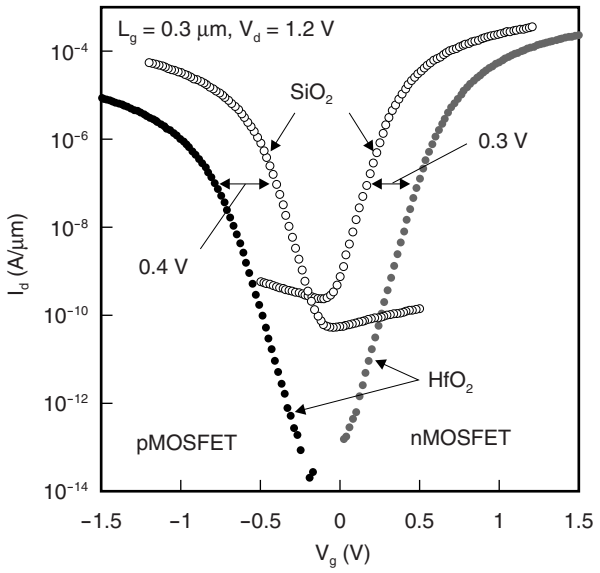

Figure 13
I_d-V_g characteristics of HfO_2 MOSFETs with L_g of 300 nm and a reference MOSFET with the same channel dose. RTA was performed at 1025°C.

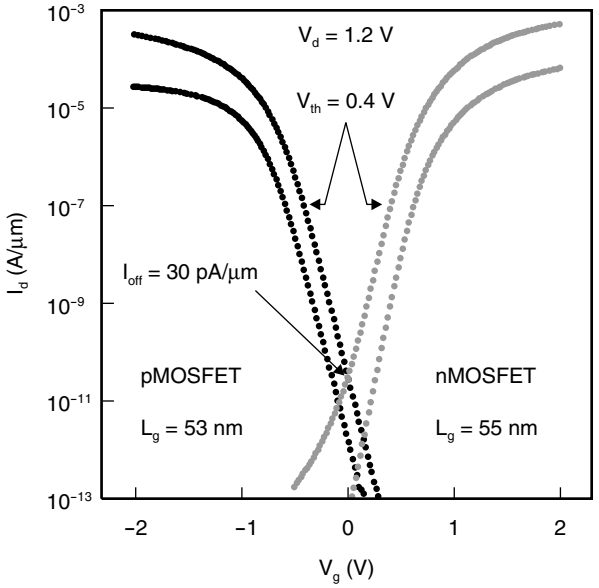

Figure 14
I_d-V_g characteristics of HfO_2 MOSFETs with L_g of 55 nm and HfO_2 of 3 nm.

less than 1 pA/µm, which is 10 000 times lower than that of the SiO_2 reference. The SiO_2 reference has a high I_{off} because it has a high gate leakage current. Therefore, the I_{off} cannot be suppressed by increasing the threshold voltage.

V_{th} almost stays constant down to L_g of 50 nm. Although the corresponding subthreshold factor gradually rolls up to 100 mV/decade, short channel effects in the nMOSFETs were fairly well suppressed even when the L_g was reduced to 50 nm. The subthreshold factors of the pMOSFETs (95 to 100 mV/decade) were slightly larger than those of the nMOSFETS, even at L_g as high as 0.2 µm. This difference can be considered to be due to boron penetration through the HfO_2. This issue can be improved by introducing a thin SiN layer as discussed in Section 3.2.

The I_d-V_g characteristics of HfO_2 MOSFETs with L_g of 55 nm are shown in **Figure 14**. The V_{th} was controlled by adjusting the channel doping concentration. The I_{off} of 25 pA/µm that was achieved was slightly larger than that shown in Figure 13, because the V_{th} was decreased by channel doping control and the subthreshold factor was increased. However, the I_{off} is still small, considering the value of EOT. We observed well-behaved I_d-V_d characteristics in the HfO_2 MOSFETs with a small L_g of 55 nm. An I_{dsat} of 140 (110) µA/µm and an I_{off} of 25 (25) pA/µm were obtained at $V_g = V_d = 1.2$ V. A T_{eff}^{inv} of 2.3 (2.9) nm and a J_g of 2×10^{-4} (5×10^{-4}) A/cm^2 for n(p)MOSFETs with a 3 nm-thick HfO_2 layer. Although I_{dsat} was observed to be relatively small, I_{on}/I_{off} can be improved by improving the mobility and suppressing boron penetration as discussed in Section 3.2.

3.4 Thermal stability

CVD HfO_2 films tend to crystallize at a fairly low temperature. Since Al_2O_3 has a high thermal stability, Al incorporation into HfO_2 can be considered to increase the thermal stability in addition to increasing the entropy. In this section, we examine the thermal stability of $Hf_xAl_{1-x}O_y$ using XRD and XTEM.

Figure 15 shows the tendency of crystallization in the range from the as-deposited temperature (500°C) to 1050°C. Although the annealing time and film stack structure are not

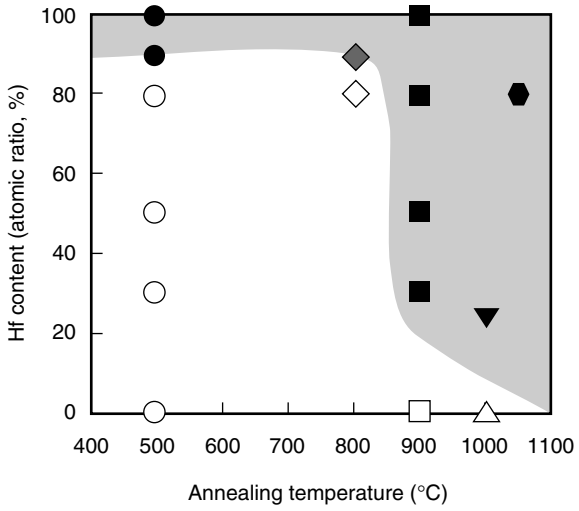

Figure 15
Crystallization map of $Hf_xAl_{1-x}O_y$ layers. The x-axis shows the Hf content as the atomic percentage, and the annealing temperature is from the 500°C as-deposited temperature to 1050°C. White symbols indicate the amorphous phase, and black symbols indicate the crystallized phase as judged from XRD and XTEM. The gray diamond indicates an ambiguous phase. Also:
- Circles indicate 10 nm, as-deposited layer.
- Diamonds indicate 4 nm layer annealed at 800°C for 30 s.
- Squares indicate 10 nm layer annealed at 900°C for 30 s.
- Black triangle indicates 10 nm layer annealed at 1000°C for 10 s.
- Hexagon indicates 4 nm layer annealed at 1050°C for 60 s with polysilicon.
- White triangle is quoted from Ref.18).
- All samples except the as-deposited and quoted samples were annealed in N_2 ambient.

unified, the degree of crystallization can be grasped and the hatched area can be considered to be crystallized. Even when the Hf content of x is increased from 0 to 0.8, the $Hf_xAl_{1-x}O_y$ stays amorphous up to 800°C. Therefore, even an Al incorporation of only about 10% by atomic percentage into HfO_2 increases its thermal stability by 300°C.

We measured the gate leakage current and accumulation capacitance of MOS capacitors with a polysilicon gate and a 4 nm-thick $Hf_xAl_{1-x}O_y$ ($0 \leq x \leq 1$) layer. We found that the minimum leakage current and the maximum capacitance was obtained at x = 0.8. This suggests that even a small amount of Al in $Hf_xAl_{1-x}O_y$ suppresses the crystallization that may cause leakage current and increases the dielectric constant. This in turn suggests that Hf-rich $Hf_xAl_{1-x}O_y$ combines the thermal-stability advantage of Al_2O_3 and the dielectric-constant advantage of HfO_2, and is therefore a potential candidate for 65 nm nodes and beyond.

4. Summary

We reported on recent progress in high-k gate dielectrics made of Al_2O_3, HfO_2, and $Hf_xAl_{1-x}O_y$ ($0 \leq x \leq 1$). Several types of MOSFETs were fabricated with a conventional CMOS process and then evaluated. We obtained the following results:

1) We investigated an Al_2O_3 gate stack with and without DMH-doping. A minimum D_{it} of 4×10^{10} $cm^{-2}eV^{-1}$ was obtained near the midgap in a DMH-doped Al_2O_3 MOS diode, which is half that obtained in a non-DMH-doped Al_2O_3 MOS diode. Also, DMH-doping into Al_2O_3 provided a mobility enhancement and an increase of I_{dsat}.
2) We found that a top SiN layer greatly helps to suppress HfO_2/polysilicon reaction and dopant diffusion. The base oxide of the SiON also helps to improve the reliability and thermal stability of the gate stack. We fabricated an nMOSFET with a SiN/HfO_2/SiON gate stack having a T_{eff}^{inv} of 1.7 nm that shows an I_{dsat} of 357 µA/µm at L_g of 0.35 µm. This SiN/HfO_2/SiON gate stack is a promising technology for realizing ultra-thin, gate stacks in 65 nm nodes and beyond.
3) A 55 nm CMOS with a 3 nm HfO_2 gate dielectric was fabricated using a conventional process flow with high-temperature annealing at ≥ 1000°C and a cobalt silicide. The J_g was decreased by more than three orders of magnitude, and a low I_{off} was obtained. These results show that HfO_2 is very promising for low-standby power applications.
4) We investigated the thermal stability of $Hf_xAl_{1-x}O_y$ by varying the annealing temperature and the Hf content of x. Within the

range $0 \leq x \leq 0.8$, $Hf_xAl_{1-x}O_y$ stayed amorphous up to 800°C, which is at least 300°C higher than the corresponding temperature for HfO_2.

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