## Reliability Improvement in Deep-Submicron nMOSFETs by Deuterium

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This paper reviews recent experimental and theoretical findings critical for process integration of deuterium post-metal anneals to improve hot-electron reliability in deepsubmicron Si CMOS circuits. After the first demonstration using deuterium, this concept has been reproduced and extended by several other researchers. In this paper, we propose a mechanism that explains the large improvement in hot-electron reliability that is observed when deuterium is introduced. We also describe spectroscopic experiments we made that support this mechanism, including its treatment of the dissipation of excited vibrational energy to the substrate silicon lattice.

### 1. Introduction

Low-temperature, post-metal annealing in a hydrogen gas ambient is widely used in MOS fabrication to form SiH bonds with the Si dangling bonds at the Si/SiO<sub>2</sub> interface and thereby passivate them. This procedure is necessary because the dangling bonds cause circuit instabilities by shifting the threshold voltage Vth and reducing the channel conductance. It is now accepted that, over very long-time operation, the SiH bonds are gradually broken by electrons passing through dielectrics such as SiO<sub>2</sub>, which results in the formation of silicon dangling-bonds and the release of hydrogen atoms. The requirement for a stable Si/SiO<sub>2</sub> interface has increased as the gate length of MOS devices has been reduced, and this has led to a search for electrically passivating atoms that can form stronger bonds with the Si. The use of deuterium instead of hydrogen in the post-metal anneal of MOS devices with an Si/SiO<sub>2</sub> interface was first proposed by Lyding et al.<sup>1)</sup> in 1996. Afterward, Lyding et al.<sup>2)-6)</sup> and other groups,<sup>7)-9)</sup> including us, demonstrated that passivation using deuterium in an oxynitride interface and in a silicon-nitride side-wall system improved stability. The purpose of this paper is to give readers references on this topic.

# 2. Post-metal annealing in deuterium

#### 2.1 Background

Lyding et al. found that the electronstimulated desorption yield of deuterium from silicon surfaces is hundreds of times lower than that of hydrogen.<sup>10)-13)</sup> Based on this finding, the group proposed the use of deuterium in the post-metal anneal, because the SiD bonds formed in the interface would be more resilient to electron bombardment than SiH bonds during device operation. In their first demonstration,<sup>1)</sup> they exposed SiD bonds to hot electrons and monitored the evolution of Vth to gain an indication of the hot-electron reliability. The first demonstration showed that the use of deuterium can provide a large improvement in circuit stability. We have performed experiments that provided similar results, including experiments involving D diffusion through inter-metal dielectric layers.



#### Figure 1

Cross-sectional view of MOSFET with multi-level Cu/dielectrics used in this work.

#### 2.2 Experimental details

For our experiments, we fabricated a  $0.12 \ \mu m$ CMOSFET with a shallow trench isolation; 2.3 nm-thick gate oxynitride; and six layers of copper wiring, including oxide (SIO), nitride (SIN), and oxynitride (SION) interlayer dielectrics. The device is shown in Figure 1. Then, we annealed with  $D_2$ ,  $H_2$ , or  $N_2$  and compared the effects on hotelectron reliability. To clarify the thermal/chemical reactions that occur during the introduction of D atoms, we observed chemical structures that contain H/D atoms in the interlayer dielectrics using an FTIR. D<sub>2</sub> annealing followed by additional annealing in N<sub>2</sub> or H<sub>2</sub> ambient at 450°C was also carried out to check their thermal stabilities. The thermal migration of deuterium and hydrogen through the several dielectric layers up to the interface was also analyzed using SIMS.

#### 2.3 Hot-carrier immunity

Before applying electrical stress with hot electrons, we compared the initial electrical characteristics of nMOSFETs annealed in  $D_2$ ,  $H_2$ , and  $N_2$  ambients. As shown in **Figures 2** and **3**, there was no significant difference in current drivability or transconductance ( $g_m$ ) among these samples.

**Figure 4** shows the degradation of drain current for  $D_2$ ,  $H_2$ ,  $N_2$ , and  $3\% H_2/N_2$  annealed samples under hot-electron stress. A superior



#### Figure 2

Dependence of drain current on drain voltage of nMOSFETs annealed in  $D_2$ ,  $H_2$ , and  $N_2$  ambients. Each annealing was performed at 450°C for 3 hours. Current drivabilities of these samples are almost the same.



Figure 3

Dependence of transconductance on gate bias of nMOSFETs annealed in  $D_2$ ,  $H_2$ , and  $N_2$  ambients at 450°C for 3 hours. There were no significant differences between the samples.

suppression of hot-carrier degradation for the  $D_2$  annealed sample was observed. **Figure 5** shows the dependence of device lifetime on substrate current for the  $D_2$ ,  $H_2$ ,  $N_2$ , and  $3\% H_2/N_2$  annealed samples under channel hot-carrier stress. The figure shows that, under the given conditions, the



Figure 4

Drain current degradation in D<sub>2</sub>, H<sub>2</sub>, N<sub>2</sub>, and 3% H<sub>2</sub>/N<sub>2</sub> annealed samples under channel hot-carrier stress as a function of stress time. A superior suppression of hot-carrier degradation was observed in the D<sub>2</sub> sample.



Figure 5

Dependence of device lifetime on substrate current in D<sub>2</sub>, H<sub>2</sub>, N<sub>2</sub>, and 3% H<sub>2</sub>/N<sub>2</sub> annealed samples under channel hot-carrier stress. The lifetime is defined as the time to reach a 10% degradation in saturation current. The D<sub>2</sub> sample yielded the best hot-carrier immunity.

lifetime of the  $D_2$  annealed sample is about 5 to 17 times longer than the lifetime of the non-annealed sample. The D profile obtained by SIMS shown in **Figure 6** confirms that D atoms were introduced up to the gate dielectrics.

To clarify where hot-carrier degradation occurred, we plotted gm vs. Vg-Vth for  $D_2$  and  $H_2$ annealed samples during the stress (**Figure 7**).





Depth profiles of D, H, and N atoms in the interlayer dielectrics measured by secondary ion mass spectroscopy. D atoms were detected at the gate-oxynitride/silicon-substrate interface, and a small amount of H atoms was incorporated in the SIO interlayer dielectrics.

For both the  $D_2$  and  $H_2$  annealed samples,  $g_m$  is degraded mainly near the maximum of the curve and is only slightly degraded at high values of Vg, indicating that the degradations are mainly caused by a reduction in electron mobility due to damage done to the dielectrics beneath the gate electrode.<sup>14)</sup> These results confirm that D atoms diffused and were incorporated at the gate-oxynitride/silicon-substrate interface beneath the gate dielectrics, even though there were six intermediary metal/dielectric layers.

We further investigated the thermal/chemical instability of the interfacial D atoms. **Figure 8** shows the lifetimes of additionally annealed samples. An additional  $N_2$  anneal at 450°C decreased the lifetime, implying the easy removal of D atoms at the interface. An additional  $H_2$  anneal further reduced the lifetime down to the lifetime of non-annealed samples.

## 2.4 Reaction of D atoms in the dielectric layers

The incorporation of H or D atoms in the dielectric layers was checked by observing the characteristic stretching frequencies of OH(D),



Figure 7

Degradation of transconductance during hot-carrier stress. In the  $H_2$  and  $N_2$  samples,  $g_m$  is degraded mainly near the maximum of the curves, meaning the degradations are chiefly caused by damage to the gate dielectrics beneath the gate electrode.



#### Figure 8

Device lifetimes of samples additionally annealed in  $N_2$  or  $H_2$  ambient at 450°C for 2.5 hours after  $D_2$  annealing at 450°C for 30 minutes. Additional annealing decreased the lifetime by removing the D atoms at the interface.

NH(D), SiH(D) in the infrared light region. We noted that the  $D_2$ ,  $H_2$ , and  $N_2$  samples had the same amounts of incorporated H atoms and no D atoms remained after the  $D_2$  anneal, suggesting that D atoms migrate through the layer very quickly without exchange reactions. Although our SIN layer, which was plasma-deposited at the low temperature of 400°C, has a large number of NH and SiH structures, their chemical structures were basically stable, even after  $D_2$  annealing at 450°C. We did not observe an accumulation of H(D) atoms in the layer during annealing, which was inconsistent with the conclusion of a recent report.<sup>15</sup>

On the other hand, the SION layer showed interesting behaviors, depending on the annealing conditions. As shown in **Figures 9 (a)** and **(b)**,

about 1/5 of the NH structures (3380 cm<sup>-1</sup>) were changed to ND structures (2480 cm<sup>-1</sup>) by  $D_2$  annealing, while annealing in  $H_2$  and  $N_2$  did not affect the NH structures. It is surprising that the ND structures were unaffected by the additional anneal in  $N_2$  and  $H_2$ . This result suggests that the exchange process is not simply thermal. The same feature in the exchange process was also seen with SiH structures in the SION layer, **Figure 9 (c)**. So far, no clear explanation for this feature has been suggested.

#### 2.5 Summary of the electrical test

1) We demonstrated that the introduction of D atoms into the gate-oxynitride/silicon-substrate interface through six metal/dielectric layers is thermally possible and that it improves the channel hot-electron reliability. 2) The exchange reaction with H atoms in the SION interlayer dielectrics works as a trap for D migration. The trapped D atoms form ND and SiD atoms and are quite stable. However, some D atoms escape the trap and reach the Si/SiO<sub>2</sub> interface to form SiD bonds that decompose thermally at 450°C, as is illustrated in **Figure 10**. 3) Initially bonded H atoms in the SIO and SIN layer did not affect the migration of D atoms, even at  $450^{\circ}$ C.

### 3. Proposed mechanism of the large isotope effect

### 3.1 Theoretical approach

At the beginning of their demonstration, Lyding et al. started a trial to explain the large isotope effect on the surfaces and the interface.<sup>1)</sup> Since the electronic structures of hydrogen and deuterium at the interface and anywhere else are identical, the large isotope effect must have something to do with their difference in mass.

The simplest explanation is that this phenomenon is caused by the higher activation energy of deuterium due to its lower zero-point energy. However, this explanation conflicts with the observed temperature-independence of the desorption yields from the surfaces. For a simi-



#### Figure 9

Evaluation of H and D atoms incorporated in SION under various annealing conditions. Characteristic stretching frequencies of NH (a), ND (b), and SiH (C) in the infrared region were observed using FTIR.



Figure 10

A Deuterium migration model with traps. The exchange reaction with H atoms in the SION works as a trap for deuterium migration. The trapped D atoms in the SION layer are more stable than those at the interface.

lar reason, this phenomenon cannot be explained by H or D tunneling through the barrier. A different mechanism that involves the quenching of an excited state was first discussed by Menzel and Gomer.<sup>16)</sup> In this mechanism, the isotope effect is due to the large mass of deuterium and its influence on the extent of quenching. Both H and D feel the same repulsion as they move along the excited-state potential curve. However, D moves more slowly and stays in the vicinity of the silicon substrate surface longer so that the corresponding state is more heavily quenched. Therefore, the excited SiD can dissipate its energy to the silicon lattice-phonons much easier than the SiH. The mechanism was first applied to explain the desorption yield in the low-voltage bias region by Shen et al.<sup>10)</sup> They used a theoretically calculated vibrational barrier height of 1.5 eV and a vibrational energy of 0.26 eV (2200 cm<sup>-1</sup>) for the stretching vibration. Because it required the fifth or sixth excited states to desorbe and the energy quantum of 0.26 eV was very different from the 0.064 eV (520 cm<sup>-1</sup>) value for the silicon phonon, the mechanism remained controversial.<sup>17)-26)</sup> Van de Walle<sup>22)</sup> pointed out that the silicon phonon strongly interacted with the SiH bending instead of the SiH stretching. He assumed that the vibrational energies of the SiH and SiD bending



Figure 11

P-polarized IR spectra in Si-H and Si-D stretching region obtained after 100 internal reflections. The resolution was  $0.0125 \text{ cm}^{-1}$ .

were 0.081 eV (650 cm<sup>-1</sup>) and 0.057 eV (460 cm<sup>-1</sup>), respectively, and showed that the dissipation from the SiD bending to the silicon phonon was efficient by considering the energy conservation. Our experimental results presented below support Van de Walle's model,<sup>27)</sup> except that we observed the following bending vibrational energies: 626.6 cm<sup>-1</sup> for SiH and 536.8 and 415.4 cm<sup>-1</sup> for SiD.

#### 3.2 Spectroscopic test

The mechanism was experimentally tested by monitoring the dissipation efficiencies for SiH and SiD bendings.<sup>27)</sup> If the dissipation through the SiD bending is efficient, one can expect an energetically broader bending, because efficient dissipation is another expression of the short duration of the corresponding vibration.

**Figure 11** shows the spectral feature of the Si-H and Si-D stretching region. The Si-H stretching was seen at 2083.7 cm<sup>-1</sup> with a width of 1.1 cm<sup>-1</sup>. The absorption features shown in Figure 11 agree with various reports that the surface is homogeneous from an infrared-spectroscopic point of view. <sup>28),29)</sup> Due to the deuteration, the peak was shifted to 1515.6 cm<sup>-1</sup> with a width of 1.4 cm<sup>-1</sup>.



Figure 12

Transmission IR spectra in the bending region. Incidence angle was 45°, and the resolution was 0.0125 cm<sup>-1</sup>. Spectra with broad features are shown at a reduced resolution of 0.5 cm<sup>-1</sup>. Arrows show reproducible peaks.

The bending region from 1000 to 400 cm<sup>-1</sup> was observed in the transmission geometry of the sample surface whose stretching we obtained. The bending spectra are shown in **Figure 12**. A very narrow (1.1 cm<sup>-1</sup>) peak due to Si-H wagging is seen at 626.6 cm<sup>-1</sup>, and its transition dipole is known to be in the (111) plane.<sup>30)</sup> We did not observe any other peaks with absorption intensities above 0.0005 in the wavenumber region down to 400 cm<sup>-1</sup>. On the deuterated surface, we observed two broader and weaker peaks at 536.8 cm<sup>-1</sup> and 415.4 cm<sup>-1</sup> having widths of 3.4 cm<sup>-1</sup> and 3.5 cm<sup>-1</sup>, respectively.

As shown in Figure 12, the two bending modes of D:Si(111)  $1\times1$  were observed to be three to four times broader than the corresponding modes of H:Si(111)  $1\times1$ . These broadenings are not due to the inhomogeneity, because the stretching gives a narrow peak, as stated above, and clear electron diffraction spots of a  $1\times1$  surface structure have been confirmed. We observed stretching and bending peaks that were well separated and had an anisotropic nature derived from normal coordinates based on a simple structural model

that considers the surface Si-H/D layer. The good separation and anisotropic nature indicate that this model provides a good representation of vibration and the two modes are well isolated from each other and substrate phonons. Therefore, the source of the width can be treated as a perturbation. The interaction with the Si-D bending modes at 536.8 and 415.4 cm<sup>-1</sup> may well be caused by phonons of the substrate Si. Note that the highest phonon frequency at the gamma point of Si crystal is 520 cm<sup>-1</sup> at 300 K. The two bending modes are therefore located just above and below that frequency. Considering the symmetry, phonons are most likely to occur at the zone boundary of the momentum space. The broadening mechanism is not thought to include the specific symmetry of the surface structure; rather, it includes simple three-dimensional interactions. On a D:Si(110) 1×1 surface, the Si-D bending modes were separated into two peaks at 522 cm<sup>-1</sup> and 439 cm<sup>-1</sup>, and these peaks were several times broader than those of Si-H bending at 611 cm<sup>-1</sup> on H:Si(110)  $1 \times 1$ . This experiment supports the above idea about the source of the broadening. Among the possible known mechanisms,<sup>31)</sup> the most likely explanation of the broadening is the phase relaxation, which has been successfully used to explain the temperature dependence of the stretching peak width.

The vibration of these atoms is repeatedly excited electrically during MOS device operation until the bonds are finally broken.<sup>22)</sup> It is suggested that during the accumulation of vibrational energy, the Si-D wagging vibration is a more effective cooling pathway than Si-H wagging.<sup>22)</sup> This is because the wagging frequency is expected theoretically to be very close to the substrate phonon frequency,<sup>10)</sup> and therefore, it might be strongly coupled with the heat bath of the substrate. At the interface, the inhomogeneity is expected to give a somewhat larger absorption width. However, since the corresponding peak wavenumber is unaffected by the inhomogeneity, the above discussion on the homogeneous surface is still meaningful. Our spectroscopic observations possibly indicate the existence of an effective dissipation pathway associated with D atoms through the interaction of the surface layer with substrate Si phonons.

## 3.3 Other effects on electrical characteristics

Deuterium can also be introduced at the interface to control parameters other than the hot-carrier reliability. However, although several theoretical approaches have been made,<sup>32)-40)</sup> there have been no results consistent with device tests so far.

## 4. Summary

In this paper, we reviewed recent experimental and theoretical findings critical for process integration of deuterium post-metal anneals. We demonstrated that the introduction of D atoms into the gate-oxynitride/silicon-substrate interface through six metal/dielectric layers is thermally possible and that it improves the channel hot-electron reliability. We then described our investigations of D diffusion through inter-metal dielectric layers and the chemical reaction with existing H atoms using SIMS and infrared spectroscopy. Next, we proposed a mechanism that explains the large improvement in hot-electron reliability that is observed when deuterium is introduced. Finally, we described spectroscopic observations we made that support our mechanism, including its treatment of the dissipation of excited vibrational energy to the substrate silicon lattice.

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