<100> Strained-SiGe-Channel p-MOSFET with Enhanced Hole Mobility and Lower Parasitic Resistance

● Masashi Shima

(Manuscript received December 10, 2002)

Employment of the <100> channel direction in a strained-$Si_{0.8}Ge_{0.2}$ p-MOSFET provides a hole mobility enhancement as large as 25% and a parasitic resistance reduction of 20% compared to a <110> strained-$Si_{0.8}Ge_{0.2}$ channel p-MOSFET, which already has a better mobility and threshold voltage roll-off than the Si p-MOSFET. These results suggest that the <100> strained-SiGe-channel p-MOSFET can be used to achieve high-speed CMOS devices that operate at low voltages.

1. Introduction

High-speed devices require a large charging current that is obtained by either reducing their channel length or increasing their carrier mobility. Recent difficulties encountered in sub-0.1 μm research have driven some groups to develop technologies that increase carrier mobility by introducing strain. Two promising candidates that have resulted from this research use an SiGe crystal to form a strained channel structure. One is a strained Si channel structure grown on a relaxed SiGe buffer layer of several microns that has threading dislocations at a density of 10^4 to 10^6 cm^{-2}.[1),2)] Although, especially in n-MOSFETs, a large carrier mobility enhancement has been demonstrated, a thick SiGe buffer layer prevents the development of a practical process technology. The other candidate is a strained SiGe channel structure grown on a normal Si substrate.[3)-8)] An SiGe layer several nm thick provides the big advantage that only a small change from the standard fabrication process is needed for hole mobility enhancement. It also improves the characteristics of p-MOSFETs so that the difference in current drivability between p- and n-MOSFETs is eliminated, which simplifies CMOS circuit design. This paper reports on additional characteristics improvements that can be achieved in strained-SiGe p-MOSFETs having gate lengths as short as 0.1 μm by changing the channel orientation.

2. Electronic-band structure

The calculated electronic-band structures of the valence bands of relaxed-Si and strained-SiGe are shown in **Figures 1 (a)** and **(b)**, respectively.[3),9)] In the case of relaxed-Si {Figure 1 (a)}, the anisotropic heavy hole (HH) and light hole (LH) bands degenerate near the G point. On the other hand, a biaxial compressive strain in SiGe creates an energy gap between the HH and LH band energies and induces band mixing. This leads to the merits that the hole effective mass in the lower energy band is small and anisotropic {Figure 1 (b)} and inter-band scattering between the two mixed bands is reduced. The (100) and (110) directions in the electronic-band diagrams correspond to the <100> and <110> channel directions of real-space MOSFETs {**Figure 1 (c)**}. The large population of holes in the anisotropic lower energy band suggests that the electrical characteristics of

strained-SiGe p-MOSFETs are strongly dependent on orientation.

3. Device fabrication

Figure 2 shows a cross-sectional TEM image of the fabricated strained-SiGe-channel p-MOSFET. The dark area is a strained SiGe layer that exists in the channel region and the extension regions under each sidewall. The left inset in Figure 2 shows the strained-SiGe structure, which was grown by ultra-high vacuum chemical vapor deposition (UHV-CVD). An 11 nm Si-cap layer, 10 nm strained-$Si_{0.8}Ge_{0.2}$ layer, and 100 nm Si-buffer layer were grown epitaxially on an Si(001) substrate. Growth of the strained SiGe structure was followed by a conventional CMOS process with LOCOS isolation as shown in **Figure 3**. High-energy phosphorus and low-energy arsenide implants were used to form retrograde-wells. Low-energy, high-dose arsenide implants were used to control the threshold voltage without the need for punch-through implants. Then, boron implants were used to form extension regions after formation of a 2.9 nm-thick thermal gate oxide and a poly-Si gate. The Si-cap layer grown on the SiGe layer was exhausted after the formation of a sacrificial oxide for ion implantation and the gate oxide. Finally, formation of a sidewall was followed by high-dose boron implants and rapid thermal annealing. Formation of silicide was omitted to simplify the fabrication process. We fabricated strained-SiGe-channel p-MOSFETs along the <100> and <110> directions on separate wafers in order to investigate the channel orientation dependence of the electrical characteristics.

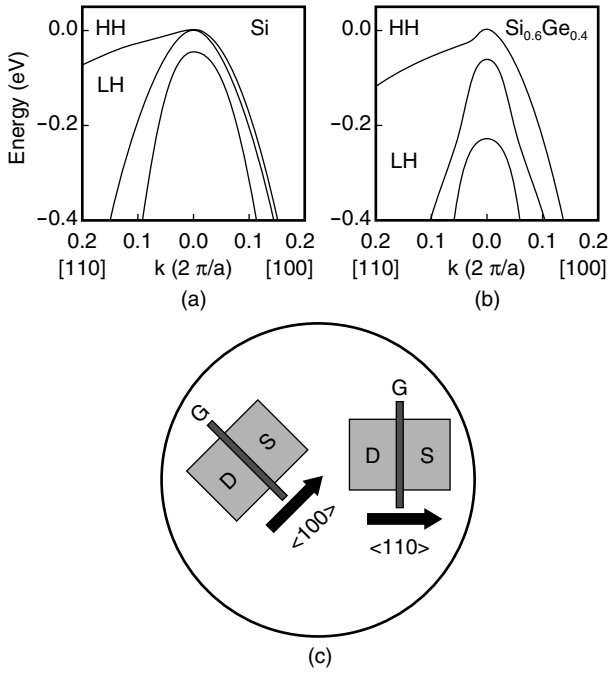

Figure 1
Electronic energy band structure and its orientation dependence in (a) unstrained Si and (b) strained SiGe.

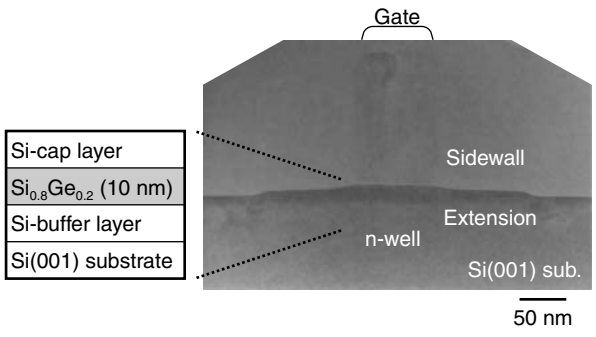

Figure 2
Cross-sectional TEM image of strained-SiGe-channel p-MOSFET and its epitaxially grown structure.

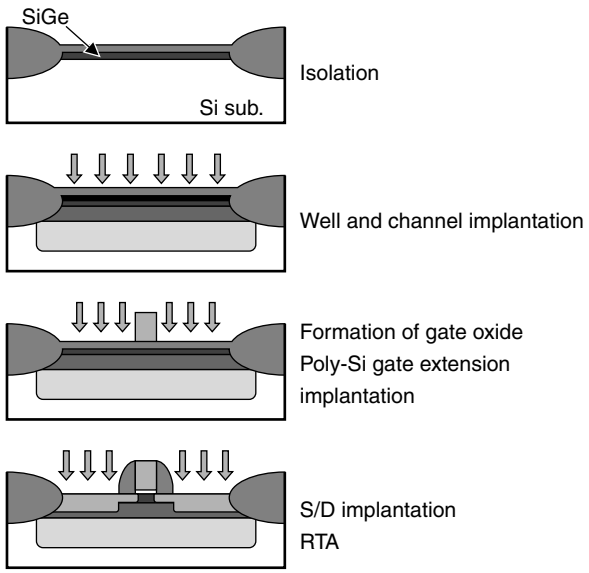

Figure 3
Fabrication process.

4. Electrical characteristics of fabricated p-MOSFETs

In order to increase the current drivability of MOSFETs, it is necessary to increase the mobility and reduce the parasitic resistance without decreasing the gate capacitance. **Figure 4** shows the split capacitance-voltage (C-V) characteristics of the <100> strained-SiGe, <110> strained-SiGe, and <110> Si p-MOSFETs. The fact that the three capacitances are the same at the gate voltage V_g at which the inversion layer forms is evidence that the Si-cap layer has been exhausted. **Figure 5** shows measured mobilities in these three devices as a function of V_g minus the threshold voltage V_{th}. The figure shows that at V_g-V_{th} = −1.2 V the strained-SiGe-channel p-MOSFET with a <100> channel orientation has a 25% higher mobility than the same device with a <110> channel orientation. Also, at the same voltage, the <110> strained-SiGe-channel p-MOSFET has about a 20% higher mobility than the <110> Si channel p-MOSFET. In the case of relaxed Si p-MOSFETs, the mobility enhancement resulting from the change of channel orientation is reported to be only a few percent.[10] The large mobility enhancement in the strained-SiGe MOSFETs is considered to have resulted from a large population of holes in the non-degenerate anisotropic band made by mixing the HH and LH bands. **Figure 6** compares the single-side parasitic and contact resistances. A reduction in parasitic resistance of about 20% was

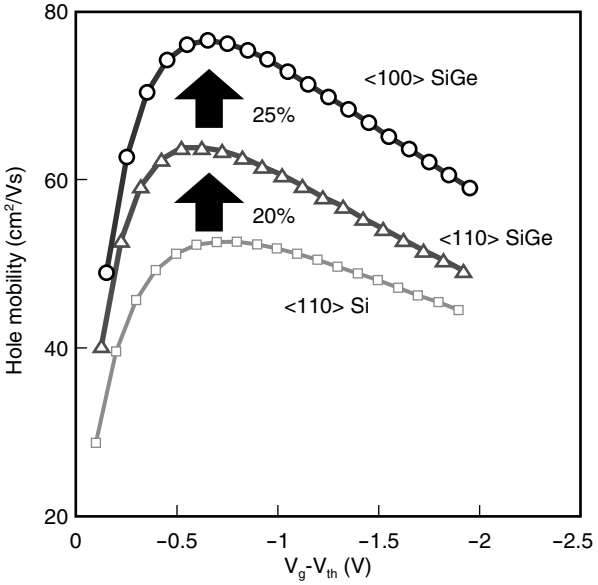

Figure 5
Comparison of mobilities.

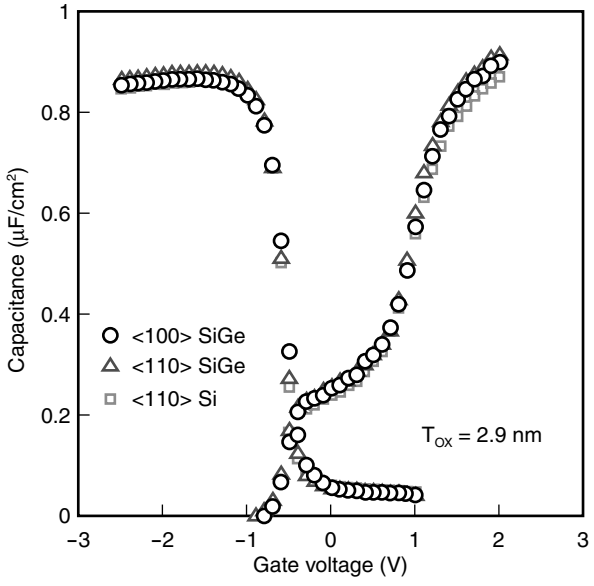

Figure 4
Capacitance-voltage characteristics of p-MOSFETs.

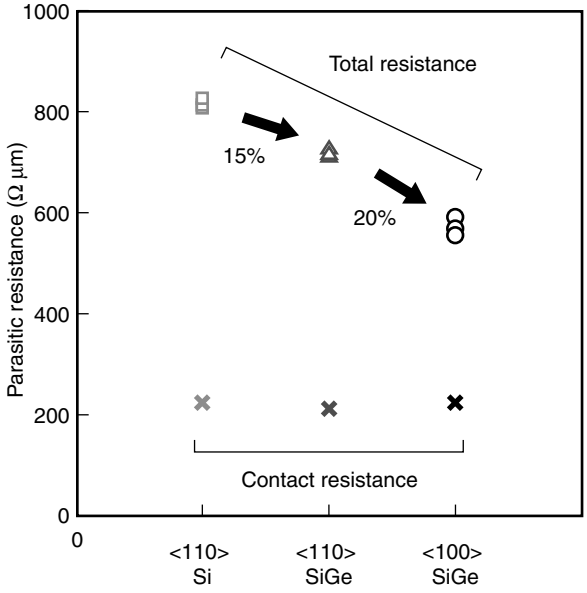

Figure 6
Comparison of parasitic resistances.

obtained by changing the channel orientation of the strained-SiGe p-MOSFET. Because the contact resistance was almost the same, the difference is considered to be due to the difference in the lateral resistance of the extension region. When the gate length is reduced to below 0.1 μm and the oxide thickness is made thinner to increase the drive current, the advantage of a lower parasitic resistance becomes much more important. **Figure 7** shows the drain current-drain voltage (I_d-V_d) characteristics of 0.1 μm gate-length devices. The <100> strained-SiGe p-MOSFET shows a steeper increase of I_d and a larger saturation current than the <110> strained-SiGe p-MOSFET. This increase is due to the larger mobility, larger saturation velocity, and lower parasitic resistance of the <100> strained-SiGe p-MOSFET.

When the channel length of electron devices is reduced, we need to ensure there is a minimal increase in off current; otherwise, there will be an unacceptable increase in power consumption. **Figure 8** compares the I_d-V_g characteristics of strained-SiGe and Si p-MOSFETs having the same channel implant density. The sub-threshold slopes of the I_d-V_g characteristics are the same, indicating that the strained-SiGe channel p-MOSFETs have the same resistance to an increase in off current as the Si p-MOSFETs. **Figure 9** compares the I_{on}-I_{off} characteristics of <100> and <110> strained-SiGe-channel p-MOSFETs having gate lengths from 0.1 to 1.0 μm. It was clearly observed that changing the channel orientation from the

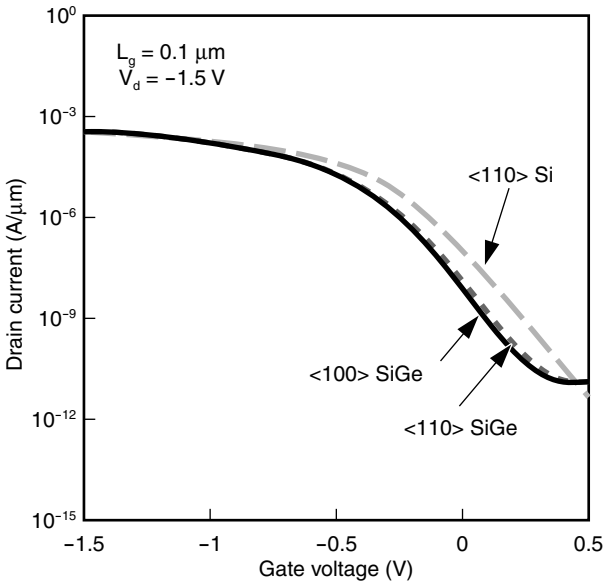

Figure 8
Comparison of I_d-V_g characteristics.

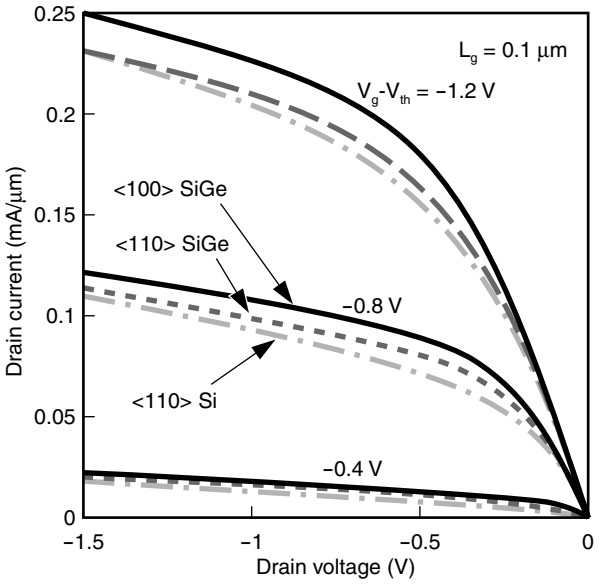

Figure 7
Comparison of I_d-V_d characteristics.

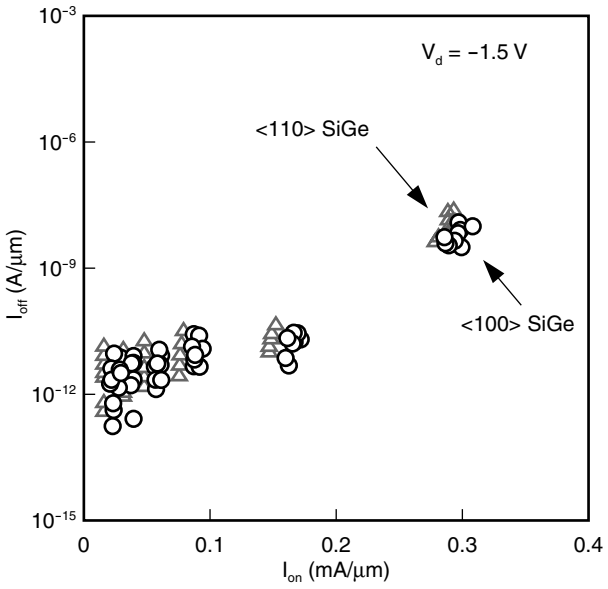

Figure 9
Comparison of I_{on}-I_{off} characteristics.

<110> to <100> direction increases I_{on} without increasing I_{off}. **Figure 10** compares the V_{th} roll-off characteristics when there are no pocket implants. The difference between the V_{th} of the SiGe and Si p-MOSFETs at long gate lengths is explained by the electronic energy offset in the valence band. This relation is reversed due to better roll-off characteristics when the gate length is reduced to 0.1 μm. The better roll-off characteristics of strained-SiGe channel p-MOSFETs make strained-SiGe technology attractive for use in short-channel devices.

5. Conclusions

A <100> strained-SiGe channel p-MOSFET has demonstrated a hole-mobility enhancement of about 25% and a parasitic resistance reduction of about 20% compared to a <110> strained-SiGe channel p-MOSFET, which already has a better mobility and threshold voltage roll-off than the Si p-MOSFET. These results suggest that the <100> strained SiGe channel p-MOSFET can be used to achieve high-speed CMOS devices that operate at low voltages.

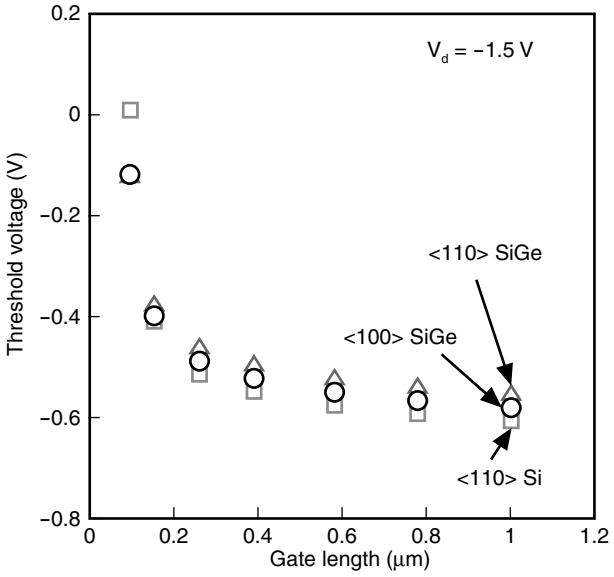

Figure 10
Comparison of V_{th} roll-off characteristics.

References

1) K. Rim et al.: Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's. *IEEE transactions on Electron Devices*, **47**, 7, p.1406-1415 (2000).
2) F. Schaffler et al.: High-mobility Si and Ge structures. *Semicond. Sci. Technol*, **12**, p.1515-1549 (1997).
3) Y. Yeo et al.: Enhanced Performance in Sub-100nm CMOSFETs Using Strained Epitaxial Silicon-Germanium. International Electron Devices Meeting Technical Digest, p.753-756, 2000.
4) D. K. Nayak et al.: Enhancement-Mode Quantum-Well Ge_xSi_{1-x} PMOS. *IEEE Electron Device Letters*, **12**, 4, p.154 (1991).
5) V. P. Kesan et al.: High Performance 0.25μm p-MOSFETs with Silicon-germanium Characteristics for 300K and 77K Operation. International Electron Devices Meeting Technical Digest, p.25-28, 1991.
6) T. Tezuka et al.: Novel fully-depleted SiGe-on-insulator pMOSFETs with high-mobility SiGe surface channels. International Electron Devices Meeting Technical Digest, p.946-948, 2001.
7) K. Goto et al.: Fabrication of a $Si_{1-x}Ge_x$ Channel Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) Containing High Ge Fraction Layer by Low-Pressure Chemical Vapor Deposition. *Japanese Journal of Applied Physics*, **32**, p.438-441 (1993).
8) M. J. Palmer et al.: Effective mobilities in pseudomorphic Si/SiGe/Si p-channel metal-oxide-semiconductor field-effect transistors with thin silicon capping layers. *Applied Physics Letters*, **78**, p.1424-1426 (2001).
9) J. M. Hichley et al.: Hole transport theory in pseudomorphic $Si_{1-x}Ge_x$ alloys grown on Si(001) substrates. *Physical Review*, **B-41**, 5, p.2912-2926 (1990).
10) H. Sayama et al.: Effect of <100> Channel Direction for High Performance SCE Immune pMOSFET with Less Than 0.15μm Gate

Length. International Electron Devices Meeting Technical Digest, p.657-660, 1999.

Masashi Shima received the B.E. degree in Mechanical Engineering from Waseda University, Tokyo, Japan in 1989 and the M.S. degree in Materials Science and Engineering from Tokyo Institute of Technology, Tokyo, Japan in 1991. He joined Fujitsu Laboratories, Ltd., Atsugi, Japan in 1991, where he has been engaged in research and development of short-gate HEMTs and quantum effect devices. He is currently developing high-speed, low-power CMOS devices. He is a member of the Japan Society of Applied Physics.